Doctoral Thesis

Quasi-Eight-Level Inverter with Output-Side Transformers for Single-Phase Off-Grid Electrical Energy Supply

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by

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Leoben October 2010

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I declare in lieu of oath, that I wrote this thesis and performed the associated research myself, using only literature cited in this volume.

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Kurzfassung

Vor Ort verfügbare erneuerbare Energiequellen sind ideal für die Bereitstellung der Stromversorgung in entlegenen Gebieten geeignet. Gegenwärtige Lösungen erfordern hohen Aufwand an Leistungselektronik und deren Ansteuerungen, um eine gute Qualität der Ausgangsspannung zu erzielen. Diese Arbeit beschreibt das Design und Layout einer speziellen einphasigen Stromversorgung mit einer hohen Spannungsqualität und einem geringen Aufwand an Leistungselektronik durch Anwendung eines speziellen Quasi-Acht-Punkt-Wechselrichters mit Hilfe einzelner H-Brücken.

Zunächst werden die verschiedenen Möglichkeiten der Umsetzung eines mehrstufigen Wechselrichters für netzgekoppelte und seine Stromversorgung untersucht und die Vorteile und Nachteile der jeweiligen Lösung ausgezeigt und ein H-Brücken-Modul entworfen und gebaut. Mithilfe diese Module und einigen innovativen Konzepten wird ein Modell eines mehrstufigen Wechselrichters entwickelt und eine Reihe von vorläufigen Messungen durchgeführt.

Unsere neuen Erkenntnisse haben Vorteile im Vergleich zu anderen standard Multi-Level-Wechselrichter-Topologien. Gemeinsame Ansätze haben Trenntransformatoren mit Delta-, Stern-oder Zickzack-Wicklung Verbindungen. Der komplexeste Teil ist, um die benötigten Parameter wie Induktivität und Widerstandswerte des einzelnen Transformators zu bestimmen. In dieser Arbeit werden alle Wechselrichter durch einen gemeinsamen Zwischenkreis eingespeist. Die Transformatoren sind am Ausgang der Wechselrichter, der die primäre Seiten jedem Wechselrichter parallel geschaltet und die sekundären Seiten in Reihe geschaltet sind. Gruppierung von diesen sieben Transformatoren als 1, 2 und 4 können insgesamt 7 Spannungsebenen hergestellt werden. Bezugnehmend auf Sinusförmigesspannung, jede Gruppe von Transformatoren funktionieren unterschiedlich in einer Periode. Daher der Klirrfaktor und die Verluste der Wechselrichter bestimmen Schaltzustände dieser drei Gruppen von Transformatoren. Schaltfrequenzen zwischen 4 kHz...20 kHz, sind die wichtigsten Arbeitsbereich des MOSFETs Wechselrichter und experimentellen Ergebnisse zeigen, besser Ausgangsspannung mit zunehmender Frequenz.

Diese Vorteile verhindern Filter Umsetzung welche in der Regel eine gemeinsame Lösung ist und auch eine Verringerung der Kosten bei dieser Art von Systemen.

Abstract

Renewable energy resources available locally are ideally suited for providing electricity supply in remote areas. This work describes design and layout of a special single phase supply system with high voltage quality and low power electronics expenditure through application of a special quasi-eight-level inverter output voltage shape with H-bridge circuit configuration. The task is to minimize the number of stochastic and unknown parameters influencing the device functionality.

First, the different possibilities to implement a multilevel inverter for grid and its power supply are explored, pointing out the advantages and disadvantages of each solution. Then, an H-bridge-module is designed and built. With these modules and together with some innovative concepts a model of a multilayer inverter is developed and a set of preliminary measurements are gained.

Our new contribution has advantages compared to other standard multilevel inverter topologies. Common inverter approaches have isolation transformers with delta, star, or zigzag winding connections. The most complex part is to determine the needed parameters such as inductance and resistance values of each transformer. In this thesis, all the inverters are fed by a common DC bus. The transformers are located at the output side of the inverters which the primary sides are connected to each inverter in parallel and the secondary sides are connected in series. Grouping of these seven transformers as 1, 2 and 4, total 7 voltage levels can be produced. Referring to sinus voltage, each group of transformer acts differently in one period. Therefore, switching states of these three groups of transformers determine the total harmonic distortion and losses of the inverters. Switching frequencies between 4 kHz…20 kHz, are the main operation area of the MOSFETs inverter and experimental results show better output voltage with the increasing frequencies.

These advantages prevent filter implementation which is usually a common solution and also decrease the costs in such kind of systems.

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1 Introduction

In the period from 2003 to 2008, wind power capacity increased from 40GW to 120GW, solar photo-voltaic power capacity increased from 2GW to 13GW [24]. Continuous improvements are urgently needed in all industrial and consumer applications. This is the case of a large number of new active systems, such as wind turbines, photovoltaic systems, and others [4][6][30][46][49][121]. The new developments in semiconductors which allow an increase of their maximum voltage, current and switching frequency, investment reduction, reliability, quality of output voltage, in such a way that it is possible to design efficient and reliable Voltage Source Converters for Middle Voltage applications [8][10][34][62]. Among these designs, two-level Voltage Source Converter (2L-VSC) with active-front-end and transformer configurations is mainly employed and therefore, this dissertation deals with the improvement of control and comparison of these switching devices [95][121]. First, the basic operation principles and several mathematical models of the VSC are presented including some design considerations and establishing the main specifications and features of a 2L-VSC under several operation conditions.

The performance of an inverter with any switching strategies can be related to the harmonic contents of its output voltage [3][67][69][88]. As the number of input voltage levels increase, the output waveform approaches the sinusoidal wave with minimum harmonic distortion. H-bridge converter for producing an ac voltage employ switches which may be transistors (MOSFET or IGBT), or at very high power, thyristors (GTO or GCT)[5][21][33]. This thesis provides a comprehensive analysis on low-voltage converter and inverter topologies which are different in many aspects from those for high-power voltage drives, drive system configurations, and control schemes. The aim of this thesis is a new control method for low voltage converters. There is a large variety of converter models and topologies with power semiconductors (IGBTs, IGCTs, and GTOs). However, there is no application of MOSFETs converters realized and compared to standard ones viewing several parameters of new research areas.

With the development of power electronics in the recent years, the medium-voltage (MV) and high power applications have been proposed as the most competitive choice increasingly used in several industries to conserve electric energy, increase productivity and improve product quality. Many different topologies such as two-level Voltage Source Converter (2L-VSC), series connected H-Bridge Voltage Source Converter (SCHB VSC), three-level Neutral Point Clamped Voltage Source Converter (3L-NPC-VSC) have been raised from the early idea of multi-level waveforms generation.

PWM-modulated Voltage Source Converter (VSC) is more and more used as active front-ends in several applications and especially in supplying variable-speed drives [29]. Multilevel topologies are frequently used mainly in order to reduce the line-side current harmonic content and to overcome the problems due to the limited rated voltages of the switching devices available on the market. In the paper a very efficient control strategy of a multilevel cascaded H-bridge VSC is presented. Depending on the maximum value of the switching frequency selected through losses or from harmonics considerations, optimized performances can be obtained in terms of reduction of the harmonic content of line-side currents and reduction of line reactive power.

1.1 Structure of Thesis

Chapter 2 is a review of the state-of-the-art with different possibilities to build a number of converters and rectifiers based of the application requirements, such as power semiconductors, dc link capacitors, and transformers.

Chapter 3 discusses the Quasi-Eight-Level Inverter control operation performance for MV off-grid connected applications. The several types of multi-level inverters and configurations of transformers and harmonics cancellation seen as an input of the whole system are compared.

Chapter 4 reports the mathematical procedure used to design the main components of Multi-level Voltage source converters (VSC) which have received a lot of attention in the recent years. These converters have been proposed as the best choice in a wide variety of medium voltage (MV) applications including cascaded H-Bridge inverters. These topologies have better output voltage quality, reduced electromagnetic interference (EMI) problems, and lower overall losses in some cases. The basic converter, including the MOSFETs, modulation and switching frequency is described in this chapter is focused on modelling each component of the considered system. The frame of this chapter is also a detailed description of the simulation and experimental results which have been carried out in order to verify the proposed algorithms. The theory of operation of the inverter design is described in detail: a simulation model is built and its validity is tested against actual measurements. Mathematical models and some design considerations are presented, extending these ideas in order to select the passive electric components for 230V-4kVA operation conditions.

Chapter 5 describes the modelling and simulation of each detailed phases in this work. The modulation, losses, and efficiency of pre-mentioned converters are calculated and compared. Simulation results describe the fundamental operation performances of the AFE rectifier, mechanical system models and design criteria of the inverter and load models.

Chapter 6 is focused on the implementation of the designed control system and experimental validation; the control system is implemented in an ATmega16 platform and tested with an experimental test setup.

Finally, chapter 7 lists the conclusions and outlines the research plans for the future.

This project is focused on the control of the grid side converter and can be organized into four main parts and is divided into seven chapters which are summarized as follows:

1. Background and project definition
2. Modelling
3. Control system design
4. Implementation and experimental evaluation

This thesis focuses on feasibility of the proposed inverter control schemes of the cascade multilevel inverter, simulation, analytical and also near single-phase, practical results of a single-phase quasi-eight-level inverter design using MATLAB-SIMULINK Power System Block is carried out.

2 State of the Art in Medium Voltage Converter Topologies

The power limit of standard converters is given by the maximum voltage and current of a switching component [14][17]. Furthermore, a low switching frequency will provide low switching losses. An initial solution to overcome this problem was to connect several switches in series or in parallel. The series connection of two or more semiconductor devices without snubber is really difficult due to the impossibility to perfectly synchronize their switching. In fact, if one component turns off faster than the others the faster one will blow up because it will be subjected to the entire voltage drop designed for the series connection.

On the other hand, parallel connection is slightly less complicated because of the property of MOSFETs and more recent IGBTs to increase their internal resistance with the increment of junction temperature [1][113][115][117]. When a component switches on faster than the others, it will conduct all the current alone than the current it was designed for that time. But in this way, the component increases its junction temperature and its resistance. Thus it limits the current which flow through it during parallel connection state. This effect makes possible to overcome the problems coming from a delay among gate signals or from differences among real turn on time of the components.

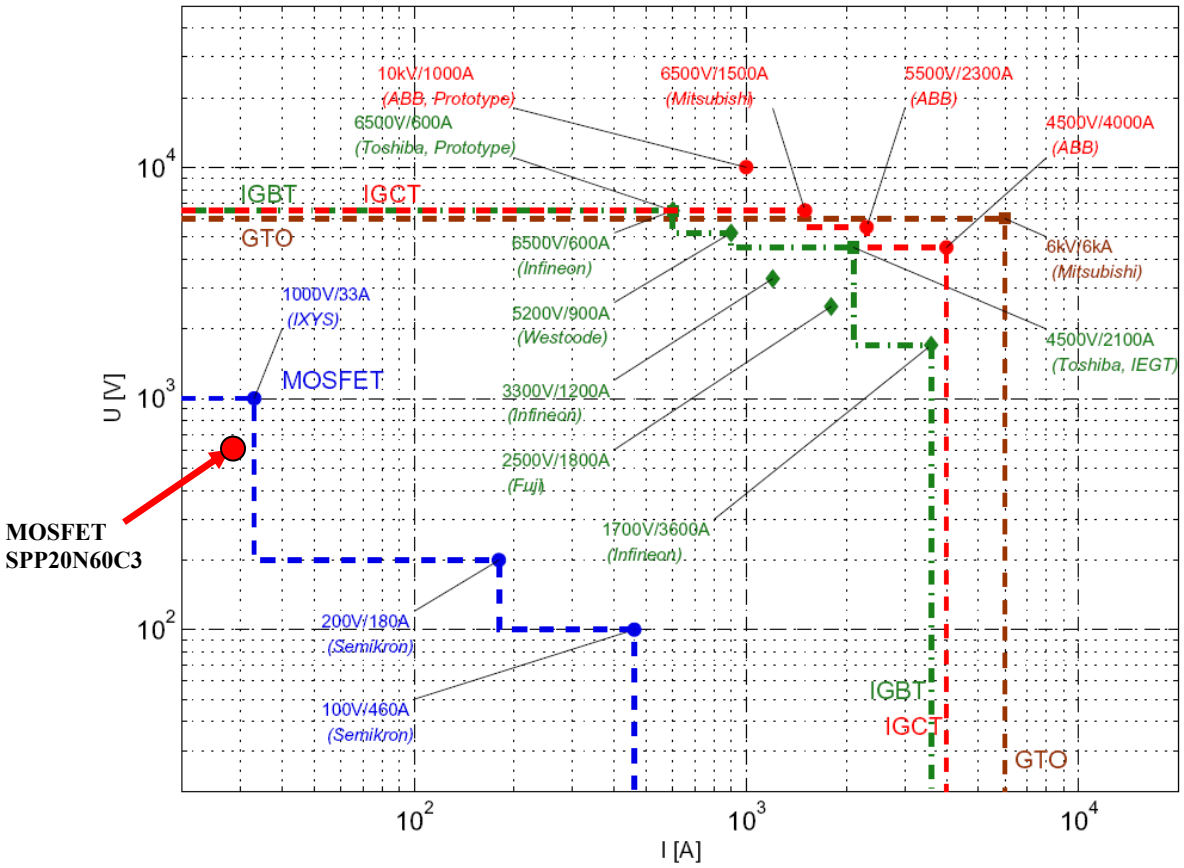


Figure 2-1: Power range of available power semiconductors [114][116]

Multilevel converters are a viable solution to increase the power with a relatively low stress on the components and with simple control systems. Moreover, multilevel converters present

several other advantages. First of all, multilevel converters generate better output waveforms than the standard converters. Then, multilevel converter can increase the power quality due to the great number of levels of the output voltage, by this way; the AC side filter can be reduced. We will propose a cable of suitable length acting as filter, decreasing costs compared to a separate filter [57]. Furthermore, multilevel converters can operate with a lower switching frequency sharing the whole voltage in small steps, so the electromagnetic emissions generated by them are weaker, to comply with the standards [15][27].

Figure 2-2 gives the methodology for designing and implementation of a system. First of all requirements must be exactly defined and test specifications including the costs should be taken in to account. Selection of architecture is the main point in a system designing. Much more time may be investigated in this phase. Measurement is also very important to prove the system reliability, searching the industry and making an equipment list.

Drafting of hardware setup is not the main issue of this work because good well-known prototypes are available in market. But, for the purpose of our implementation, we developed an inverter for possible failures which can rise during test phase. Then, with the help of simulation, several parameters are defined and results are achieved.

Structure and evaluation of a prototype is built up after having sufficient results.

Finally, test system results could be compared with the simulation and the difference between theoretical and practical ones.

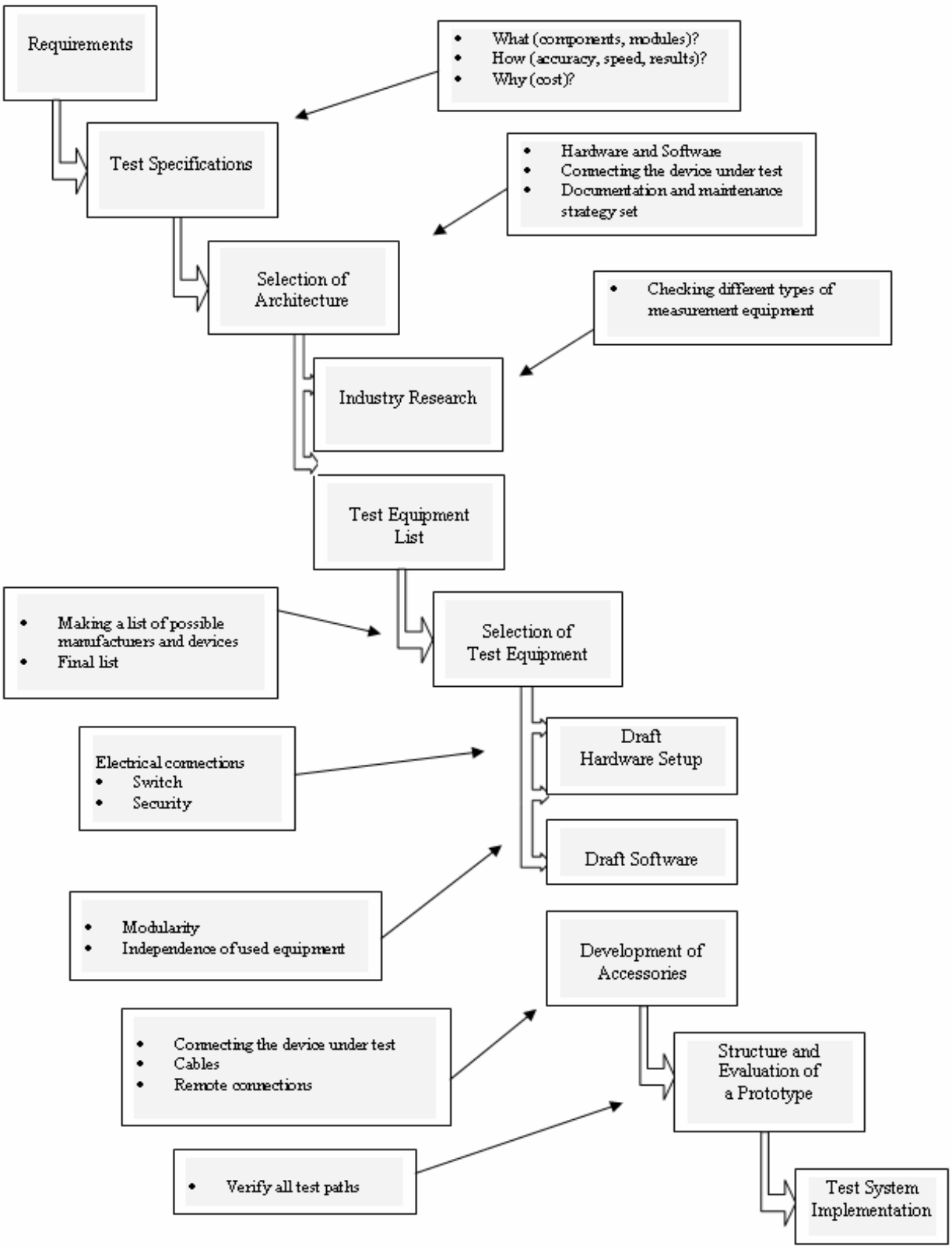


Figure 2-2: Design and implementation of a test system [26]

On the other side, because of their multi-step output voltage waveforms, the total harmonic distortion (THD) of the multi-level converter voltages is relatively low compared to the 2L-

VSC. Moreover, the effective switching frequency of the multi-level converters is a function of its number of voltage levels. In other words, to achieve the same voltage THD, a higher level converter can operate at a lower switching frequency of the individual switch. Obviously, the theoretical superiority of a multi-level converter is proportional to its number of voltage levels assuming ideal switches. However, the number of voltage levels is limited by its control complexity, complication of the system structure, cost and conduction losses. The high number of switches composing a multilevel converter may lead to the conclusion that complex algorithms are necessary [26]. Fortunately, all the modulation used for standard 2-level converters can be easily adapted to multilevel converters.

2.1 Modulation Classification

The modulation algorithm used to drive the multi-level converter give the voltage level required for each leg; the translation in the proper configuration of switches is done by other algorithms which can be hardware or software implemented. In this way, the modulation algorithm presented in chapter 3 can be used for all multilevel applications.

Actually, there are some modulation algorithms which produce output voltage shapes suited for particular multi-level topologies like the multi-carrier based PWM and the diode-clamped converters: in this case, the modulating signals are logically compatible with the required switches control which can be directly driven.

The aim of redundant configurations which is, to improve the switching pattern, to balance the current flowing through the switches, must be defined for the application. In general, low switching frequency methods are preferred for high-power applications due to the necessary reduction of switching losses, while the better output power quality and higher bandwidth of high switching frequency algorithms are more suitable for high dynamics applications [80][86][102][105].

At mixed switching frequency modulations, switches commutate at different frequencies, like hybrid multilevel modulation, and are particularly suited for hybrid converters [93][119]. Different cells can easily commutate at different frequencies. High switching frequency modulation is the adaptation of standard PWM to multi-levels and they are meant to switch at very high frequency, about 10 to 20 kHz [81]. Among them, there are Space Vector PWM (SVPWM) and Phase Shifted PWM (PSPWM) and a subclass called level shifted PWM. Phase Opposition (PO), Opposition Disposition (OD) and Alternate Opposition Disposition (AOD) modulations belong to this last group. SVPWM is the extension of the standard 2-level Space Vector Modulation to a greater number of levels. In PSPWM several phase-shifted references are used to generate the control pulses. PO, OD and AOD exploit only one reference waveform which is compared with carriers covering all the range of reference variation [45][48][79][89]. The number of used carriers is equal to M −1, where M is the number of inverter level. Cascade multi-level inverter consists of (M-1)/2 H-bridges in which each bridge's dc voltage is provided by its own dc capacitor have been developed for electric utility applications where M is the number of levels in inverter, H is the letter characterizing the topology of a 4-switch cell arrangements [126]. However, switching losses increase as the switching frequency increases. As a result, it is desirable to select the switching frequency as low as possible.

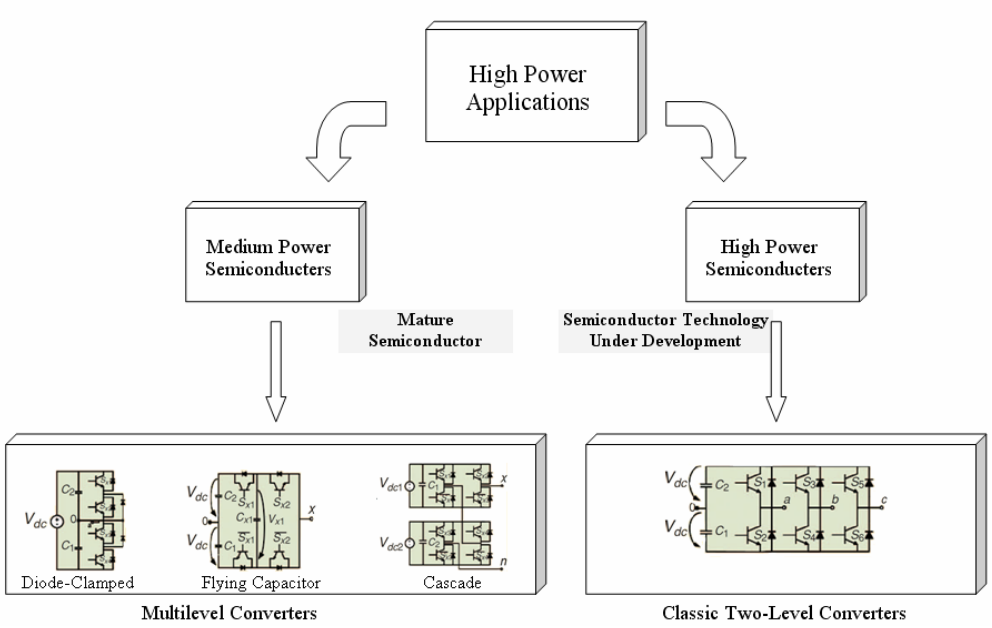


Figure 2-3: Classical two-level power converters versus most common multi-level power converters [88]

This topology requires the least number of components to achieve the same number of voltage levels. It is also possible to use modularized circuit layout and packaging because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors which are much more efficient and suitable for utility applications than multi-pulse and pulse width modulation inverters [65]. The used condensators have big capacities and control of fixing the voltage at a certain level must be performed.

2.2 Single-Phase Full-Bridge (H-Bridge) Topology

2.2.1 Configuration of Circuit

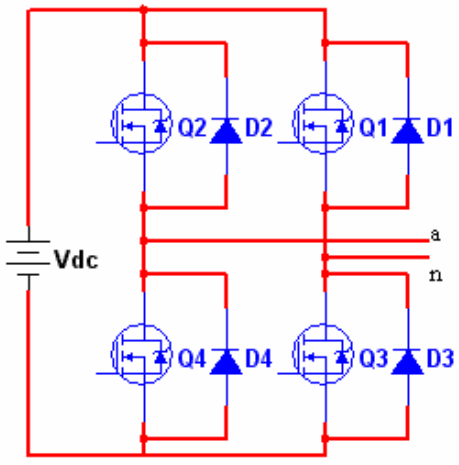


Figure 2-4: Configuration of a single-phase full-bridge (H-Bridge) VSC

The switches composed by Q1 and Q2 are the high one, whereas Q3 and Q4 constitute the low couple. The high output of one cell is shortcut to the low output of another one to realize a cascade connection between two cells.

2.2.2 Switching States and Commutations

In order to produce seven levels, the switches are controlled in such away that only two of the four switches in each H-bridge cell are turned on at any time [50]. Each cell consists of two half-bridge configurations. The labels Q2 and Q1 are used to identify the transistors as well as the transistor logic (1 = on and 0 = off). Since the transistors are always switched in pairs, the complement transistors are labelled Q4 and Q3 accordingly. In order to avoid a short circuit, the complementary leg switches are not switched simultaneously. The switch positions for the three possible states of each phase leg are given in table 2-1.

Table 2-1 Three output states of H-bridges and their current paths

V_o	On switches	Bidirectional current paths	
		$+ip_{ph}$	$-ip_{ph}$
$+V_{dc}$	Q2, Q3	Q2, Q3	D1, D4
0	OR	Q2, D1	Q3, D4
$-V_{dc}$	Q1, Q4	Q1, Q4	D1, D4

The current states for positive and negative phase currents i_{ph} are depicted in table 2-1. In positive "+" and negative "-" states, two diagonally opposite semiconductors (Q2, Q3) or (Q1, Q4) lie within the current path (Either two active switches or two diodes). In the second leg, Q1 is turned off first, followed by the turn-on of Q3 after the dead time. Recovery losses occur in D1 while Q3 experiences turn-on losses. Therefore, each typical H-bridge cell can only produce three distinct voltage levels. It should be noted that each of the switches must block the dc link voltage V_{dc}. The maximum switch/diode current is the maximum phase current $\hat{i}_{ph}$. These parameters determine the basic requirements for rating the main semiconductors.

For accuracy of switching instants, a 2-level-system has the least requirements. The only constraint is that one switch in a branch must have turned off before the second is turned on. In order not to destroy the whole system a defined procedure of switching the 4 devices of a branch in a 3-level system has to be followed. Even more critical is switching in a 5 level system. However, the higher-level systems require less magnetically decoupled transformers.

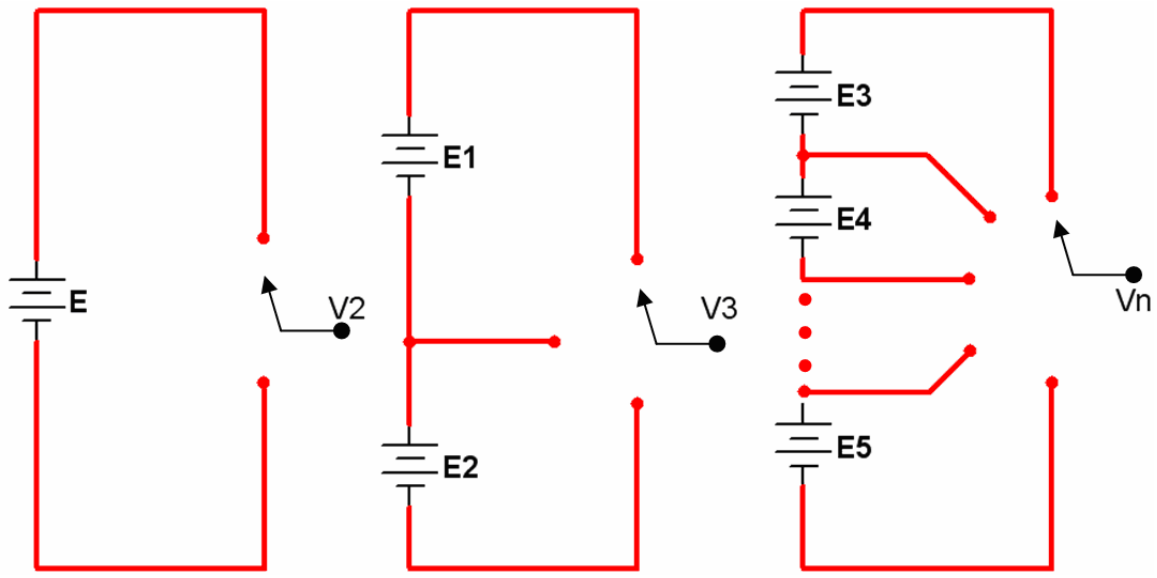


Figure 2-5: Inverter legs a) 2-level inverter, b) 3-level inverter, c) n-level inverter

2.3 Three-Phase Two-Level H-Bridge Topology

2.3.1 Configuration of Circuit

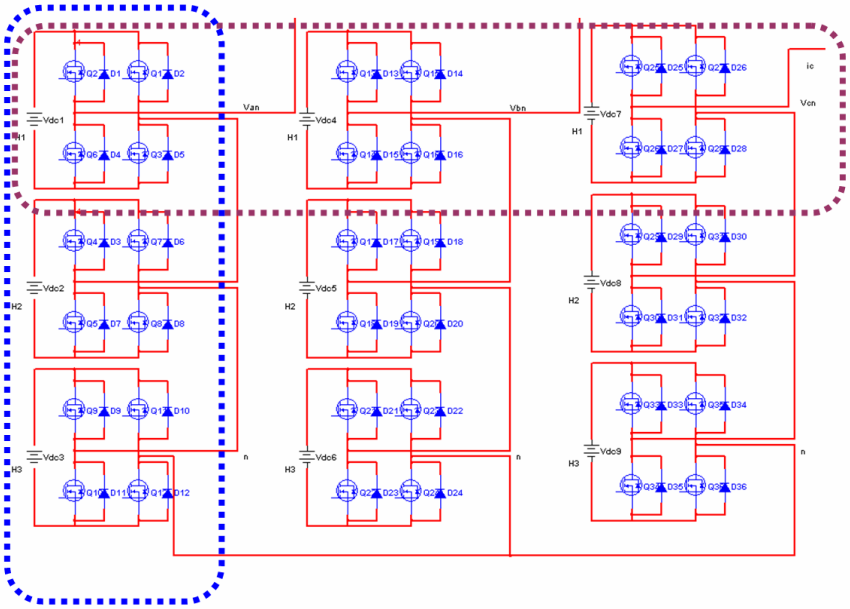


Figure 2-6: Groupings of the legs to highlight the three H-bridges (blue lines) or the two 3-phase inverters (brown lines)

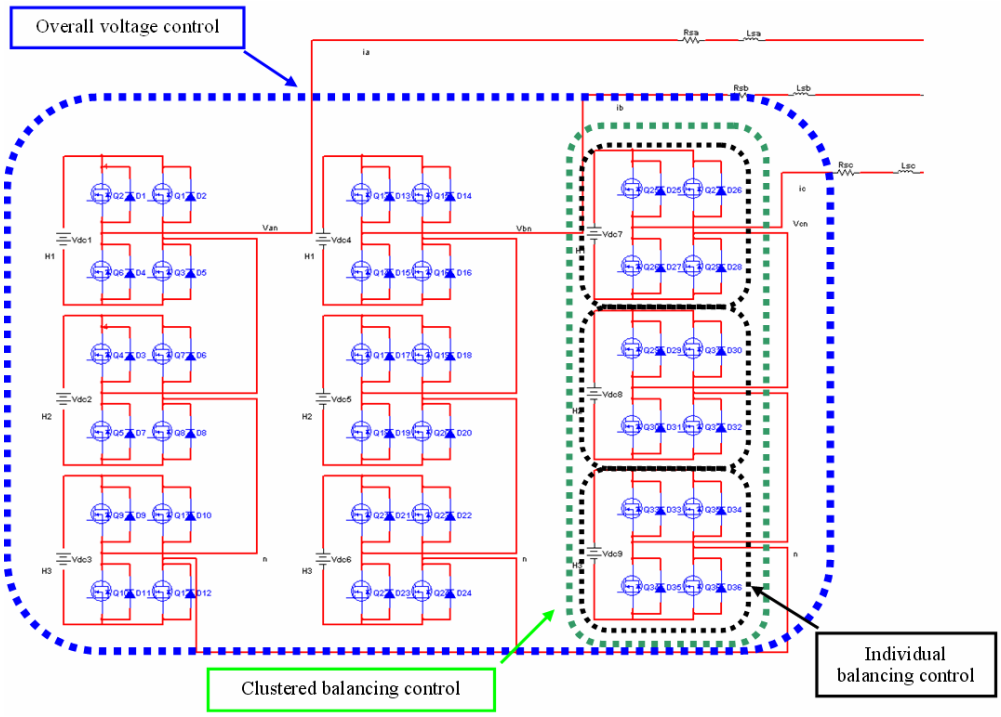


Figure 2-7: A Y-connection, seven-level cascaded converter connected to the power system

Three-phase 2L-H-Bridge, represented in figure 2-7, which was implemented mostly in systems, has separate DC sources [13][42]. The main issue is to balance the voltage of DC busses keeping the power distribution equally.

This class of multi-level converters is based on a series connection of single-phase converters and power conversion cells where the voltage and power level may be easily scaled. Most of the researches on multilevel inverter types are concentrated in diode-clamped, flying capacitor and cascade inverter groups.

Multilevel converters offer a better output power quality of the output waveforms than standard converters. The dc link supply for each H-bridge converter element must be provided separately. The ability to synthesize higher number of output voltage levels with a sufficient harmonic spectrum utilizing power semiconductors and capacitors are important advantages of this topology. However, the large number of power devices and of voltages required to supply each cell with a complex and expensive isolating transformer, as well as control the complexity are drawbacks.

The SC2LHB VSCs will be designated according to the voltage levels of the individual H-bridge cells. The step of the output voltage is comparatively small and equal to the dc bus voltage of H-bridge cell. To attain the rated medium output voltage, all single-phase low-voltage H-bridge cells are connected over the secondary sides of transformers in series, using low-cost low-voltage devices.

Table 2-2 Simulation parameters

Cascade number, N	3
Voltage line-to-neutral	7
Voltage line-to-line	13
DC Voltage	30V
Reference wave frequency, f_m	50Hz
Carrier wave frequency, f_s	4, 8, 10 and 20 kHz
Number of MOSFETs	36

Table 2-2 shows the total required components of two investigated multi-level converters as a function of the number of voltage levels. Although the same number of modules (MOSFETs/diodes) is needed in the considered topologies, the total number of components necessary in these topologies is different at higher voltage levels. In the same voltage range, the NPC requires substantially more components than the others do; therefore, it does not qualify for the use with a high number of voltage levels. Moreover, for more than three-level configuration, the NPC voltage imbalance problem cannot be overcome by utilizing modulation techniques [25][103]. Complex balance circuits would be necessary. This makes the NPC unattractive for levels larger than three.

Table 2-3 Comparison of power component requirements for multi-level topologies

	Series Connected 2-Level H-Bridge (transformers at the input of inverter which is potentially separated with DC input)	**Series Connected 2-Level H-Bridge (transformers at the output of inverter)**
Number of modules (MOSFET/Diode)	6(N-1)	6(N-1)
Number of clamping diodes	0	0
Number of dc link capacitors	3(N-1)/2	3(N-1)/6
Number of balancing capacitors	0	0
Total	15(N-1)/2	15(N-1)/6

Table 2-4 Comparison of 5L SC2LHB-VSC regarding to IGBTs and MOSFETs

	5L SC2LHB-VSC			
	IGBT		MOSFET	
	APOD	NEW	APOD	NEW
	$f_s = 1050Hz$ **m=0.9**	$f_s = 1050Hz$ **m=1**	$f_s = 1050Hz$ **m=0.9**	$f_s = 1050Hz$ **m=1**
	%	%	%	%
V_{phase}	18.74	10.05	55.51	10.37
$V_{line-to-line}$	17.06	8.27	40.96	8.29

As shown in table 2-4 the comparison indicates that new method has better voltage outputs due to lower switching algorithm for a single-phase load.

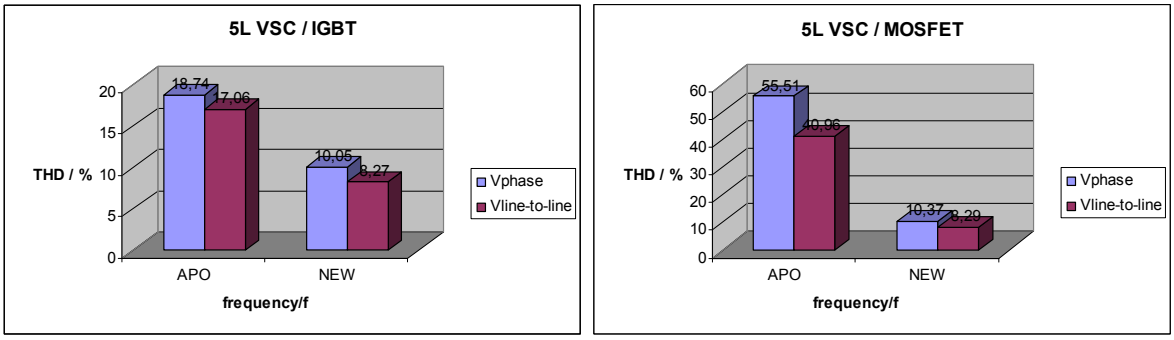


Figure 2-8: THD comparison of 5L VSC (IGBT) and 5L VSC (MOSFET)

In figure 2-8, THD of V_{phase} and $V_{line-to-line}$ shows a great difference between APOD method and our approach which has been simulated for IGBT and MOSFET configurations.

3 Main New Contribution

A designer implements the application following a certain trajectory of design levels in a top-down approach, i.e. from algorithm level to circuit level, which can be defined as design flow [11][109][112][123]. Each design level includes large collection of low power techniques which may result into a significant reduction of the power consumption [64][77][90].

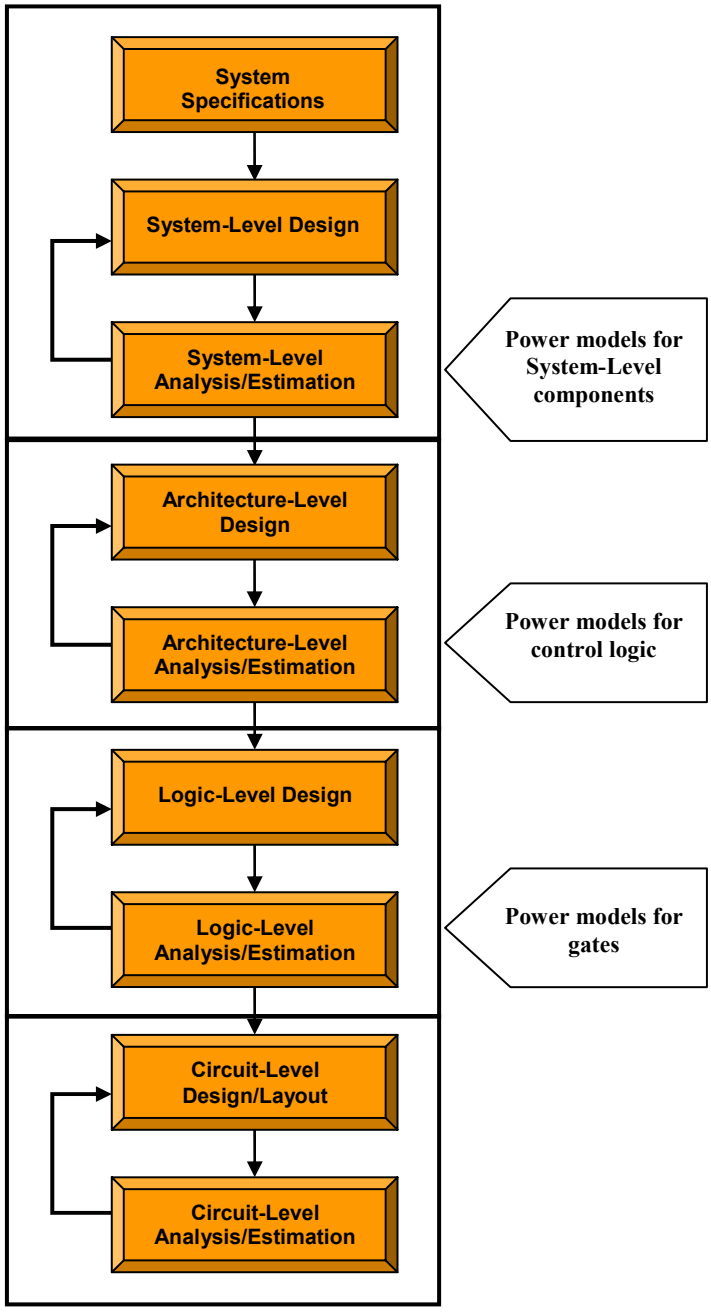


Figure 3-1: Design flow with power analysis/estimation steps [2][35]

Actually, this issue is an open research topic, strongly-depended on the application requirements [106]. The designer specifies the starting and final design level of a design

procedure, which may be a subset of a general top-down approach and therefore the use of optimization low power techniques and the estimation of the power loss must be performed [96]. To fully manage and optimize power consumption, a design flow must address power consumption issues at each stage of the design process and at each level of design abstraction. A top-down approach is illustrated in figure 3-1, which summarises the flow of steps that are required to go from a system-level specification to circuit level analysis.

As we have seen, the design for low power starts with a target specification, selecting the right algorithm and optimizing the behavioural description of the algorithm using transformation. If that description meets the specification we transform the behavioural description into a structural implementation.

3.1 Quasi-Eight-Level Inverter

The actual system will be composed of inverters which run at the same DC-link voltage and should include same type of switches for standardization purposes. We select a simple control set based on the standard triangle wave-sinusoidal reference comparison to get switching states. Alternate Phase Opposition Disposition (APODPWM) technique is employed in simulation phase to control the switching devices of the first voltage-source inverter and as well as for the rest of the inverters.

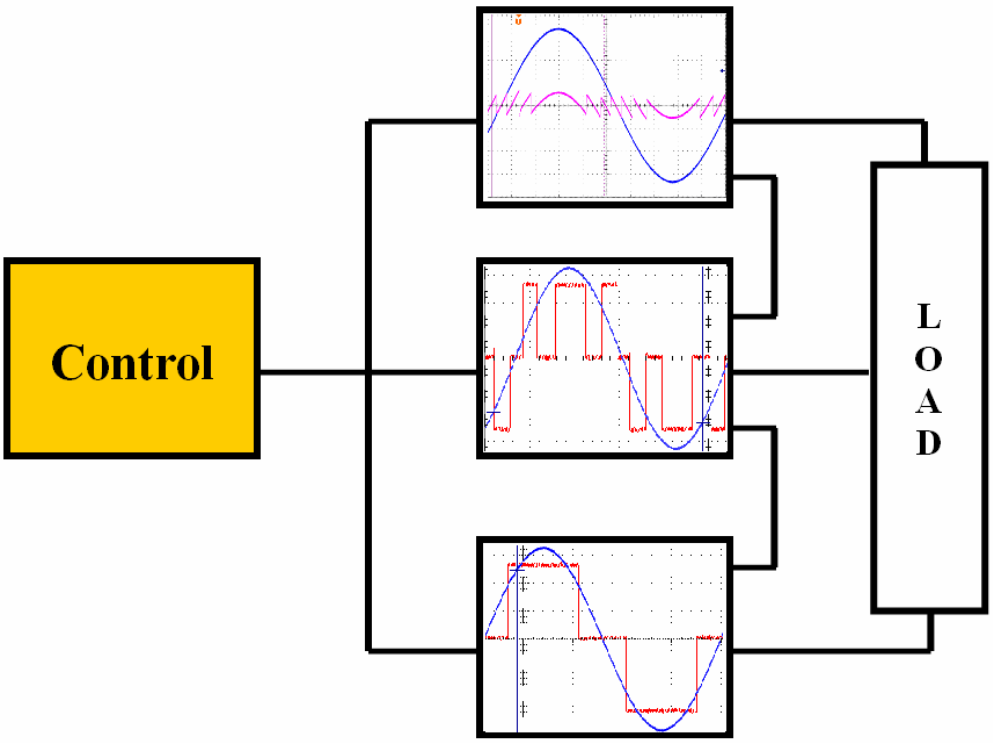


Figure 3-2: Control the separated inverters

For the proposed harmonic reduction technique, the theoretical analysis of 1-2-4 stepped voltage inverter is presented. By using a systematic method, only the polarities and the number of levels are required to be determined for different modulation levels [32][78]. Computer simulation results are provided. To verify the theory and the simulation results, a

cascade inverter based hardware prototype including a low cost 8-bit microcontroller and modularized power stage and gate driver circuits, is implemented. Experimental results indicate that the proposed technique is effective for harmonic reduction in multilevel converters, and that both theoretical and simulation results are well validated.

In a power stage, four MOSFET, SPP20N60C3 model, are used as the main switches, which are connected in full-bridge configuration. After the test on the reduced scale converter, some test benches were implemented. The SPWM and the power sharing capability were tested. Computer simulation results are provided in chapter 6.

A single-phase H-bridge inverter, as shown in figure 3-3, supplies a resistance from a DC source [36][37]. Inverter 1 has power transfer value S_0. Therefore, inverter 2 shall have double that power transfer value, i.e. $2*S_0$. As a rule of thumb, a standard design for industrial systems exhibits switching losses in controlled semiconductors being equal on-state losses.

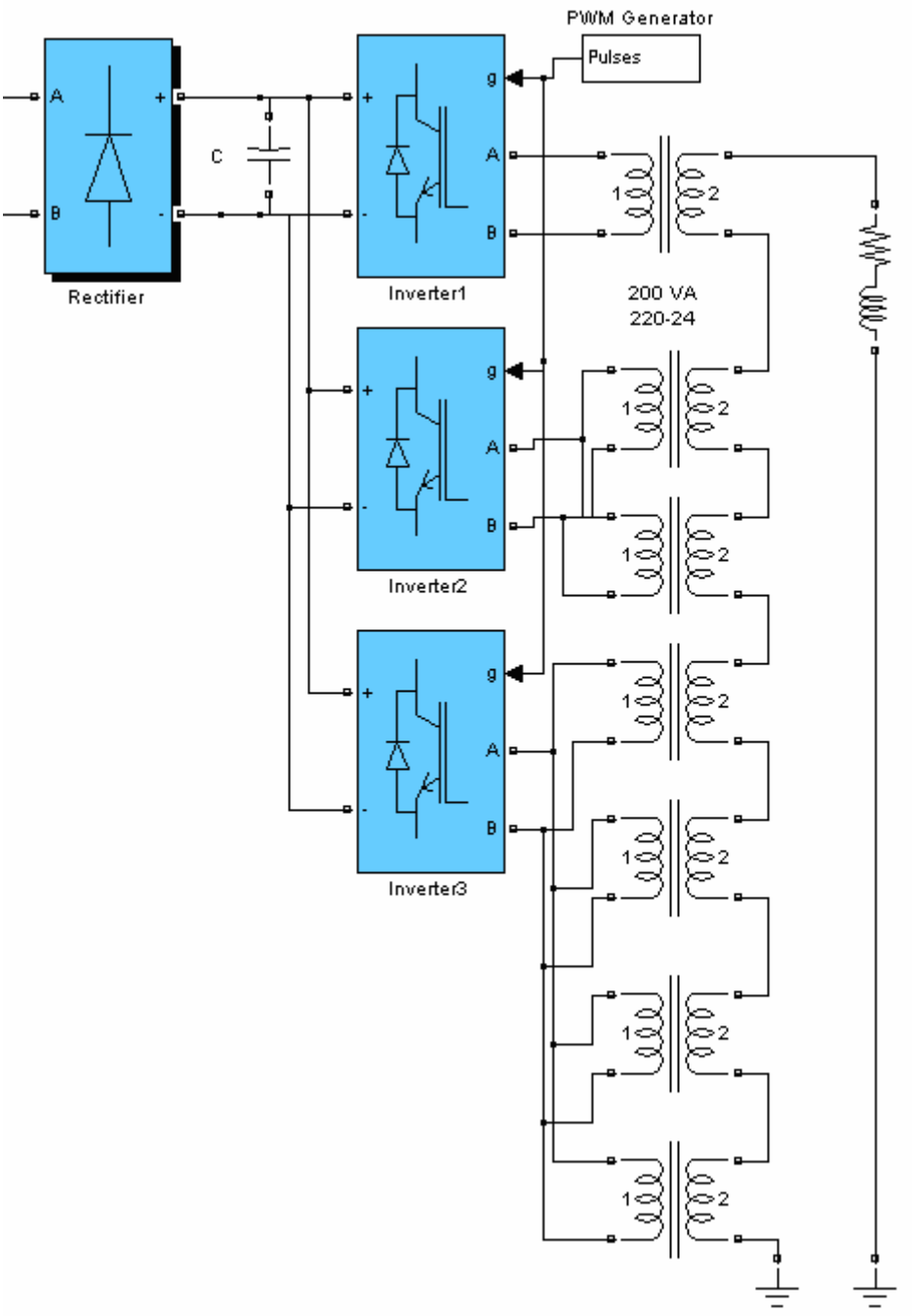


Figure 3-3: Laboratory model hardware layout

For a really good output voltage quality, we will choose a slightly higher frequency than this. Then we can estimate that inverter 2 can be exactly the same device as inverter 1. Inverter 2 runs at 3 times the fundamental frequency and the corresponding switching losses practically can be neglected for IGBT and MOSFET devices of intended power ranges whereas inverter 3 runs with the fundamental frequency. This allows about 2 times current capability which yields the demanded value of $2*S_0$ for inverter 2. The whole system requires 3 identical 2-level standard single-phase inverters only.

For practical evaluation of total system we establish a laboratory model. For cost reasons, we also integrate used components as transformers. We have 7 identical transformers organized in parallel groups of 1, 2, and 4. We also use 7 identical inverters implementing MOSFET switches for the laboratory model.

This doctoral thesis includes discussions and research assignments of system design, describes the development of a stand-alone wind turbine. Various possible configurations are investigated and a configuration using a multi-level inverter is chosen. A model is developed for controller design of the fast controllers of the system and a prototype is built for testing. The documents the performance of the prototype through measurements done on a prototype installed in a test facility where it has been tested both as a standalone unit and in parallel with battery test equipment are reported. For system wide power quality assessment and controller design a dynamic performance assessment model has been developed. As a case study, specific large wind turbine is used, and the concept is applicable for any type of wind turbine.

3.2 Comparison to Conventional Systems

Our new contribution has advantages compared to other standard multilevel inverter topologies. Common inverter approaches have isolation transformers with delta, star, or zigzag winding connections. The most complex part is to determine the needed parameters such as inductance and resistance values of each transformer. In this thesis, all the inverters are fed by a common DC bus. The transformers are located at the output side of the inverters which the primary sides are connected to each inverter in parallel and the secondary sides are connected in series. Grouping of these seven transformers as 1, 2 and 4, total 7 voltage levels can be produced. Referring to sinus voltage, each group of transformer acts differently in one period. Therefore, switching states of these three groups of transformers determine the total harmonic distortion and losses of the inverters. Switching frequencies between 4 kHz…20 kHz, are the main operation area of the MOSFETs inverter and experimental results show better output voltage with the increasing frequencies.

These advantages prevent filter implementation which is usually a common solution and also decrease the costs in such kind of systems.

4 Modelling of Quasi-Eight-Level Inverter

The circuit of figure 4-1 shows the basic topology of an H-bridge converter used for the implementation of SC2LHB VSCs. It is based on the simple, four switches converter, which is usually used for single-phase applications. A three-phase diode rectifier charges the dc capacitor and the dc voltage feeds a single-phase MOSFET bridge, which generates the PWM output of the power cell. In order to simplify the system and yet yield high output voltage quality without excessive individually operated switches and without extensive filtering we propose the quasi-8-level converter circuitry including the adapted output transformer that was shown in chapter three.

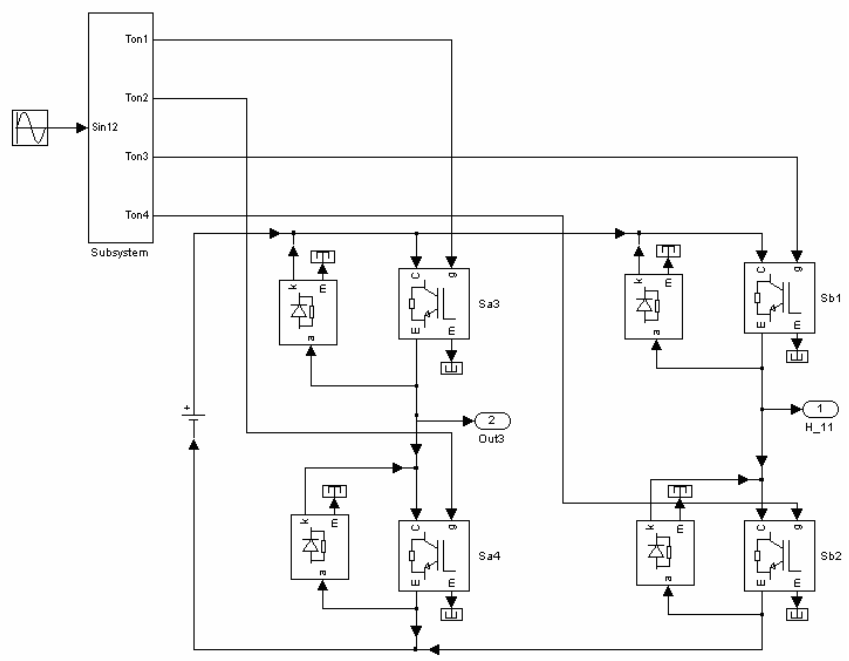


Figure 4-1: Typical power cell (H-bridge) converter

The parameters used in simulation for H-bridge converter are as follows and detailed configuration can be seen in appendix A.

Table 4-1 Simulation parameters

DC Voltage, E	30V
Modulation index, M_a	0.9
Reference wave frequency, f_m	50 Hz
Carrier wave frequency, f_s	4, 8, 10 and 20 kHz
Snubber resistance, R_s	100Ω
Snubber capacity, C_s	$220nF$
Load resistance, R	15Ω

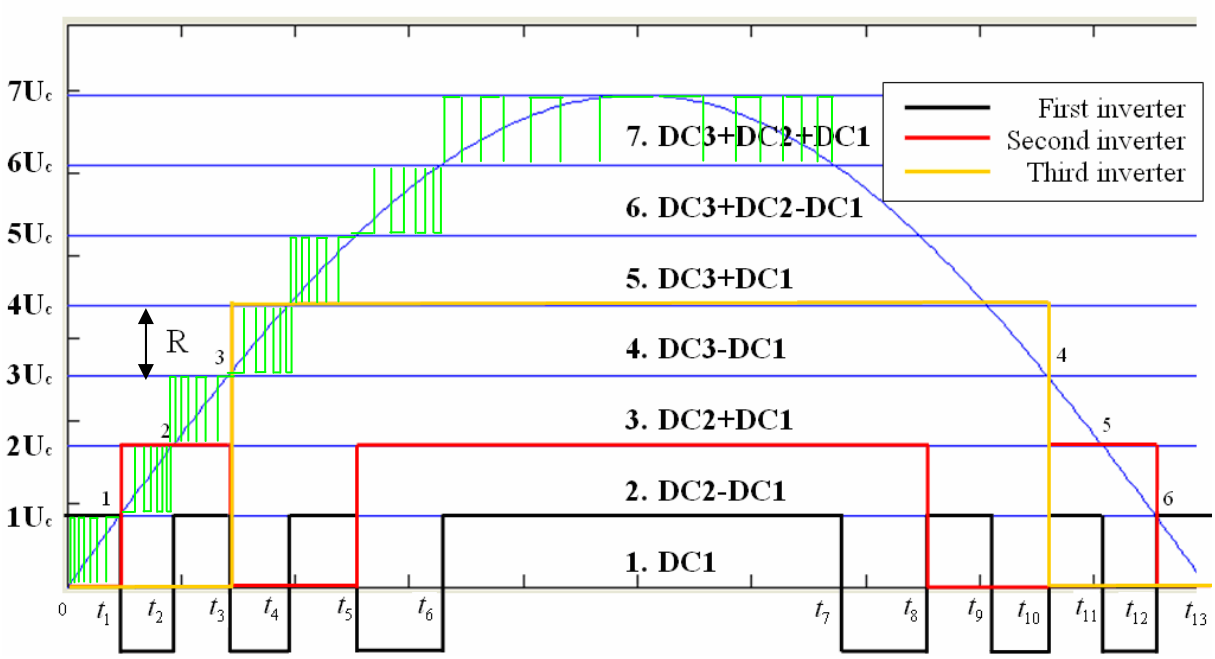


Figure 4-2: Quasi eight-level inverter and output-voltage generation

Figure 4-2 shows a half period of one cycling. The first inverter which is being controlled as PWM method helps as an auxiliary converter partially switches in "+" or "-" direction in order to produce stepped level voltages. The second and third inverters are the main blocks of the sinusoid signal and therefore are switched on or off extremely rarely compared to the first inverter. By this way, conduction and switching losses can be reduced.

Table 4-2 Switching conditions of each inverter

	1. Inverter (in PWM mode)	2. Inverter	3. Inverter
$0 < t < t_1$	+1	0	0
$t_1 < t < t_2$	-1	+1	0
$t_2 < t < t_3$	+1	+1	0
$t_3 < t < t_4$	-1	0	+1
$t_4 < t < t_5$	+1	0	+1
$t_5 < t < t_6$	-1	+1	+1
$t_6 < t < t_7$	+1	+1	+1
$t_7 < t < t_8$	-1	+1	+1
$t_8 < t < t_9$	+1	0	+1
$t_9 < t < t_{10}$	-1	0	+1
$t_{10} < t < t_{11}$	+1	+1	0
$t_{11} < t < t_{12}$	-1	+1	0
$t_{12} < t < t_{13}$	+1	0	0

where “+1” denotes the upper direction, “-1” the reverse direction and “0” the no switching mode. To perform the above rules, the digital controller employs a flowchart. The digital controller takes the voltage samples and compares them with constant DC references. Then, the region of input voltage, *R*, is updated, the control algorithm is performed, and the appropriate switching functions are determined. The switching functions are applied to the H-bridge cells and the corresponding operating modes are selected by the multiplexers. This procedure is repeated in the next sampling periods.

The following remarks about this method should be noted:
• In the proposed controller, there are two modulation mechanisms. One is generated by the analogue controller, termed as PWM mode, and the other is done by the digital controller, termed as low switching voltage algorithm.
• During each sampling period, the switching functions do not change.

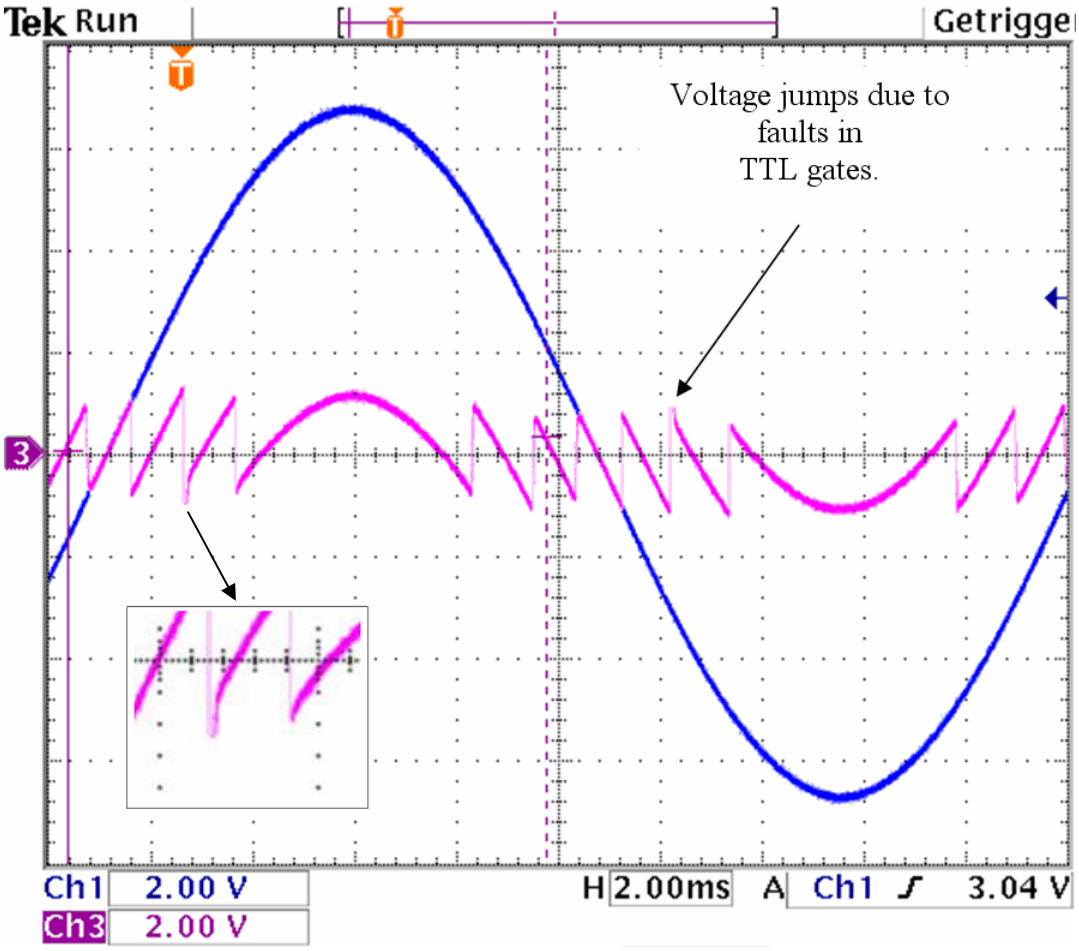
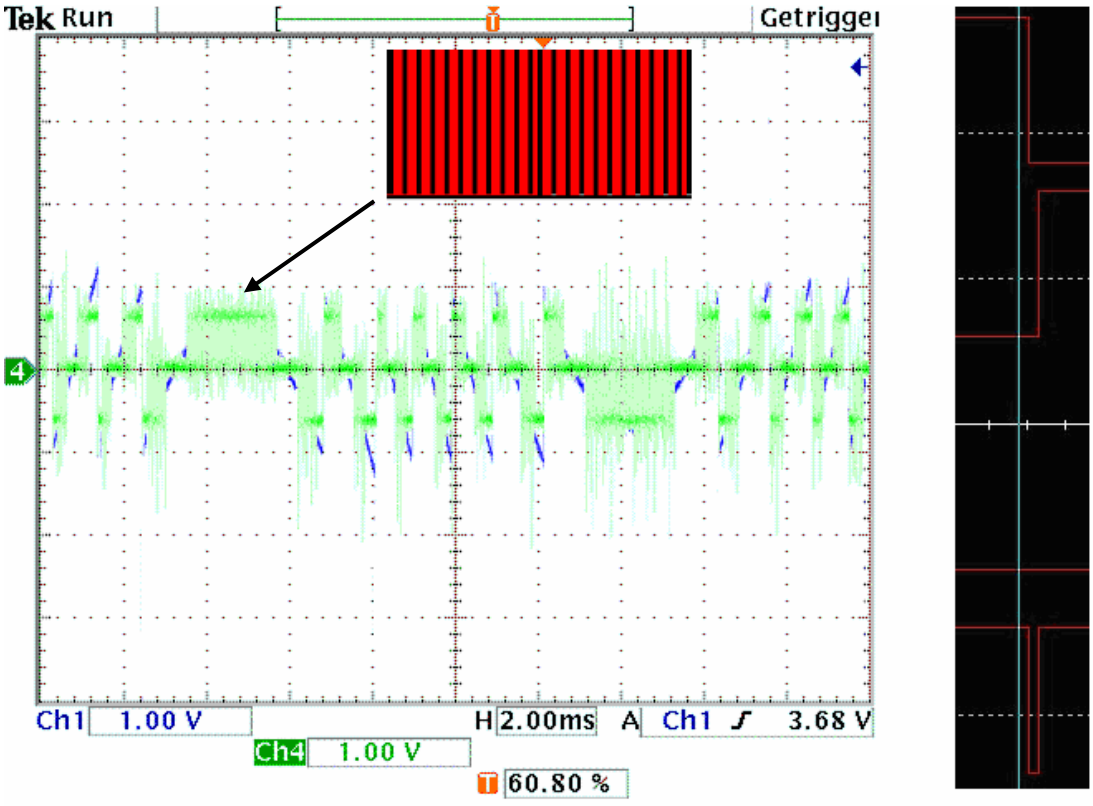


Figure 4-3: PWM controlled signal (pink)

In figure 4-3, pink-coloured signal is gained from the reference sinus signal for PWM control and is compared with carrier waveforms. As seen in figure 4-4 (b), there is time interval between the gates. Logic gates operate in nanoseconds (20 ns), and each TTL gate needs time interval in order to switch on or off. This problem causes delays and voltage fluctuations.



(a) (b)

Figure 4-4: (a) PWM output signals of the first inverter (b) Output of TTL gates

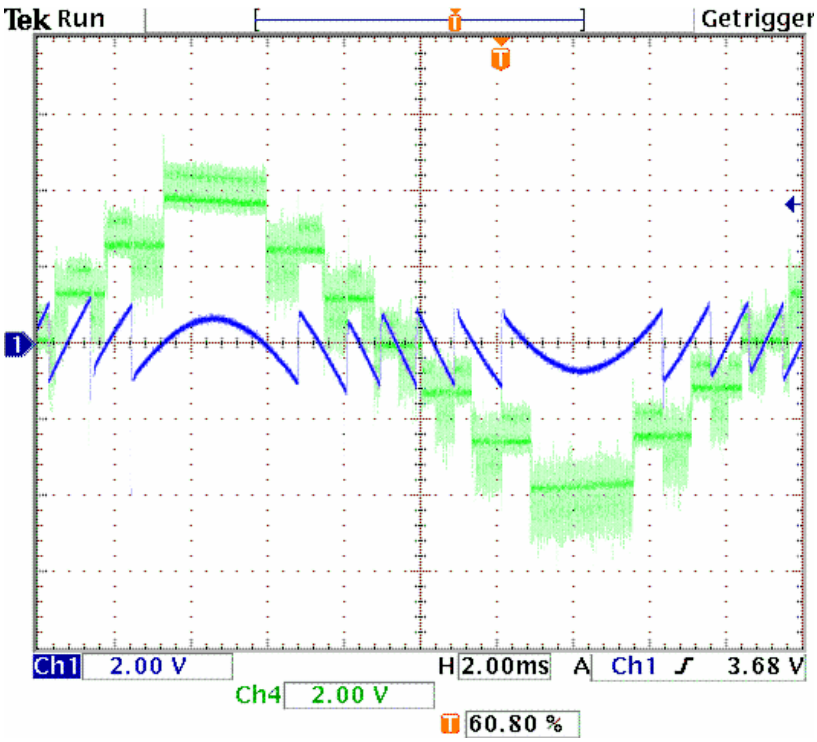


Figure 4-5: Output signal of the inverter

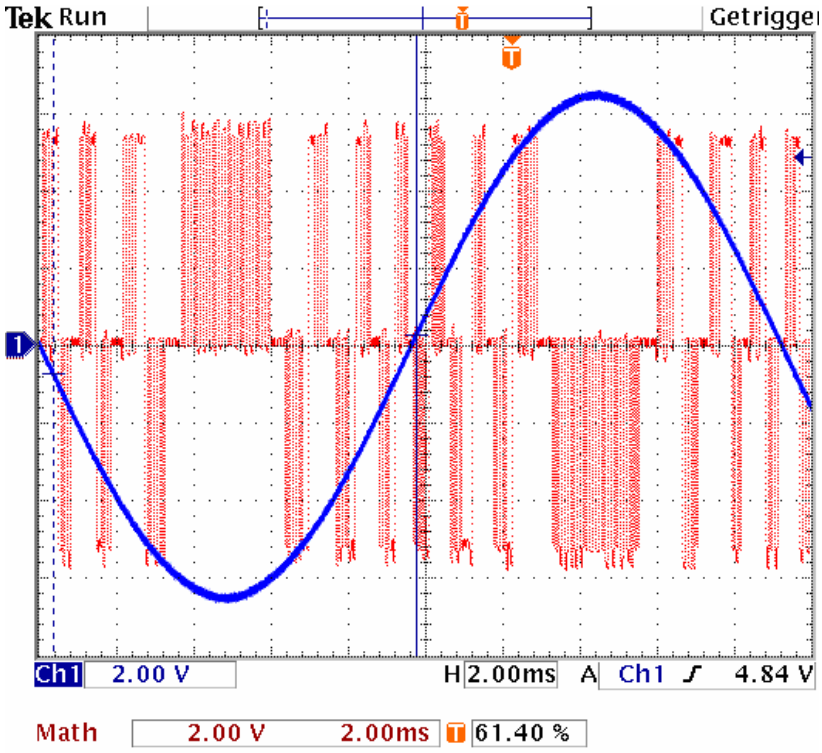


Figure 4-6: PWM signals of the first inverter

Only first inverter cell is modulated by a sine-triangle modulation as shown in figure 4-5. Practically, these signals are then modulated with sinusoid signal which is shown in figure 4-6 (blue line).

4.1 Modulation Method

4.1.1 Sine-Triangle Modulation

One first impression of a multilevel power converter is that the large number of switches may lead to complex pulse-width modulation (PWM) switching algorithms and requires many driving circuits [19][20]. However, early developments in this area demonstrated the relatively straightforward nature of multilevel PWM [22]. The purpose of PWM single-phase converter is to shape and to control the single-phase output voltage in magnitude and frequency with a practically constant input voltage U_{dc} [31]. To obtain single-phase output voltage in a single-phase PWM, the same triangular voltage waveform U_{C1} and U_{C2} are compared with control voltage waveform $(U_{\sin})$.

The frequency modulation ratio m_f and the amplitude modulation ratio M_a of a PWM are defined as

$$m_f = \frac{f_C}{f_m} \tag{4-1}$$

In order to eliminate even harmonics, the frequency modulation ratio m_f should be odd. The odd harmonics in the phase-midpoint voltages are the same as the output of any one of the legs, centred on the switching frequency and its multiples (m_f, $2m_f$ ...).

$$M_a = \frac{U_R}{U_{C_{1,2}}} \tag{4-2}$$

where U_R denotes the peak value of the fundamental component of the reference voltage. For a sine-triangle modulation of three-phase inverter the linear modulation range is limited to values of

$$0 \leq M_a \leq \frac{2}{\sqrt{3}} \tag{4-3}$$

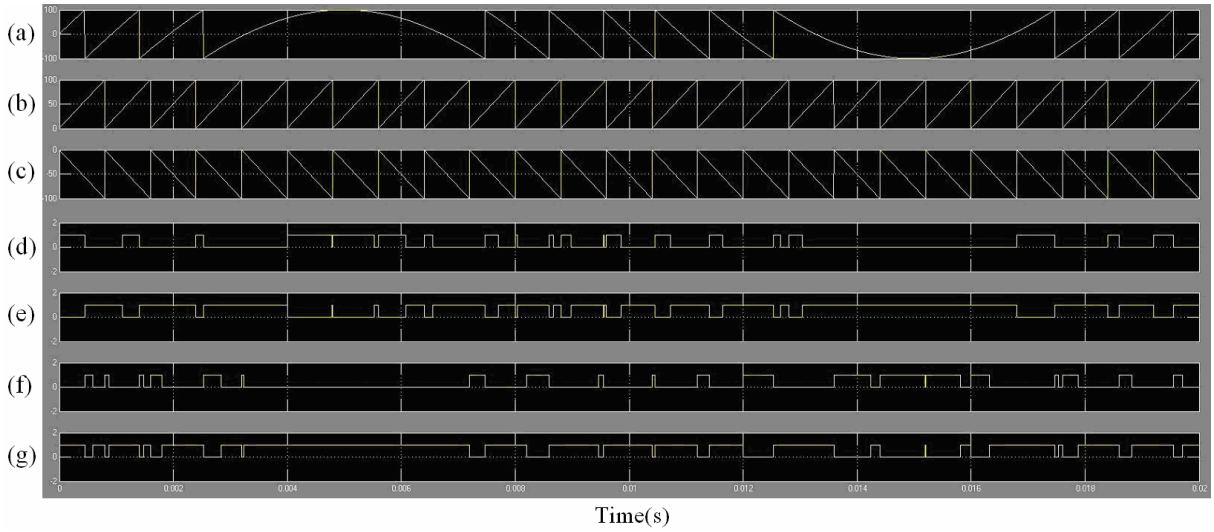


Figure 4-7: PWM control of proposed inverter (first inverter) (a) sinusoidal signal, (b) upper triangular signal, *Uc1* (c) lower triangular signal, *Uc2* (d) positive portion of *Ton,1*, (e) negative portion of *Ton,2* inverted, (f) positive portion of *Ton,3*, (g) negative portion of *Ton,4* inverted

In order to generate the switching signals, two triangular voltage waveforms U_{C1} and U_{C2}, as shown in figure 4-7, are determined by the comparison of the corresponding carrier signal and the reference signal U_R. Thus, there are four commutations during one period of the carrier signal. As shown in figure 4-8, the comparison of U_R with U_{c1} and U_{c2} results in the following logic signals to control the switches in the first leg.

$$U_{an} = \begin{cases} U_{dc} & where U_R > U_{c1}\ (Q_2, Q_3 : ON, Q_1, Q_4 : OFF) \\ 0 & where U_R < U_{c1}\ (Q_1, Q_2 : OFF, Q_3, Q_4 : ON) \end{cases} \tag{4-4}$$

For controlling the second leg switches, U_{C2} is compared with the same control signal, which yields following

$$U_{an} = \begin{cases} 0 & where U_R > U_{c2}\ (Q_1, Q_2 : OFF, Q_3, Q_4 : ON) \\ (-U_{dc}) & where U_R < U_{c2}\ (Q_1, Q_4 : ON, Q_2, Q_3 : OFF) \end{cases} \quad (4\text{-}5)$$

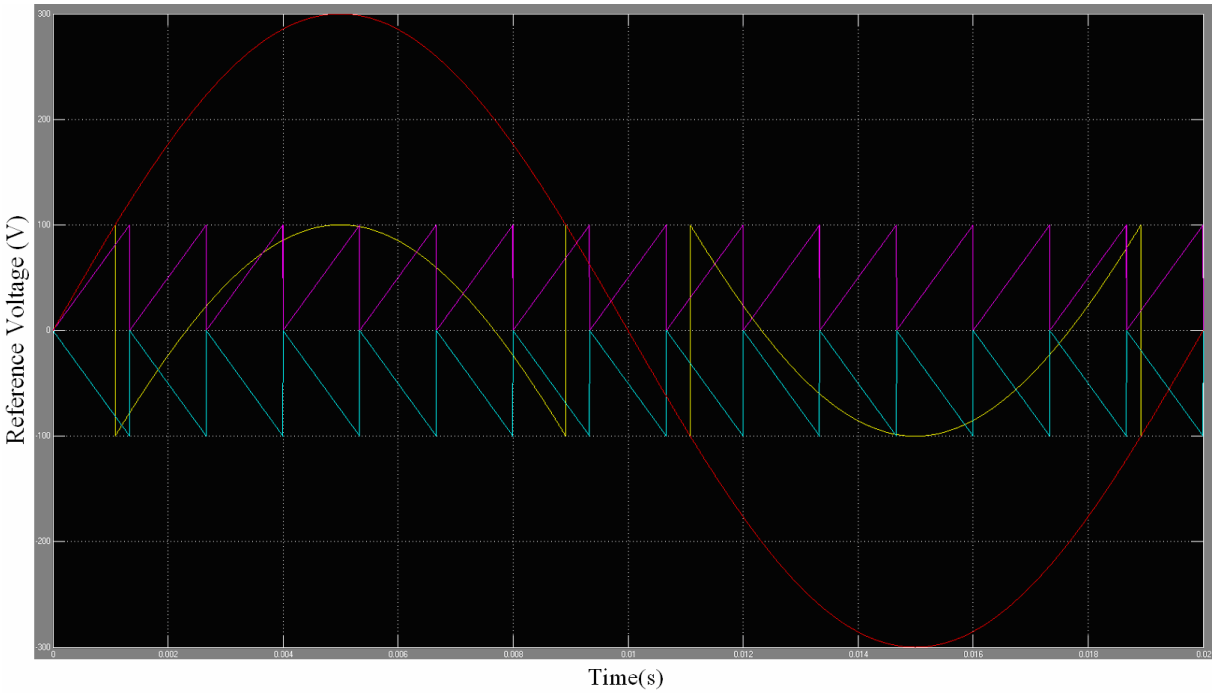


Figure 4-8: PWM control of the first inverter (sine-triangle intersection)

Yellow line shows the signal that will be pulse modulated using PC849 high density mounting type photo coupler. This signal is the subtraction of signals from reference input which are currents derived from a constant 12V DC supply over $1\,k\Omega$, $3\ k\Omega$ and $6\ k\Omega$ resistances. Comparing the reference signals with sinusoid, the PC849 photo couplers switches ON or OFF and by the way the necessary current signals are derived and provided to TL084ACD.

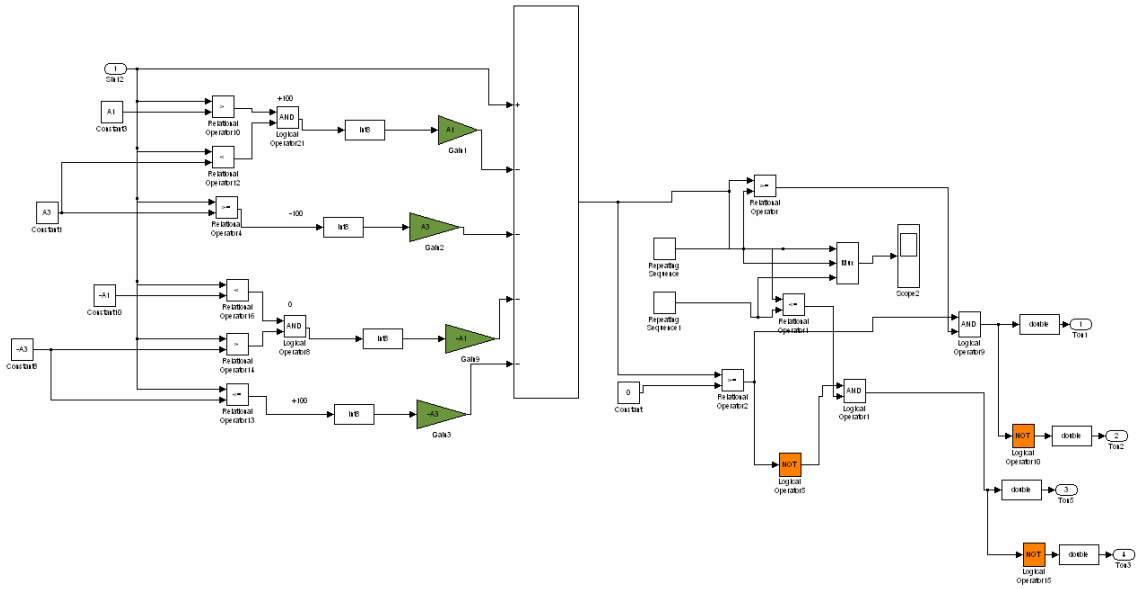


Figure 4-9: Logic circuit of the third inverter

Each reference voltage is compared with sinusoidal signal and the states of the MOSFET gates are determined. Depending on the signal value, the reference voltage is compared with triangular carriers at each time.

Table 4-3 Logic map of the PWM signals

(0)	(+)	(-)
(A▼C)▲B	┐	(A▼C)▲B
(A▼C)▼B	┐	(A▼C)▼B
(A▼B)▲C	(A▼B)▲C	┐(A▼B)▲C
(A▼B)▼C	(A▼B)▼C	┐(A▼B)▼C

where "▼" denotes "OR", "▲"denotes "AND" and "┐"denotes "NOT". The logical outputs are determined with the changing states and drive the inverter correctly. "A", "B" and "C" are the output signals for computing the (+), (-) and (0) states.

Table 4-4 States of each MOSFETs of the PWM signals

B	**Q2** ON	**Q1** OFF
Plus(+)	**Q4** OFF	**Q3** ON
A	**Q2** OFF	**Q1** OFF
Zero (0)	**Q4** ON	**Q3** ON
C	**Q2** OFF	**Q1** ON
Negative (-)	**Q4** ON	**Q3** OFF

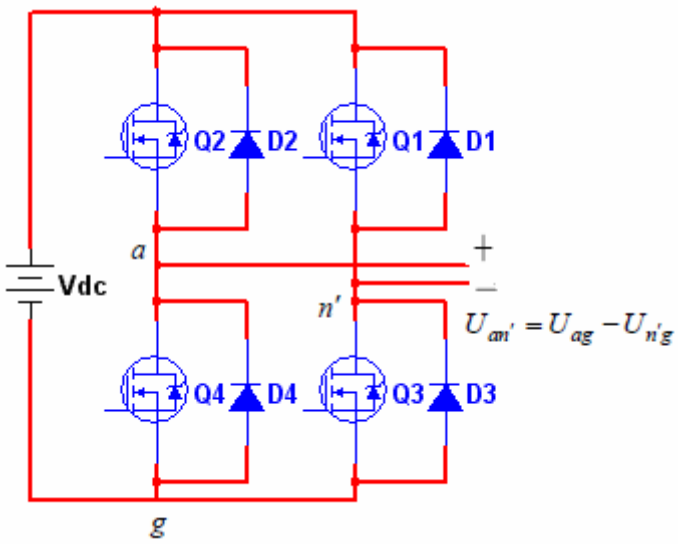


Figure 4-10: Typical power cell (H-bridge) converter

The use of PWM voltage switching causes a smaller ripple on the dc current side [53]. We notice that when both the lower or upper switches are "ON", the output voltage is zero. The output current circulates in a loop through (Q2, *D1*) or (*D2, Q1*), depending on the direction of i_{ph}. During this interval, the current i_{dc} is zero. A similar condition occurs when both bottom switches Q4 and Q3 are turned on.

Because of the diodes in anti-parallel with the switches, the foregoing voltage is independent of the direction of the output current i_{ph}. Two legs of the H-bridge are controlled separately, the first carrier band harmonics of the output voltage occur at twice the corresponding carrier frequency ($f_{1Cb} = 2f_C$) [39]. This advantage appears in the harmonic spectrum of the output voltage waveform, as shown in figure 4-25. If we choose the frequency modulation ratio m_f to be even, the output voltage waveforms of any one of the legs U_{ag} and $U_{n'g}$ are displaced

by 180° of the fundamental frequency, with respect to each other. Therefore, the harmonic components at the switching frequency in any one of the legs have the same phase, since the output voltage waveforms are 180° displaced and m_f is assumed to be even. This results in the cancellation of the harmonic component at the sidebands of the switching frequency in the output voltage.

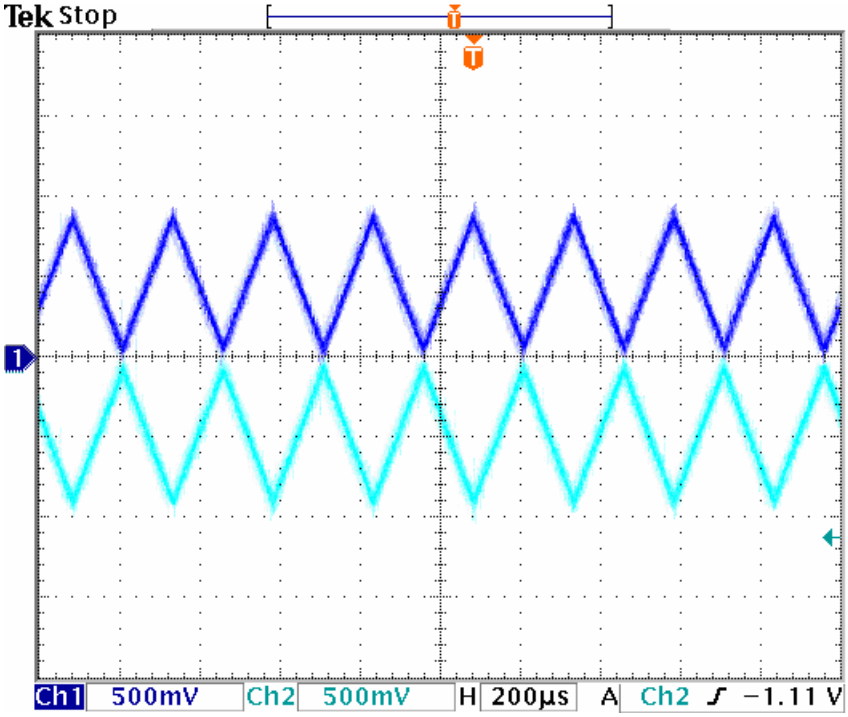


Figure 4-11: Carrier triangular waves

This PWM method uses two carrier signals of the same amplitude and frequency, which are inversed referring to point "0" with respect to each other which is another way to achieve multilevel modulation, one associated to the upper leg and another one associated to the lower leg. Figure 4-11 shows how two carriers are disposed. The upper leg carrier is a triangular wave sweeping from 0 to 1, while the lower leg carrier goes from 0 to -1. Setting the function generator V_{p-p}=0.75 V and $V_{off-set}$=0.37 V, the amplitude of signals are adjusted to 1V and -1V having different modulation index values (m_a). In this way, only one leg commutates at one time and the total output is given by the overall effects of both legs. With the representation of figure 4-11, the output is obtained as the sum of the single leg outputs, so the gating signals of the lower leg must be neglected to achieve which is still valid.

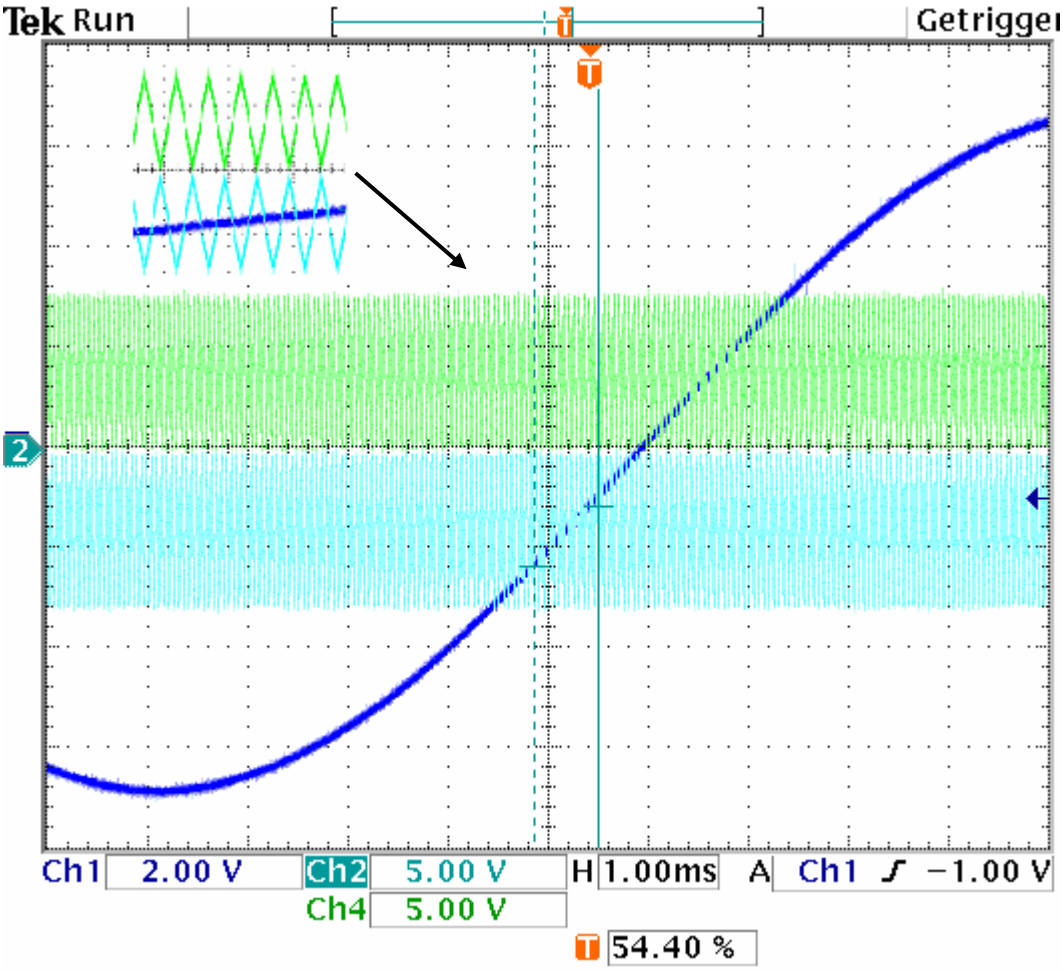


Figure 4-12: Carrier triangular waves with respect to reference sinus signal

The switching points are determined by the intersection of the triangular carrier wave U_{c1} and U_{c2} which were controlled with different frequencies and amplitude and the reference modulation sine wave, f_0 shown in figure 4-12. The output frequency is at the sine-wave frequency f_0 and the output voltage is proportional to the magnitude of the sine wave.

Table 4-5 explains basic switching strategy to develop the seven steps yielding 8 levels (including level 0). The push-pull configuration again yields 7 positive steps and 7 negative steps. In a given band of voltage we use certain output voltages of defined inverters and add these voltages at defined transfer ratio of transformer over the series connection of output side windings.

The total number of switch states for the 8L-SC2LHB VSC is 36, and the voltage steps are 15 which breaks down to seven for the positive voltage, seven for the negative voltage, and one for the zero voltage.

Table 4-5 Quasi eight-level VSC switching states

	Module1			Module2			Module3		
	T_{on1}	T_{on2}	Vdc	T_{on1}	T_{on2}	Vdc	T_{on1}	T_{on2}	Vdc
$Inv_3 + Inv_2 + Inv_1$	1	0	**Vdc**	1	0	**Vdc**	1	0	**Vdc**
$Inv_3 + Inv_2 - Inv_1$	0	1	**-Vdc**	1	0	**Vdc**	1	0	**Vdc**
$Inv_3 + Inv_1$	1	0	**Vdc**	1	1	**0**	1	0	**Vdc**
$Inv_3 + Inv_1$	1	0	**Vdc**	0	0	**0**	1	0	**Vdc**
$Inv_3 - Inv_1$	0	1	**-Vdc**	1	1	**0**	1	0	**Vdc**
Inv_3 -v INV_1	0	1	**-Vdc**	0	0	**0**	1	0	**Vdc**
$Inv_2 + Inv_1$	1	0	**Vdc**	1	0	**Vdc**	1	1	**0**
$Inv_2 + Inv_1$	1	0	**Vdc**	1	0	**Vdc**	0	0	**0**
$Inv_2 - Inv_1$	0	1	**-Vdc**	1	0	**Vdc**	0	0	**0**
$Inv_2 - Inv_1$	0	1	**-Vdc**	1	0	**Vdc**	1	1	**0**
Inv_1	1	0	**Vdc**	0	0	**0**	0	0	**0**
Inv_1	1	0	**Vdc**	0	0	**0**	1	1	**0**
Inv_1	1	0	**Vdc**	1	1	**0**	0	0	**0**
Inv_1	1	0	**Vdc**	1	1	**0**	1	1	**0**
0	0	0	**0**	0	0	**0**	0	0	**0**
0	0	0	**0**	0	0	**0**	1	1	**0**
0	0	0	**0**	1	1	**0**	0	0	**0**
0	0	0	**0**	1	1	**0**	1	1	**0**
0	1	1	**0**	0	0	**0**	0	0	**0**
0	1	1	**0**	0	0	**0**	1	1	**0**
0	1	1	**0**	1	1	**0**	0	0	**0**
0	1	1	**0**	1	1	**0**	1	1	**0**
Inv_1	0	1	**-Vdc**	1	1	**0**	1	1	**0**
Inv_1	0	1	**-Vdc**	1	1	**0**	0	0	**0**
Inv_1	0	1	**-Vdc**	0	0	**0**	1	1	**0**
Inv_1	0	1	**-Vdc**	0	0	**0**	0	0	**0**
$Inv_2 - Inv_1$	1	0	**Vdc**	0	1	**-Vdc**	1	1	**0**
$Inv_2 - Inv_1$	1	0	**Vdc**	0	1	**-Vdc**	0	0	**0**
$Inv_2 + Inv_1$	0	1	**-Vdc**	0	1	**-Vdc**	0	0	**0**
$Inv_2 + Inv_1$	0	1	**-Vdc**	0	1	**-Vdc**	1	1	**0**
$Inv_3 - Inv_1$	1	0	**Vdc**	0	0	**0**	0	1	**-Vdc**
$Inv_3 - Inv_1$	1	0	**Vdc**	1	1	**0**	0	1	**-Vdc**
$Inv_3 + Inv_1$	0	1	**-Vdc**	0	0	**0**	0	1	**-Vdc**
$Inv_3 + Inv_1$	0	1	**-Vdc**	1	1	**0**	0	1	**-Vdc**
$Inv_3 + Inv_2 - Inv_1$	1	0	**Vdc**	0	1	**-Vdc**	0	1	**-Vdc**
$Inv_3 + Inv_2 + Inv_1$	0	1	**-Vdc**	0	1	**-Vdc**	0	1	**-Vdc**

To take advantage of both low frequency (stepped modulation) and high frequency (PWM) modulation techniques, we employ the both modulation method as shown in figure 4-13. In this method, the input voltage U_x is divided into equal sections with the scale of U_c (U_c is the reference of DC-link voltages). Now we define the voltage region *K* as follows:

$$\text{Region K}: \ (\text{K}-1)U_c < U_x < \text{K}\,U_c, \ \text{K} = 1,...,\text{N}$$

Region K is the voltage interval that the magnitude of input voltage, $|U_x|$, lies between $(\text{K}-1)U_c$ and $\text{K}\,U_c$. Note that the minimum number of cells to synthesize the multilevel waveform, U_{an} is equal to the closest integer greater than (U_m / U_c), where U_m is the peak input voltage.

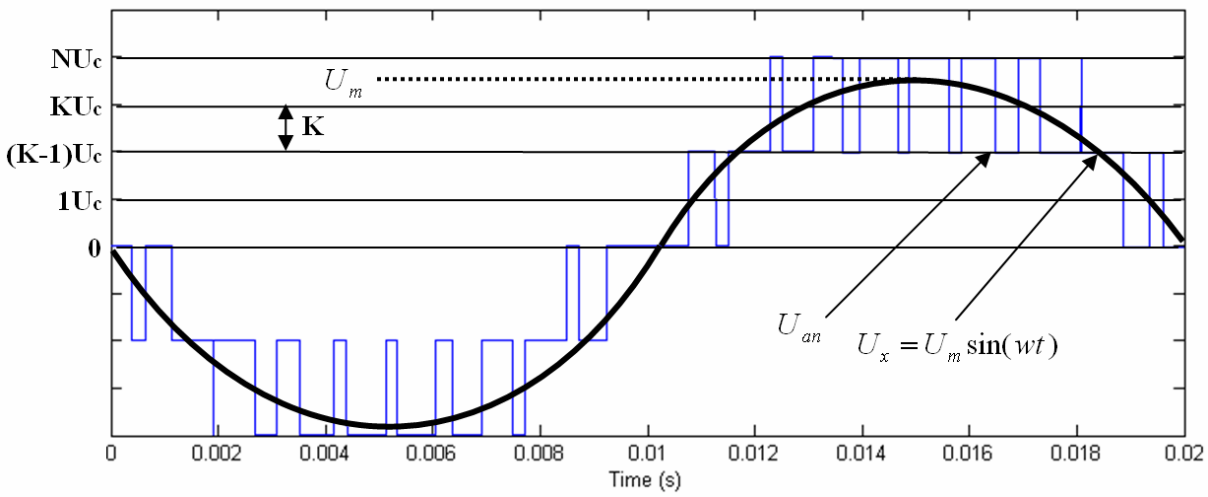


Figure 4-13: Definition of voltage regions for $\text{K} = 1,...,\text{N}$

4.1.2 Discrete Implementation

It will be seen that the discrete method presented herein relies on computation directly from the duty cycles and therefore it is not necessary to define triangle waveforms or voltage vectors. For this reason, it is preferred to use microprocessors for the second and third inverter control algorithm while sine-triangle modulation is useful in that it can provide a straightforward method of describing multilevel modulation for the first inverter.

4.1.3 First Inverter

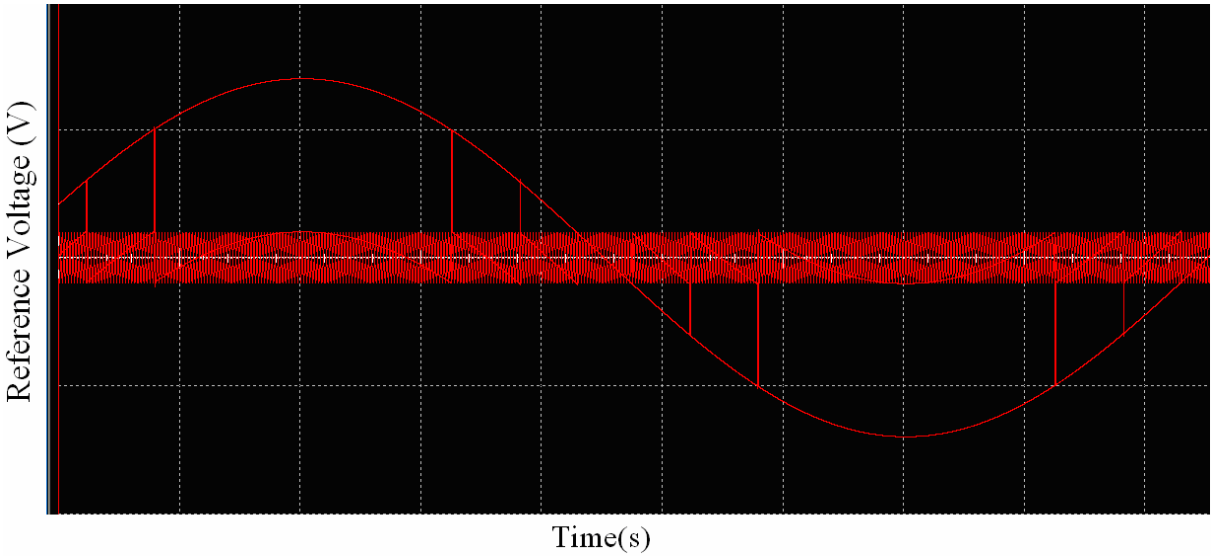


Figure 4-14: Carrier triangular waves with respect to reference sinus signal

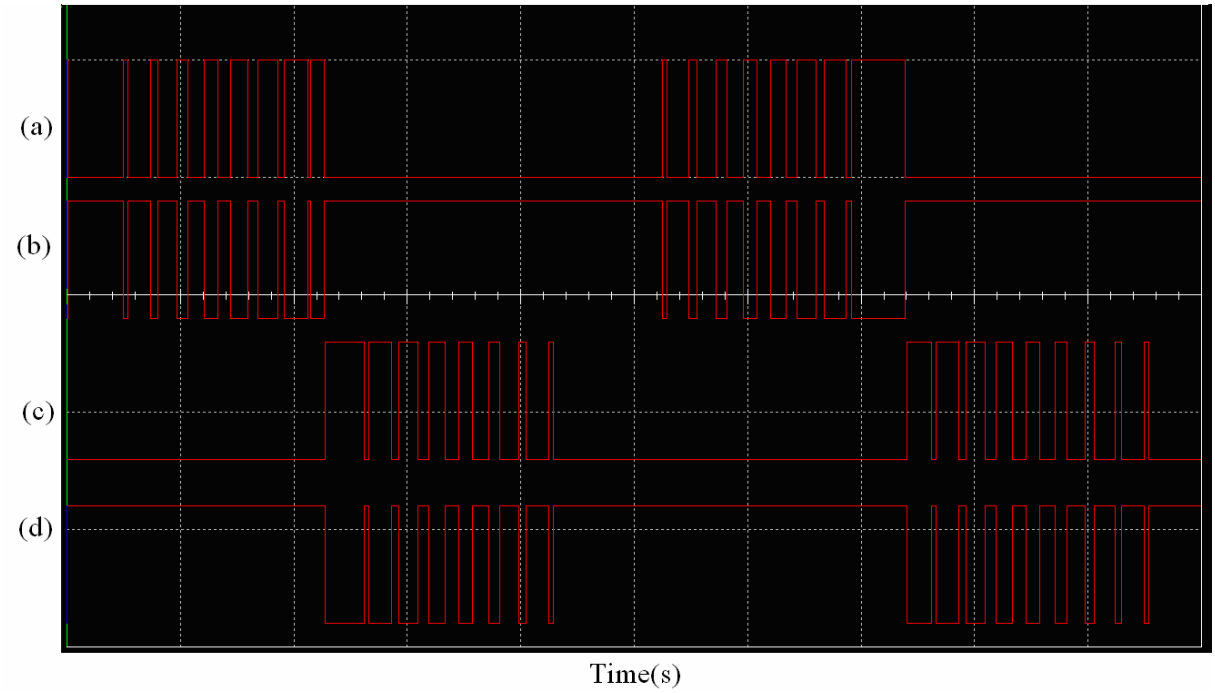


Figure 4-15: PWM signals of the first inverter (20 kHz). (a) positive portion of *Ton,1*, (b) negative portion of *Ton,2* inverted, (c) positive portion of *Ton,3*, (d) negative portion of *Ton,4* inverted

The first inverter generally runs at higher switching frequency for minimizing harmonics. We select a simple control set based on the standard triangle wave-sinusoidal reference comparison

to get switching states. Then we perform a Fourier analysis of idealized total output voltage at the transformer.

4.1.4 Second Inverter

For low-switching-frequency applications, low switching voltage algorithm is used. The basic idea of this technique is to connect each cell of the inverter at specific angles to generate the multilevel output waveform, producing only a minimum of necessary commutations. Note that only one angle needs to be determined per power cell. These angles can be computed using the principle

$$U_R = \hat{U}\sin(\omega.t) \tag{4-6}$$

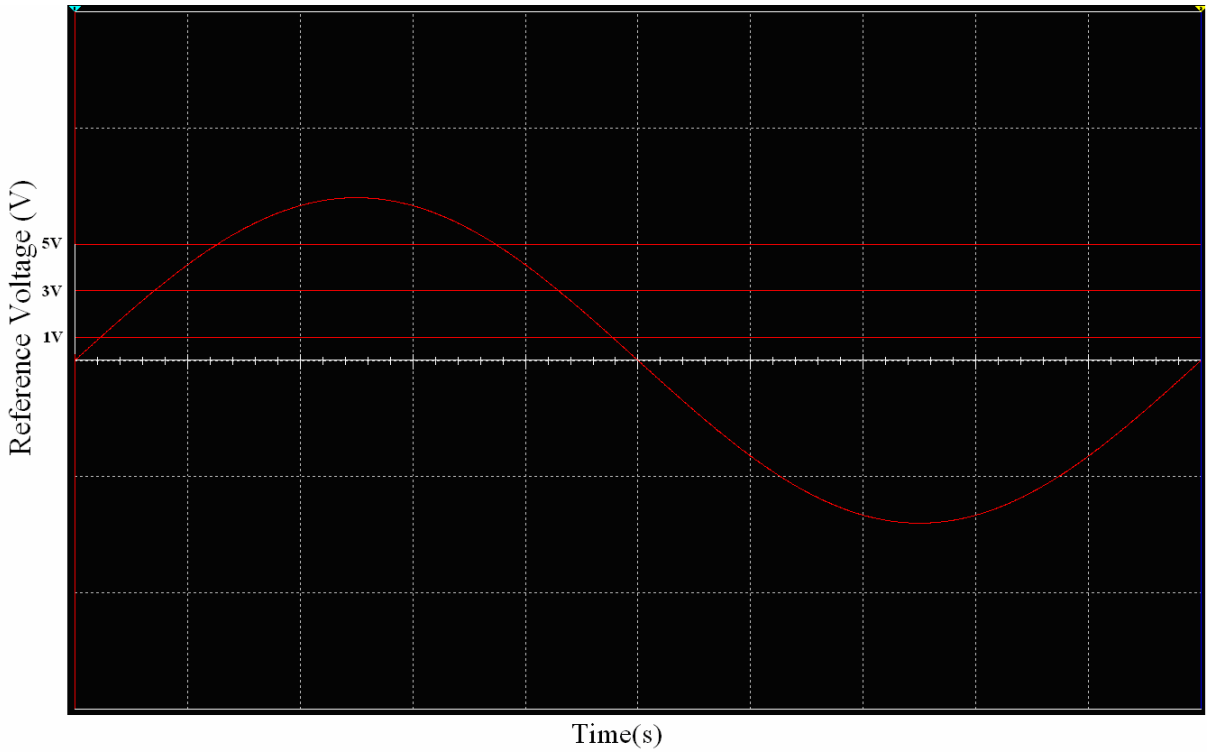


Figure 4-16: Constant DC voltages compared to reference sinus signal of the second inverter

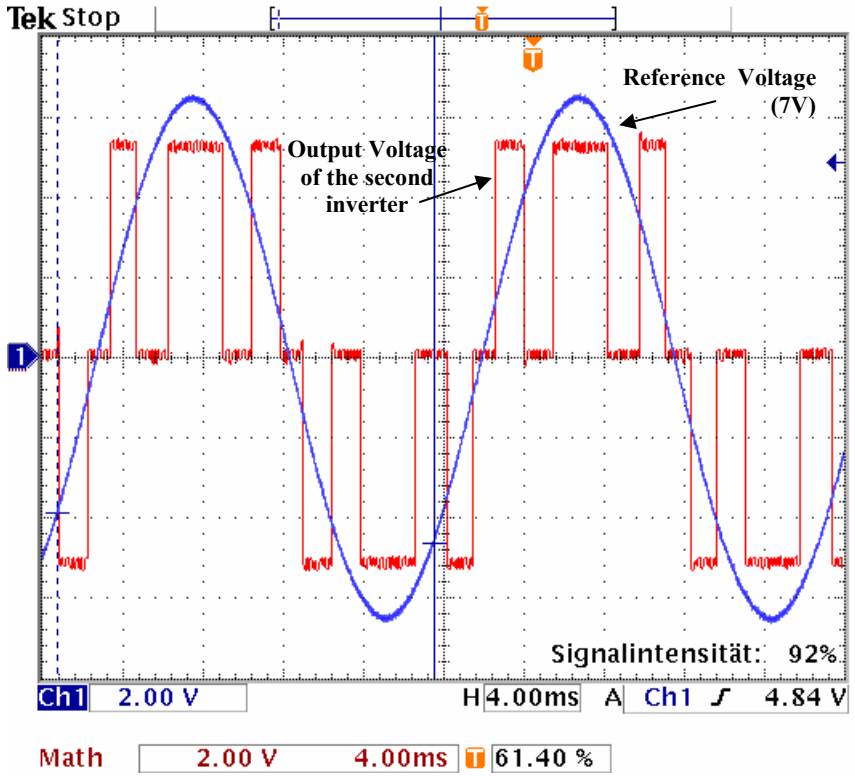


Figure 4-17: Illustration of the second inverter output respect with reference sinus signal

The second inverter is seen in figure 4-17 shows the switching times during two periods. The reference voltage values are -1V, -3V, -5V, 1V, 3V and 5V.

$$Inverter_2 = \begin{cases} ON & (3V > U_R > 1V) or (U_R > 5V) or (-1V > U_R > -3V) or (-5V > U_R \\ \text{OFF} & (1V > U_R > -1V) or (5V > U_R > 3V) or (-5V > U_R > -3V) \end{cases} \quad (4\text{-}7)$$

where U_R is sinus signal. Decreasing the losses is done with low switching frequencies, namely 6 times ON, 6 times OFF.

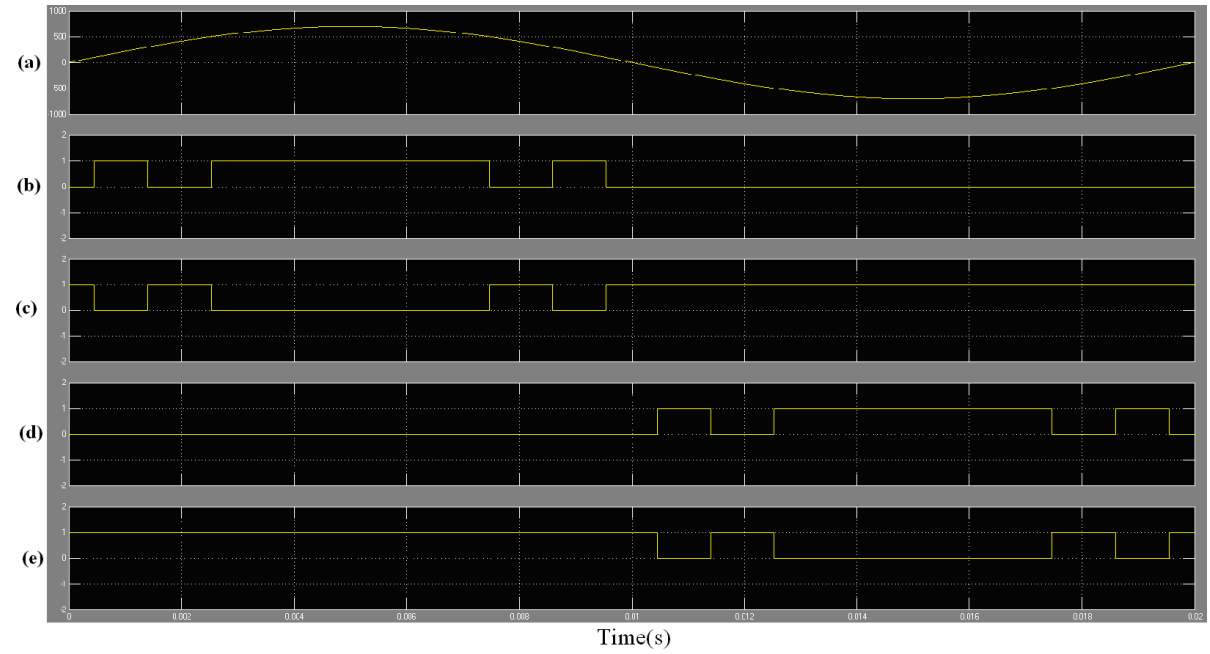


Figure 4-18: PWM control of proposed inverter (second inverter) (a) sinusoidal signal, (b) upper triangular signal, *Uc1*(c) lower triangular signal, *Uc2* (d) positive portion of *Ton,1*, (e) negative portion of *Ton,2* inverted, (f) positive portion of *Ton,3*, (g) negative portion of *Ton,4* inverted

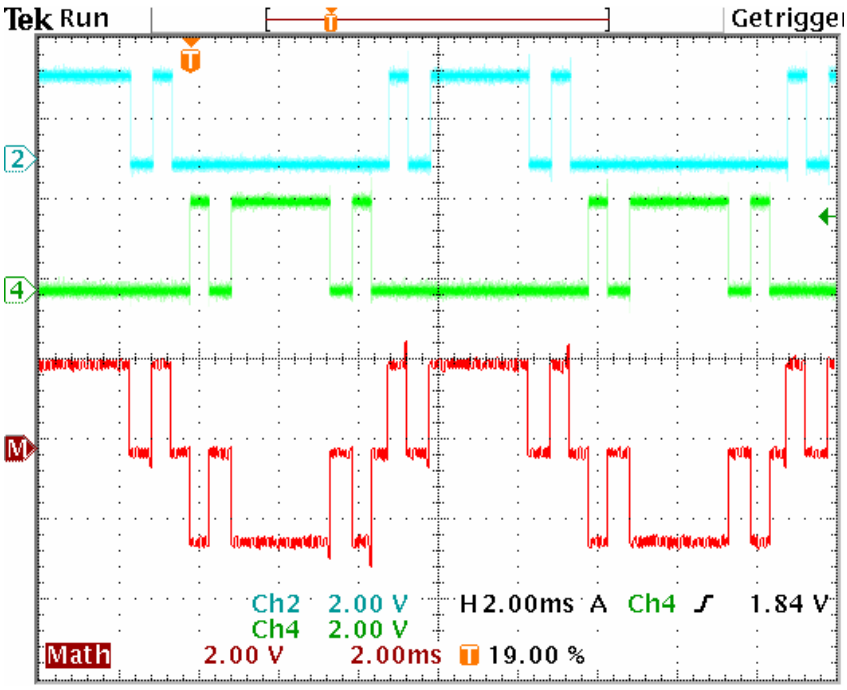


Figure 4-19: Illustration of the control signals of the second inverter

4.1.5 Third Inverter

For the third inverter, the same principle is used to compute the angles.

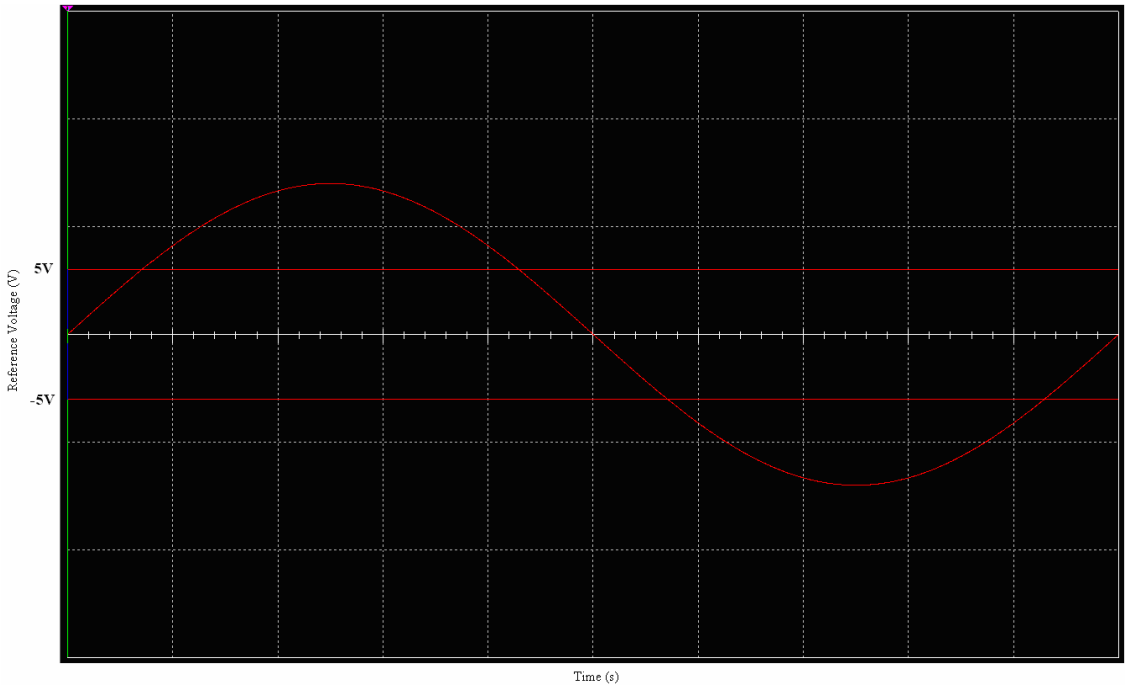


Figure 4-20: Constant DC voltages compared to reference sinus signal of the third inverter

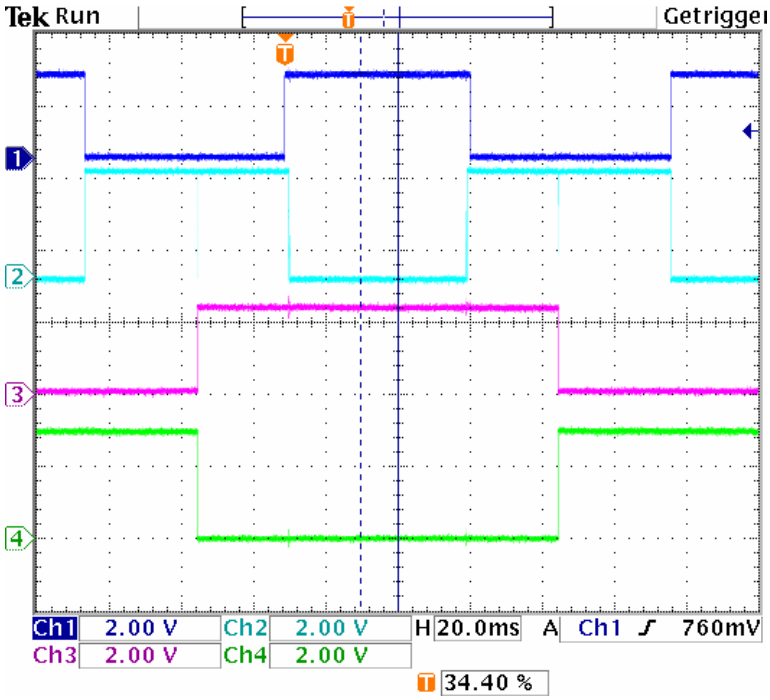


Figure 4-21: Illustration of the control signals of the third inverter

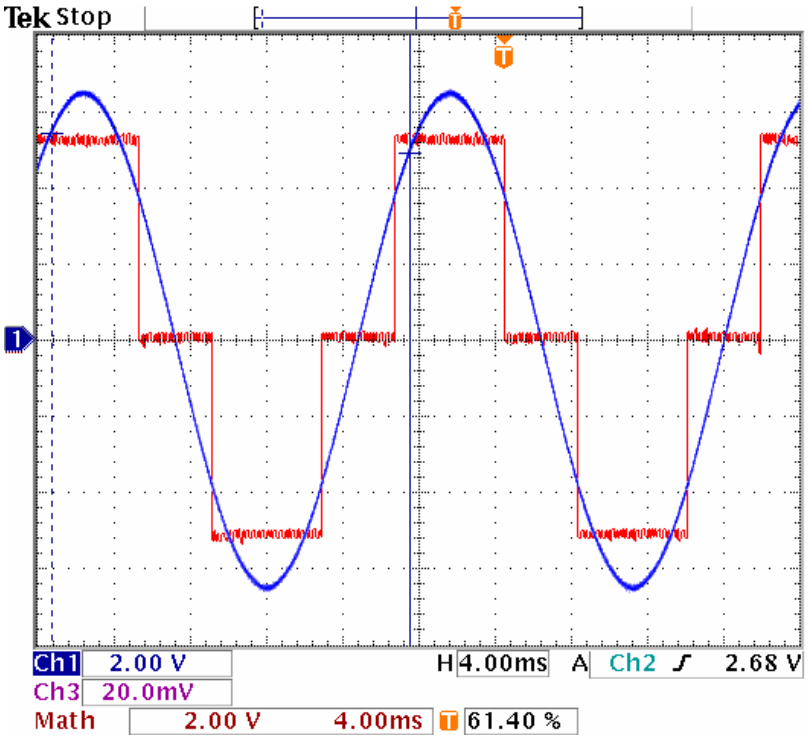


Figure 4-22: Illustration of the third inverter output respect with reference sinusoidal signal

The third inverter, seen in figure 4-22, shows the switching times during two periods. The reference voltage values are -5V, and 5V.

$$Inverter_3 = \begin{cases} ON & U_R > (5V) or (-5V) > U_R \\ \text{OFF} & (5V) > U_R > (-5V) \end{cases} \quad (4\text{-}8)$$

The third inverter, seen in figure 4-23, shows the switching times during one period. Decreasing the losses is done with low switching frequencies, namely 2 times ON, 2 times OFF in one period. Compared to second inverter, the third inverter operates only at one third of switching frequency times and has less loss.

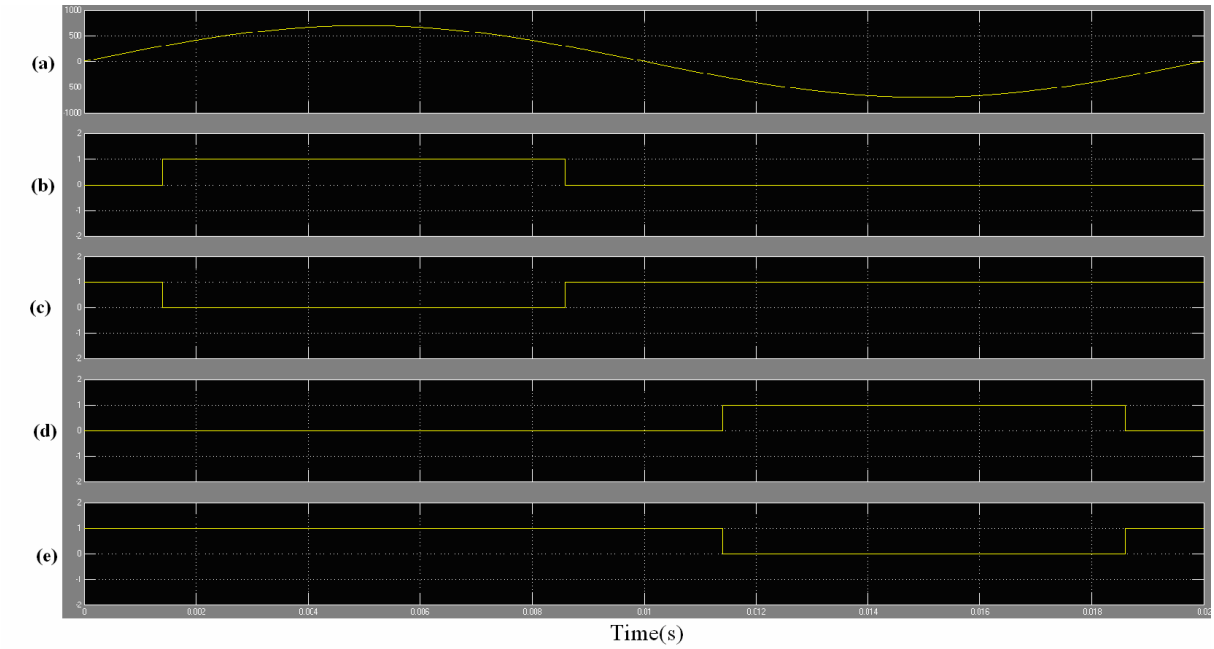


Figure 4-23: PWM control of proposed inverter (third inverter) (a) sinusoidal signal, (b) upper triangular signal, U_{c1} (c) lower triangular signal, U_{c2} (d) positive portion of $T_{on,1}$, (e) negative portion of $T_{on,2}$ inverted, (f) positive portion of $T_{on,3}$, (g) negative portion of $T_{on,4}$ inverted

The main advantage is that the converter very few times per cycle, reducing the switching losses to a minimum. In addition, low-order harmonics are eliminated, facilitating the output-filter design [75]. However, this method needs important off-line calculations to compute the angles for a variety of modulation indices and is therefore not very suited for highly dynamic systems.

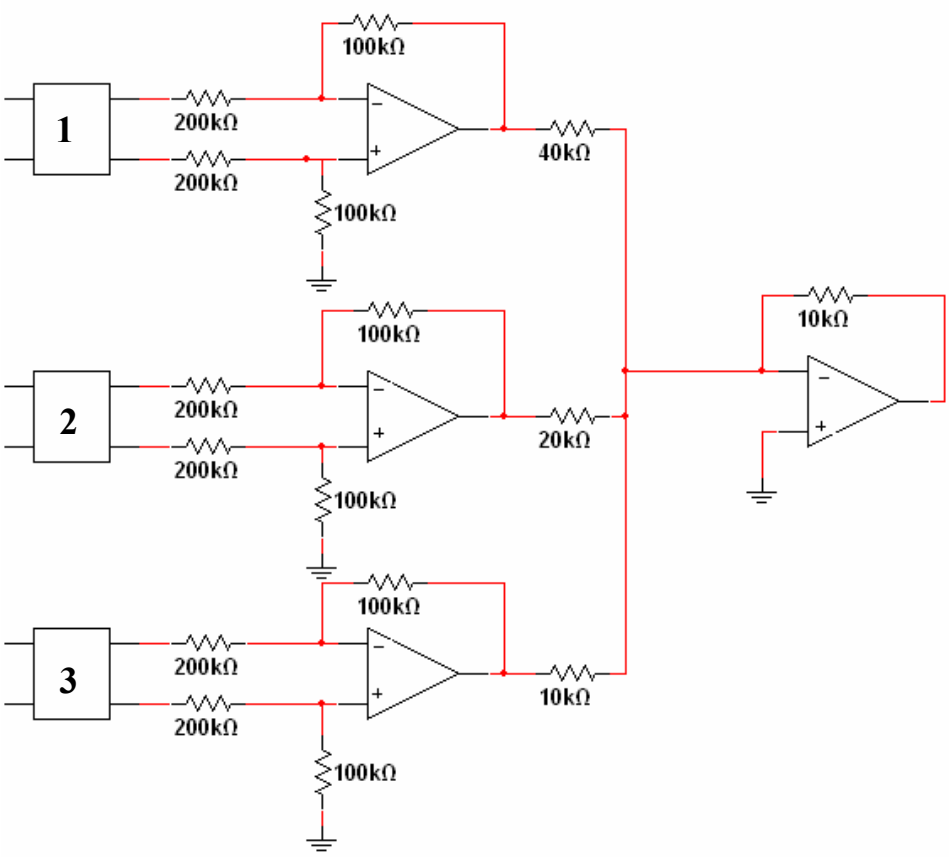


Figure 4-24: Harmonics measurement of three inverters via summing amplifiers

Total harmonic distortion is measured by amplifying and summing the output signals of each inverter [58]. The output than is given to Dynamic Signal Analyzer HP 3561A, connecting it to the computer and monitoring the signals as given in figure 4-24. Each of the inverter output is amplified and all added up in order to obtain the total harmonic components which is being measured by the signal analyzer.

Weighted total harmonic distortion (weighted THD) is proposed by Holmes [31] and is used in this chapter for the analysis and comparison of spectral performance of the different modulation techniques. Normalizing this expression to the quantity $U_1/(\omega_1 L)$ the weighted total harmonic distortion ($WTHD$) becomes defined as

$$WTHD = \frac{\sqrt{\sum_{i=2}^{\infty}\left(\frac{U_i}{i}\right)^2}}{U_1} \tag{4-9}$$

where U_1 is the fundamental voltage.

Table 4-6 shows the total required components of in two investigated multi-level converters as a function of the number of voltage levels. Although the same number of modules

(MOSFETs/diodes) is needed in the two considered topologies, the total number of components necessary in these two topologies is different at higher voltage levels.

Table 4-6 Comparison of power component requirements for multi-level topologies

Topology	Series Connected 2-Level H-Bridge (with different DC bus)	Series Connected 2-Level H-Bridge (with the same DC bus)
Number of modules (MOSFET/Diode)	6(N-1)	6(N-1)
Number of clamping diodes	0	0
Number of dc link capacitors	3(N-1)/2	1
Number of balancing capacitors	0	0

where N is the number of cascade-inverter levels.

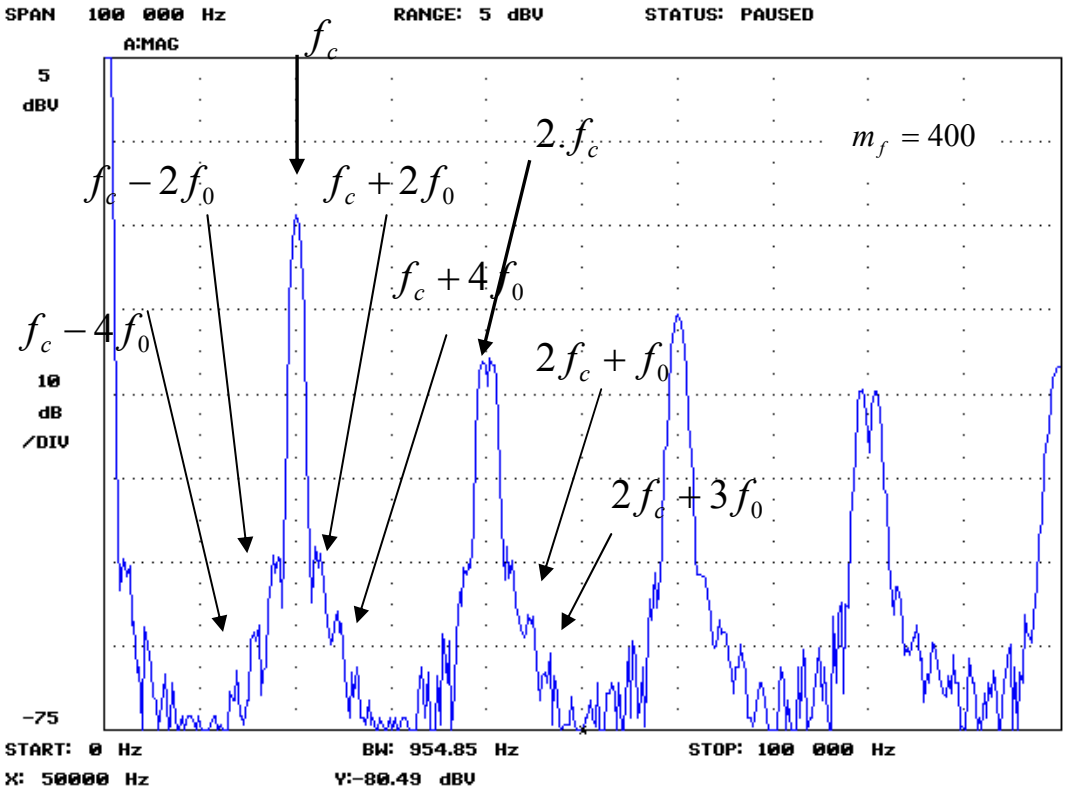


Figure 4-25: Typical phase output frequency spectrum, at a given switch commutation frequency (20 kHz)

In figure 4.25 a triangular carrier has only odd Fourier components, so the output spectrum only has carrier components at odd harmonics of the carrier frequency. The first carrier

components occur at the carrier frequency f_c. Side-band components occur spaced by $2 f_0$ from other components, around all multiples of the carrier frequency.

4.2 Power Losses

4.2.1 Compact Power Semiconductor Model

In this thesis, MOSFET modules are considered due to the modularity-laboratory power level- and degree of freedom for switching frequencies. For analysis purposes, the MOSFETs and diodes are usually considered ideal, i.e. lossless, featuring infinite current and voltage handling capability. The ideal MOSFET is simulated as being controlled by a logical gate signal ($g_s \geq 0$). It conducts an arbitrary current with zero on-state voltage when the switch is on ($g_s > 0$) and blocks any forward or reversely applied voltage with zero current when the switch is off ($g_s = 0$). The idealized device can be switched instantaneously between on and off states or vice versa by applying corresponding gate signals [122].

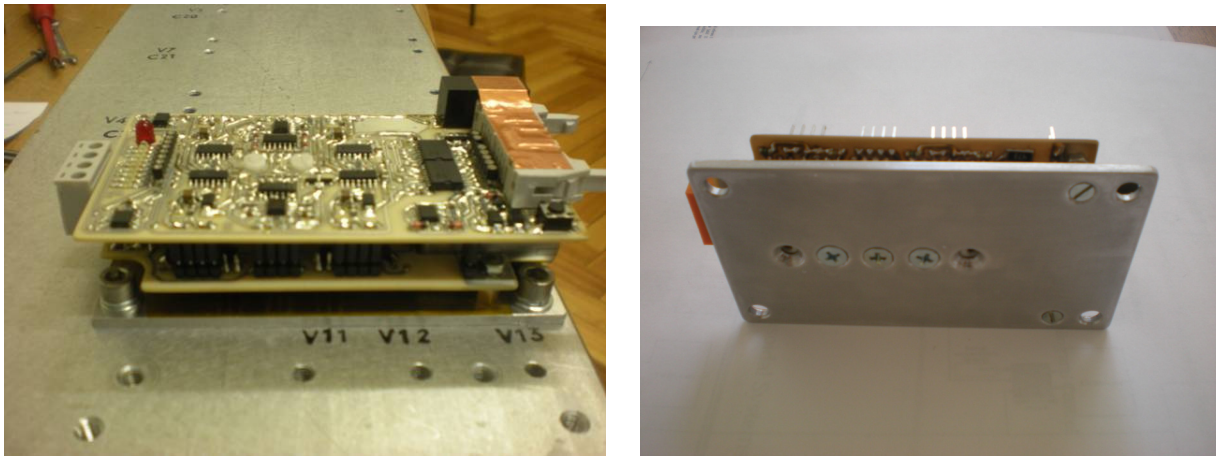
4.2.2 Conduction and Switching Losses

Figure 4-26: Switching losses in power devices (*Eon*+*Eoff*). Eon includes SPP20N60C3 diode commutation losses. *E* = *f* (*Id*), inductive load, *Tj*=125°C, *Vds*=380V, *Vgs*=0/+13V, *Rg*=3.6Ω

Switching losses are created by the commutation processes between the different switch states whereas losses in magnetic components as core and copper losses. Only turn-on and turn-off losses of active switches and recovery losses of diodes are considered. Turn-on losses of diodes are usually small so that they can be neglected.

4.2.3 Selection of Heat Sinks

A special standard MOSFET inverter module with switches has been mounted on module cooling plate and driver circuits including protection function has been designed and realized by Wenzel Meier (Figure 4-27).



(a) **(b)**

Figure 4-27: (a) module with switches (b) heat sink of each module

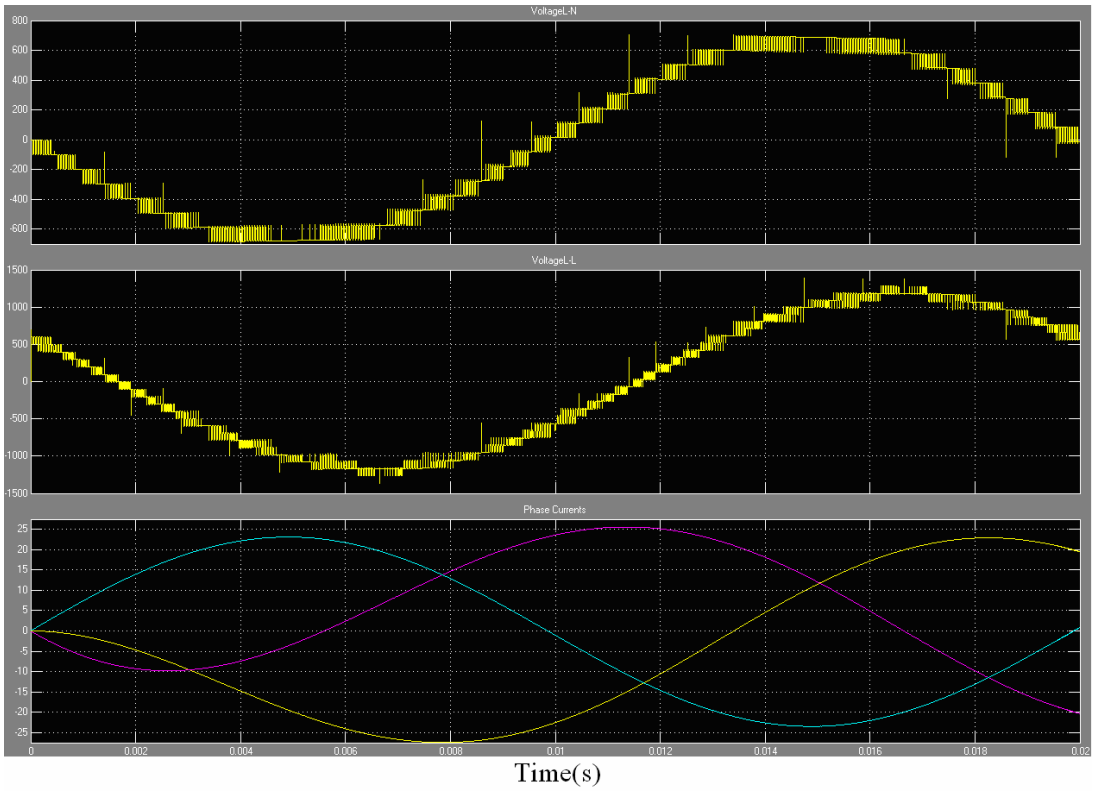


Figure 4-28: PWM control of proposed 2-level inverter at 3 kHz (a) phase waveform, (b) line-to-line waveform, (c) phase currents

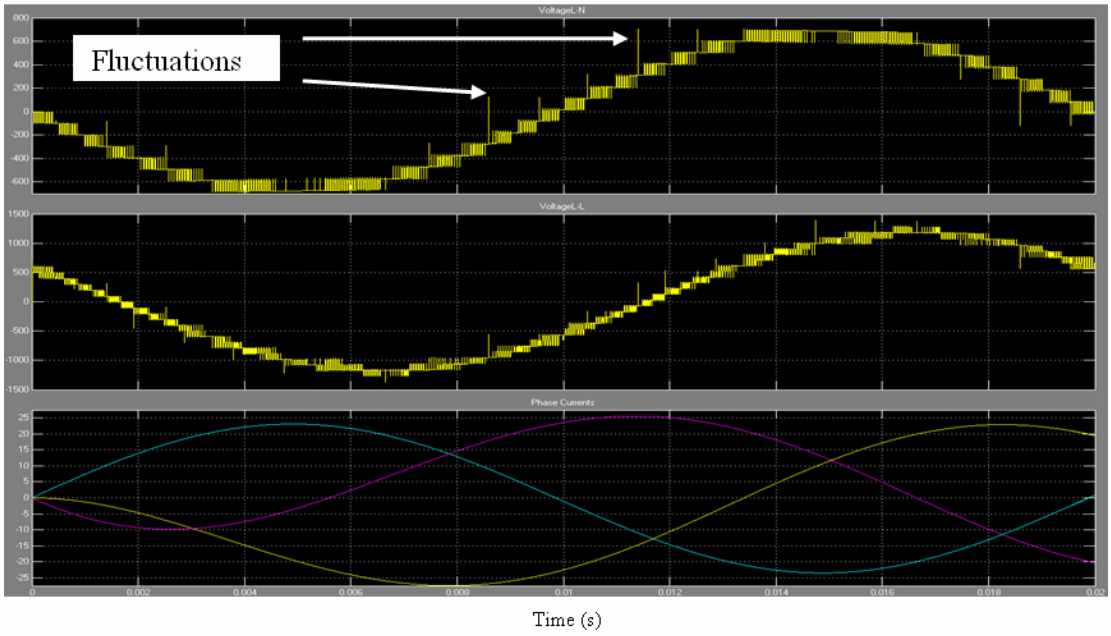


Figure 4-29: PWM control of proposed 2-level inverter at 20 kHz (a) phase waveform, (b) line-to-line waveform, (c) phase currents

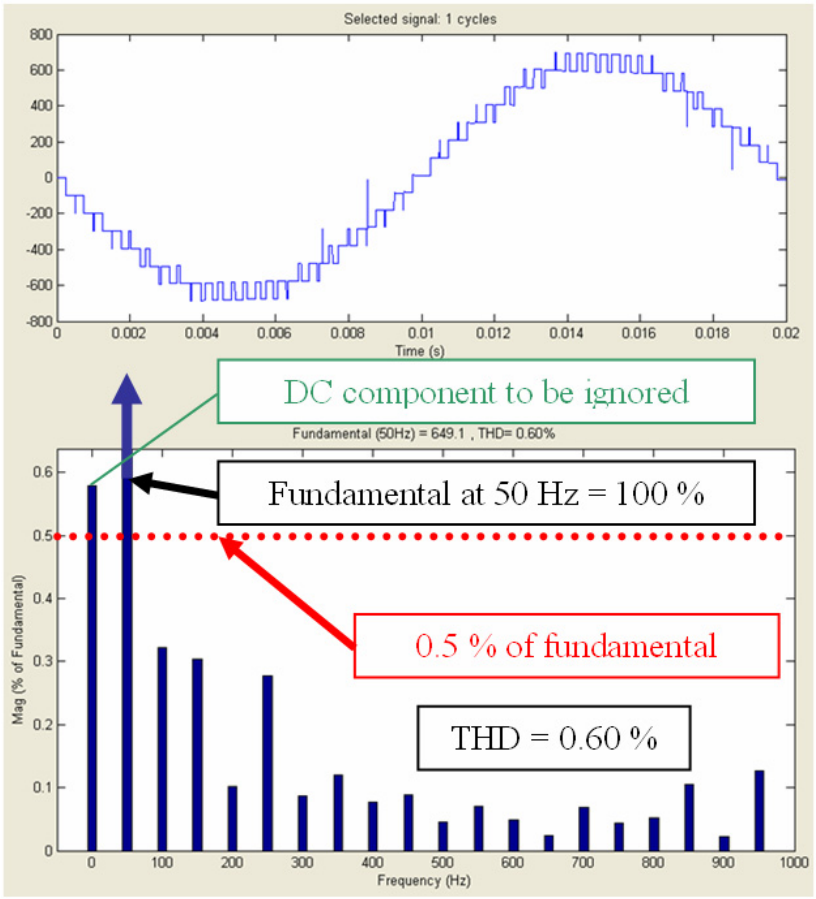


Figure 4-30: Fourier analysis of simulated idealized output voltage at 20 kHz

In the control circuit, an eight-bit microcontroller is employed to generate necessary gate drive signals. Due to limited computational capability and control resolution, the experimental

output quality is not as good as expected, especially at low modulation indexes. It should be noted that the level of steps is actually reduced when modulation is less than 0.5. This results agrees the finding in initial analysis in which the convergence fails at M = 0.5: At M = 0.4, the 7 levels become 5 levels, and at M = 0.1, the 7 becomes 3 levels. THD results are obtained for up to 1100 Hz frequencies.

Table 4-7 Specifications of the prototype

Items	Specifications and features	
Power MOSFET	Inverter	650V/20.7A
Cascaded transformers	EI lamination	1:a, 1:2a, 1:4a
Battery (V_{dc})	Oerlikon	12V 50Ah
Output (V_o)	8-level PWM	AC 230V

The increased resistance, and even more, the increased reactance (due to higher frequency), will result in an increased voltage drop and an increased voltage distortion. THD of current is less than voltage because of filtering effect of L.

Table 4-8 Parameters in the hardware prototype

Parameter of component	Value
Number of series H-bridges at the input	3
Rated power	1400VA
Nominal peak input voltage	30
Primary DC-link voltages	0..30V
Output Ph–N voltages	24 V_{rms}
Transformers turn ratio	1:8.3
Primary DC link capacitors	3300μF, 350V
Fundamental frequency	50Hz
Switching frequency	4 kHz...20 kHz (suitable for MOSFET only)

4.3 Conclusion

The measurement is made by current transducer LTS 25-NP that has 3 numbers of primary turns. The voltage drop across load resistor corresponds to the current of a phase.

The function of the proposed inverter and the designed controllers are verified by experimental results on a laboratory scale prototype. The prototype is a 200VA, single-phase transformer. The digital control unit was implemented based on an ATmega16 controller. It is worth noting that low voltage power MOSFETs (MOSFET + internal body diode with the break down voltage of 650 V) was intentionally used in the prototype to demonstrate a scale down of the real situation. However, in the medium voltage levels, the IGBTs would be the best choice due to better output power quality and current ratings.

To verify the simulation results, a quasi-eight-level voltage source converter using cascaded-inverters with the same DC source is used as a hardware prototype. The large power cells

commutate only a few times per cycle. Since the small power cells manage only 14.1% of the total power, a big reduction in switching losses is achieved.

Another major advantage of the SC2LHB is its circuit layout flexibility, because each level has the same structure and there are no extra clamping diodes or voltage balancing capacitors, which are required in the NPC and the FLC topologies. The number of output voltage levels can then be easily adjusted by changing the number of H-bridge cells. However, the control complexity is directly proportional to the number of H-bridge cells. As the number of voltage levels increases, the voltage imbalance problem becomes more of a concern. To achieve stable system, a well-defined model is necessary.

5 Modelling and Simulation

5.1 Schematic Description of the System

The first prototype was built to check the function of proposed multilevel topology. During the construction of the prototype, several problems have been fixed. The most critical problem concerns the insulation among the three inverters there are in the system. Indeed, if the insulation fails the common mode current will be free to flow and the multilevel will not work properly anymore [70] [71]. The first test had the aim to verify insulation applying switching voltage to only one phase, just to prove the absence of common mode current [28]. Then, some tests were done to see the operation of dual 2-level inverter as multilevel converter. For this purpose, a PWM modulation has been implemented and some screenshots have been captured. The detailed results and configurations are listed in appendix A. This technique allows successful voltage control of the fundamental wave as well as suppression of a selective set of harmonics [44].

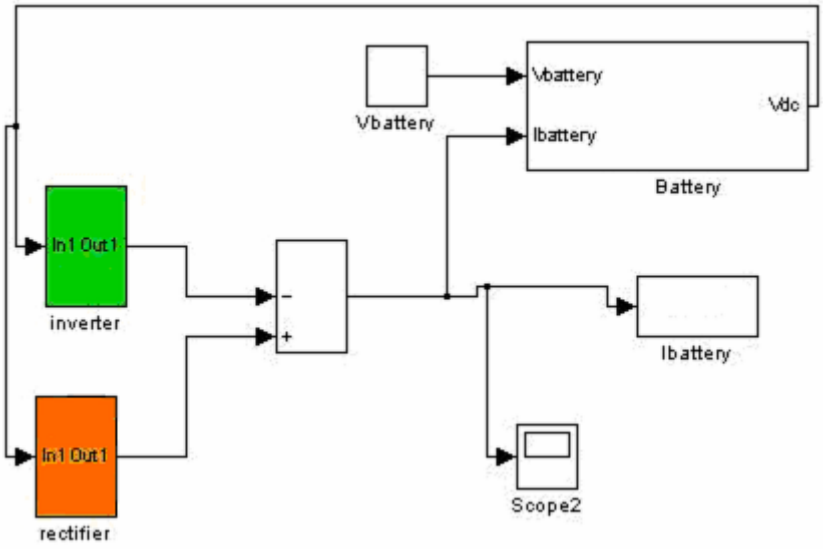


Figure 5-1: MATLAB/SIMULINK model of wind turbine system

The model of the inverter implemented in MATLAB-SIMULINK is shown in figure 5-1. SIMULINK has been chosen from several simulation tools because its flexibility in working with analogue and digital devices [16] [40]. Mathematical models can be easily incorporated in the simulation and the presence of numerous tool boxes and support guides simplifies the simulation of large system. SIMULINK is capable of showing real time results with reduced simulation time and debugging. The experimental evaluations have led to the following considerations:

- the simulation results have been validate by the experimental results
- the design of the controller is well performed

In the present simulation measurement of currents and voltages in each part of the system is possible, thus permitting the calculation of instantaneous or average losses, efficiency of the drive system and total harmonic distortion [9].

The green block is the 3-phase inverter connected to the two blocks representing the rectifier as shown with orange block and battery. The DC bus has 15 units of 24V batteries connected in series. The two inverters are composed by several masked subsystems. The proposed system consists of three blocks, rectifier, inverter and battery. In rectifier unit, as shown in figure 5-2, there are the wind model, PMSM and rectifier modules. In inverter unit, the inverter, grid and filter blocks are modelled [7]. In order to simulate the entire system for the assessment of the control system, the models of the following items are required:

- model of the PMSM
- model of the rectifier
- model of the DC-link capacitor
- model of the converter
- model of the transformer and cable (modelled as LCL-filter)

The two blocks are composed by several masked subsystems. Rectifier block has a wind motor simulation model and inverter block has 1-phase load. Both these components have parasitic snubber capacitances and resistances which can not be zeroed without creating problems to the solver [51]. However, the components are well suited for a behavioural analysis of the system.

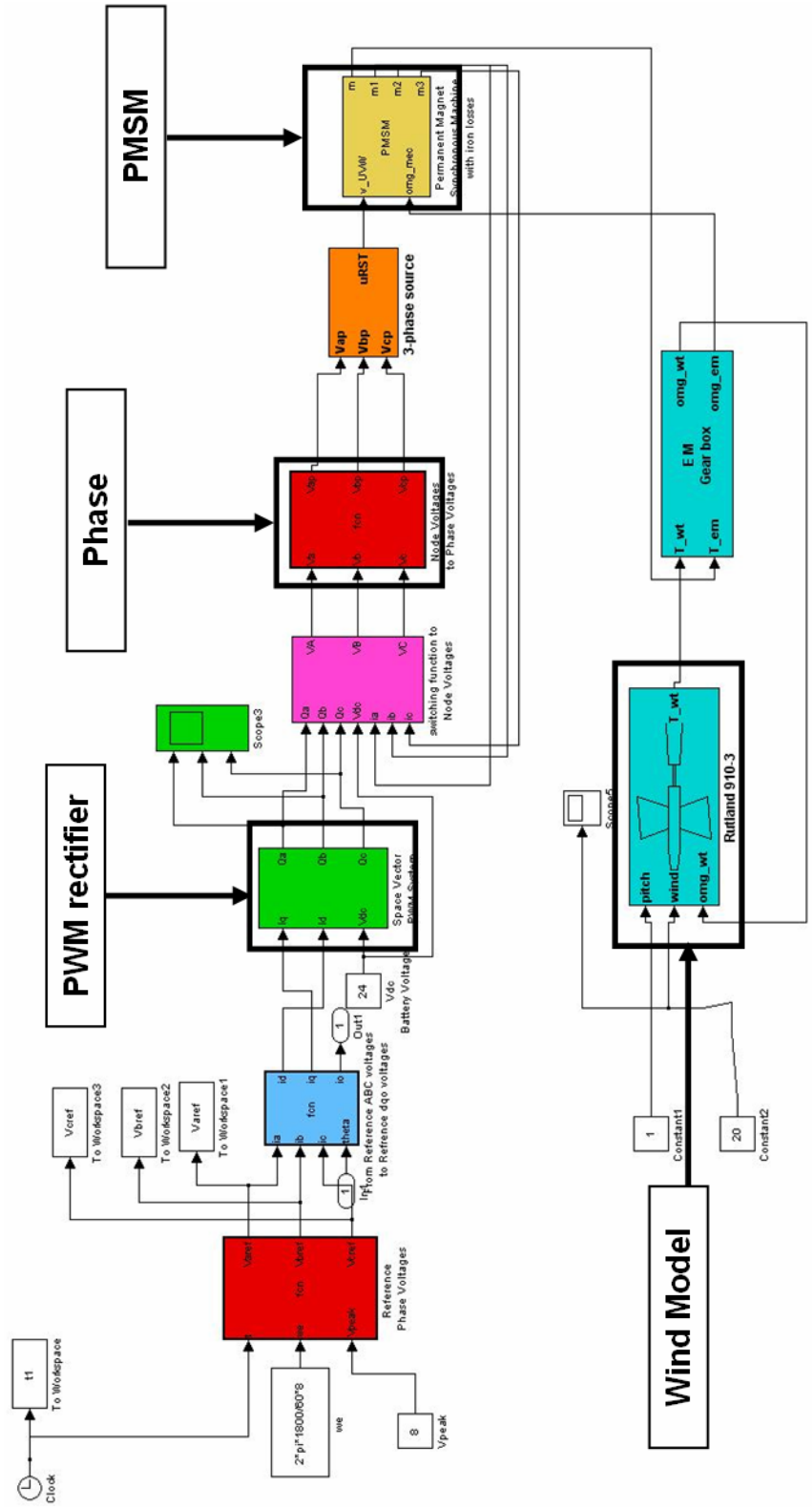


Figure 5-2: Rectifier block set

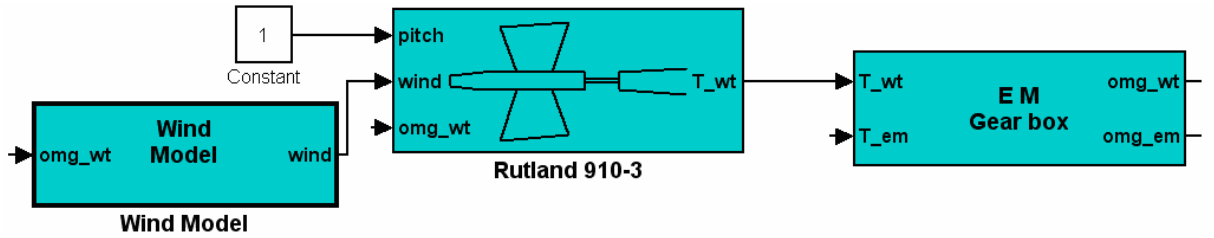
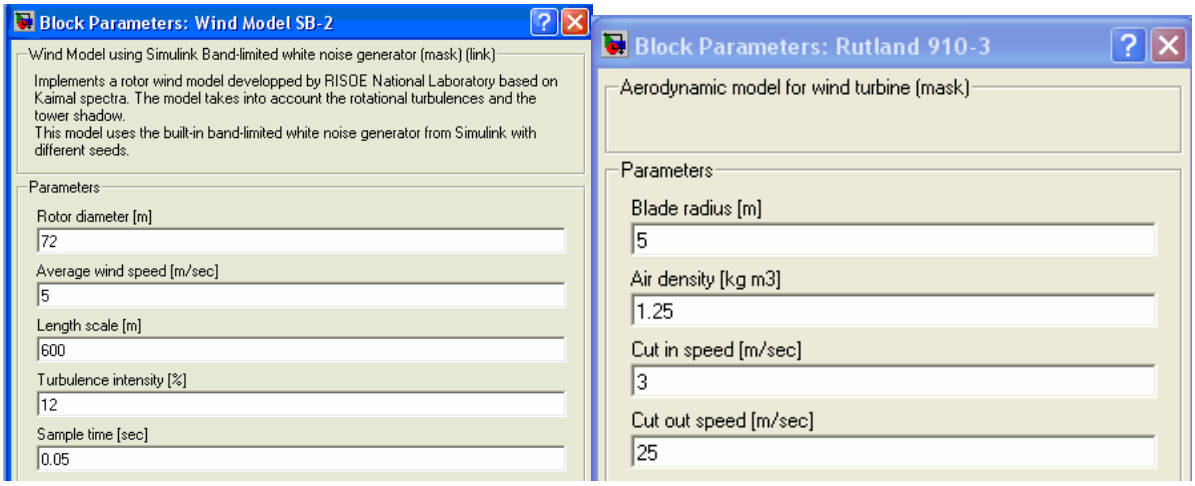


Figure 5-3: Wind modelling system connected to PMSM

Wind model defines the rotor diameter, average wind speed, and turbulence intensity. In toolbox, white noise is filtered through Kalman filter and the characteristic of wind is determined [110]. The wind information is then given to motor and the cut in, cut out speed, and blade radiuses are described.



(a) **(b)**

Figure 5-4: (a) Parameters of wind model (b) Parameters of wind turbine

The amount of electrical power produced by a turbine depends on the size and type of the turbine and where the turbine is located. A characteristic that represents a typical power output in relation to the wind speed is given in figure 5-5. At low wind speeds, no electrical power is generated. Approximately 3 m/s and above the turbine is rotating, and at about a wind force (12 - 13 m/s) the turbine is supplying its maximum power.

At wind speeds over 25 m/s former generations wind turbines were designed to shut down in a controlled way to avoid overloading or damaging the turbine's installation or construction. Modern turbines however are equipped with a pitch control that changes the angle of the rotor wing in extreme weather. The result is that the power supply can be guaranteed even in bad weather conditions. When very heavy storms occur it still is necessary to stop the turbine and set pitch angle into 0° "sailing" position.

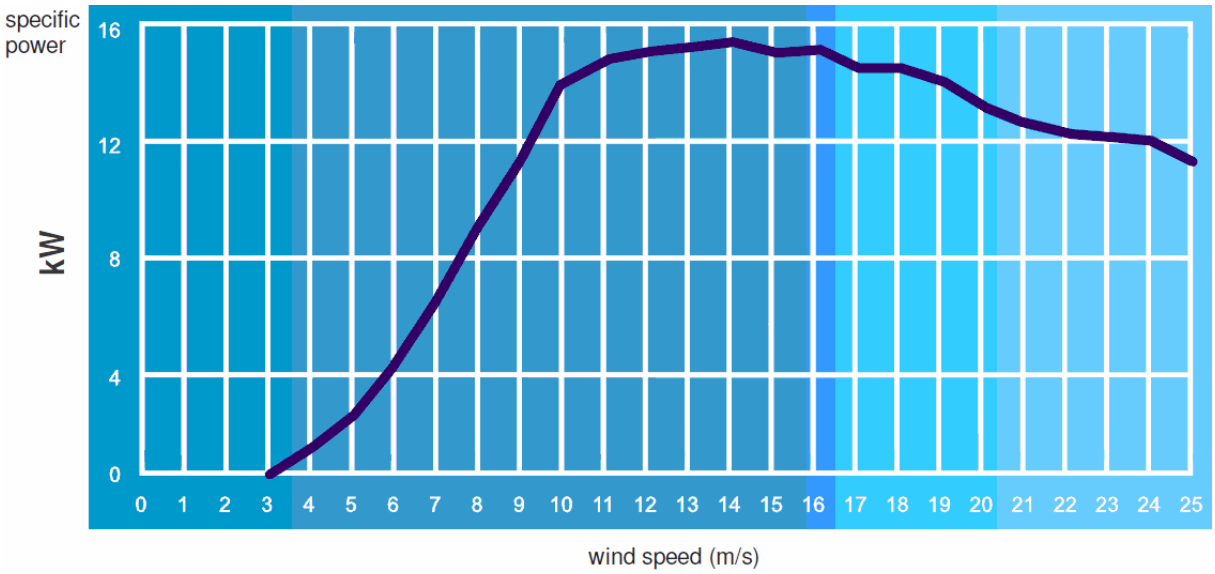


Figure 5-5: Turbine power curve [120]

The power output curve of the turbine is used for simulation parameters. Control system features such as automatic stop in case of too strong wind, keeping rotation-speed constant, adjustment to wind availability; automatic speed reduction is case of storms or gusts and temperature control which are not aimed in this thesis [73].

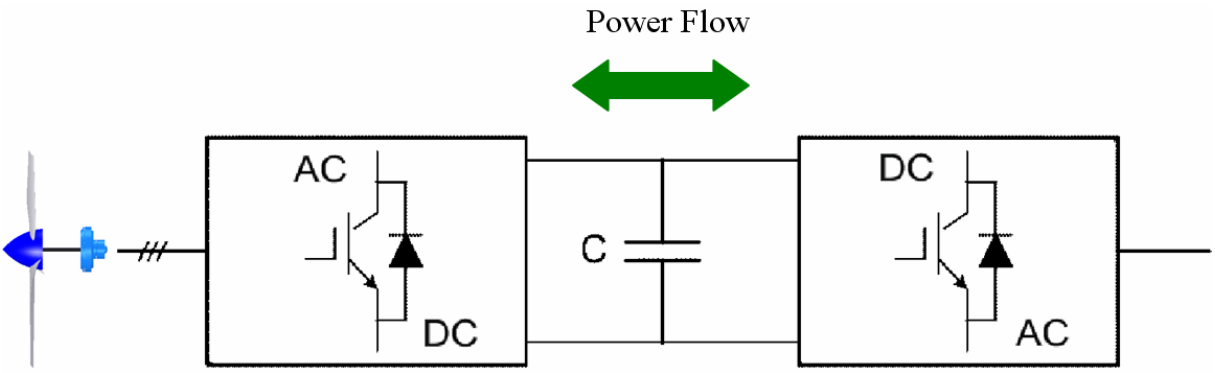


Figure 5-6: Small wind turbine with active rectifier for maximum power point tracking and unity power factor

Maximum power point tracking depends on the wind speed information and power delivered from the wind turbine. DC bus voltages and currents are determined from the inverter and converter side.

5.2 The Structure of the System

For all turbines, configuration data and general mechanical properties were collected in order to obtain design levels through implementation of simple load models and load cases [52][84]. Datasets of all available test measurements on the operating turbines were gathered.

An effort was made to neglect all datasets in which measurement equipment failures existed that could have compromised the quality of the datasets [72]. Due to the difficulty and expense involved in measuring axial and shear forces in the field, most load cases involving these types of loads were disregarded in this study.

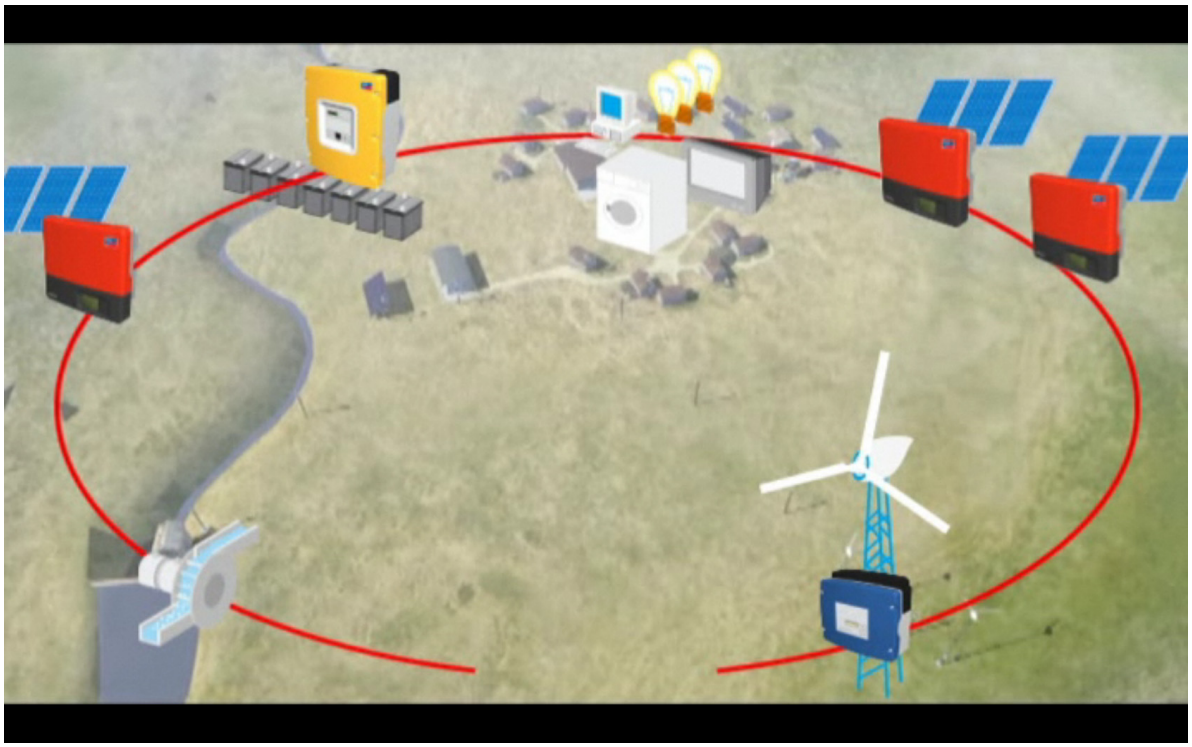


Figure 5-7: A snapshot of the animation showing the single-phase load of a village with PV and wind turbine [128]

The single-phase configuration for small village is shown in figure 5-7. The energy sources which are gained from wind turbines, photo voltaic, and may be water dam can be used for the energy consumption of the village. The red circle indicates that the system has single-phase and in the future if high power is required the system can be expanded into 3-phase system where large consumers are needed.

Battery lies in the middle point of such a network. With the energy from the battery, a changing voltage network to which it is characterized by flexibility and intelligent management of energy producers and consumers is built. Expanded learning opportunities and facilities such as schools, hospitals can be provided. The intelligent battery storage management makes the system small and inexpensive.

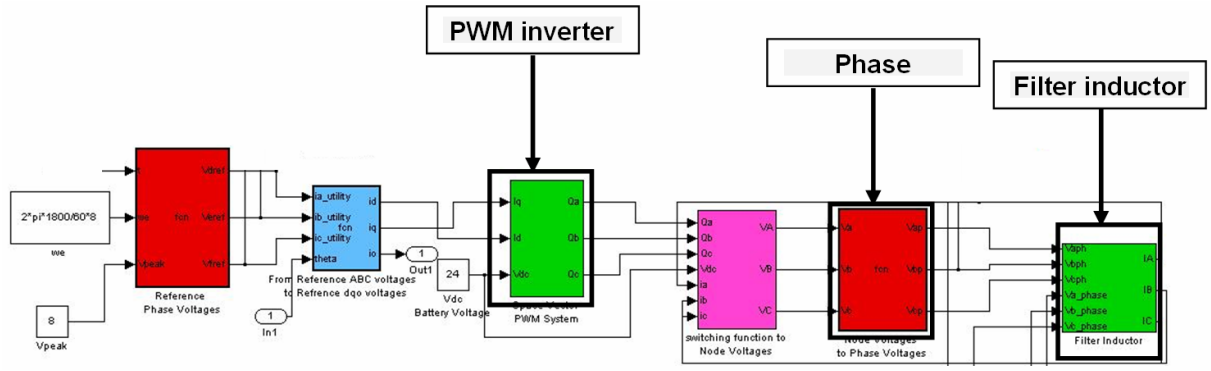


Figure 5-8: Inverter block set

5.2.1 Permanent-Magnet Synchronous Machine

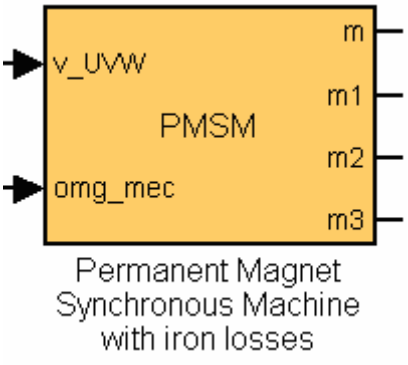


Figure 5-9: Permanent magnet synchronous machine model with iron losses

The PM motor drive simulation was built in several steps like abc phase transformation to $dq0$ variables, calculation torque and speed, and control circuit [91][101][104]. The abc phase transformation to $dq0$ variables is built using Parks transformation and for $dq0$ to abc the reverse transformation is used. For simulation purpose the voltages are the inputs and the currents are output. Parks transformation used for converting V_{abc} to V_{dq0} and the reverse transformation for converting I_{dq0} to I_{abc} is implemented in PMSM tool.

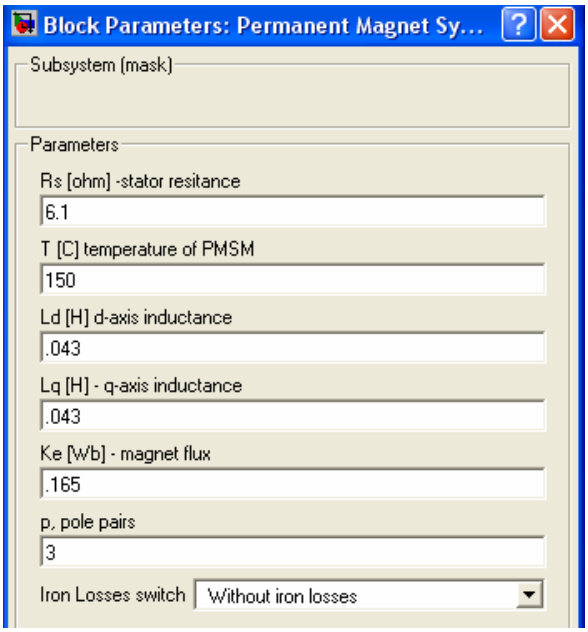


Figure 5-10: PMSM parameters

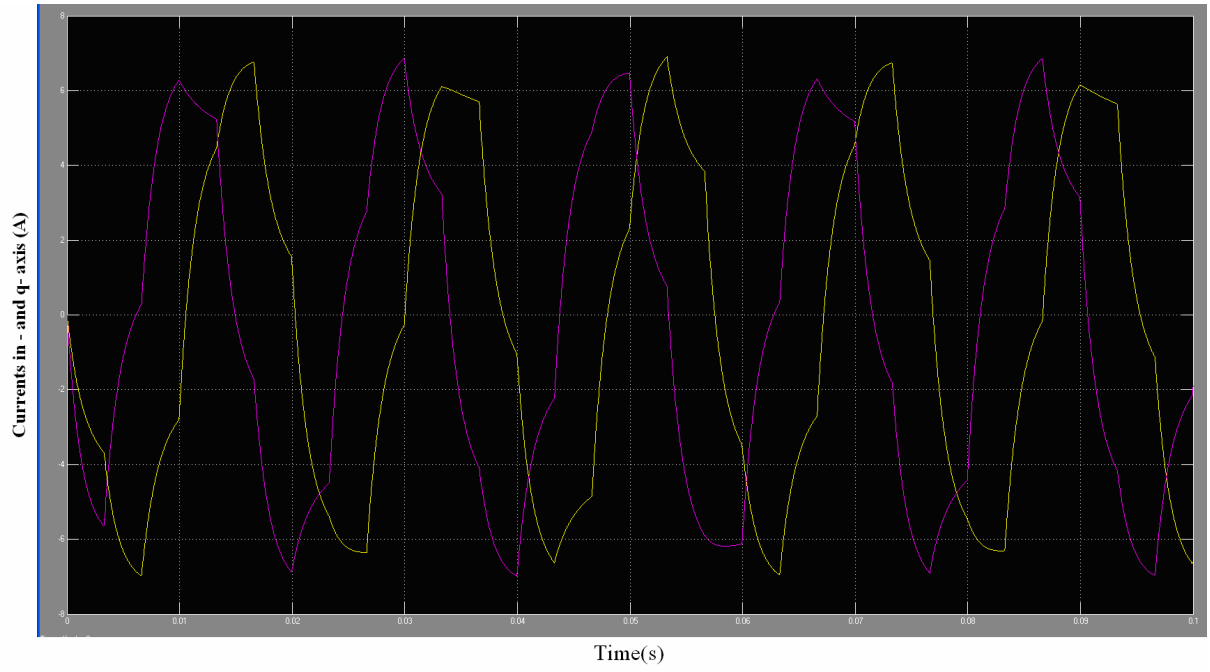


Figure 5-11: Currents in d- and q-axis

5.2.2 Algorithm Analysis

The inverter model is written as M-file that includes the explanation of PWM hysteresis method which is the core of the control made over the 2-level inverter. The hysteresis controller compares the actual phase current with the commanded ones [43][76][82]. If the magnitude of the error is greater than a present level (2%), the inverter leg is switched appropriately to low, although the actual current also depends on the currents in the other phases [56][108] and this is shown for a single phase in figure 5-15.

For a given phase, the transistor that requires to be switched is dependent on both the error sign and the sign of the commanded current (I^*). For a hysteresis bandwidth of I_{ref}, the algorithm used for the inverter leg of Q_2 / Q_3 and individual current control in each phase is:

$$i_{low} = I_{ref} - 2\% I_{ref} \quad (5\text{-}1)$$

$$i_{up} = I_{ref} + 2\% I_{ref} \quad (5\text{-}2)$$

$$\text{If } i \le i_{low} \text{ then } V_a = V_{dc} \quad (5\text{-}3)$$

$$\text{If } i_{low} < i < i_{up} \text{ and } \frac{di}{dt} \ge 0 \text{ then } V_a = V_{dc} \quad (5\text{-}4)$$

$$\text{If } i_{low} < i < i_{up} \text{ and } \frac{di}{dt} < 0 \text{ then } V_a = 0 \quad (5\text{-}5)$$

$$\text{If } i \ge i_{up} \text{ then } V_a = 0 \quad (5\text{-}6)$$

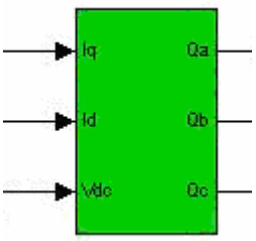


Figure 5-12: The block diagram of hysteresis PWM system

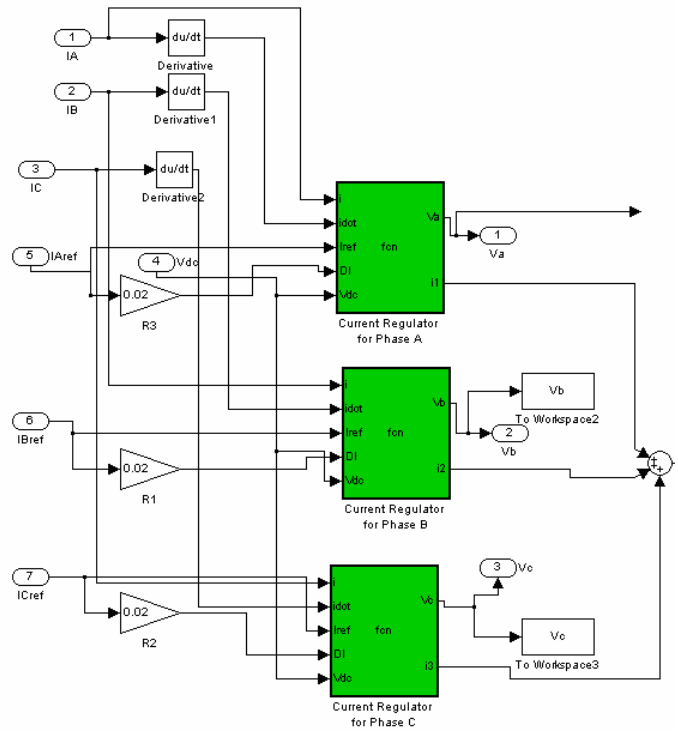


Figure 5-13: Block diagram of current regulator

A special function was written for current regulation as MATLAB file (see Appendix A). Referring to lower and higher values of current, the inverter produces voltages of $+V_{dc}$ or $-V_{dc}$. The error tolerance (δ) is given as 2% in order to have a better regulation results.

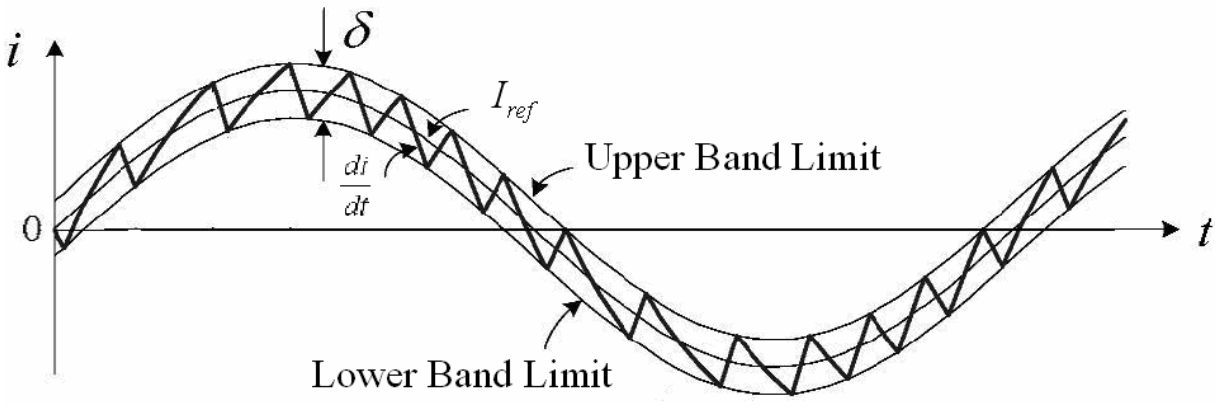


Figure 5-14: Tolerance and band current controller [76]

The disadvantage of the hysteresis current controller is that the switching frequency is dependent on the motor parameters, speed and dc bus voltage.

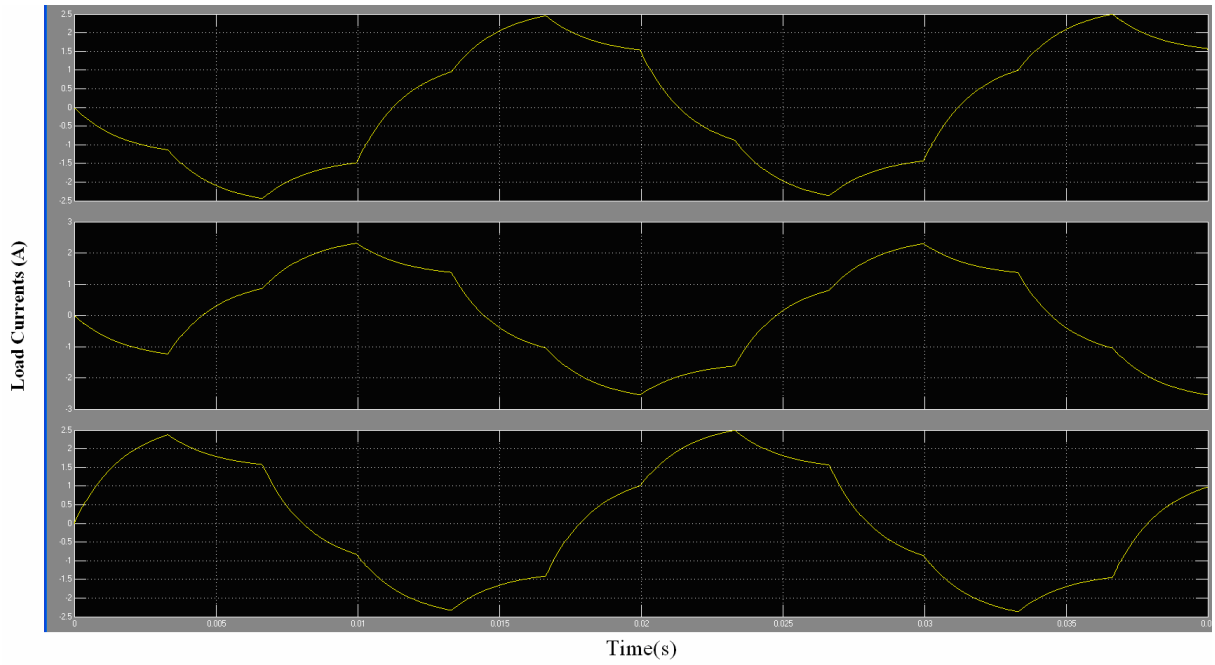


Figure 5-15: Load currents

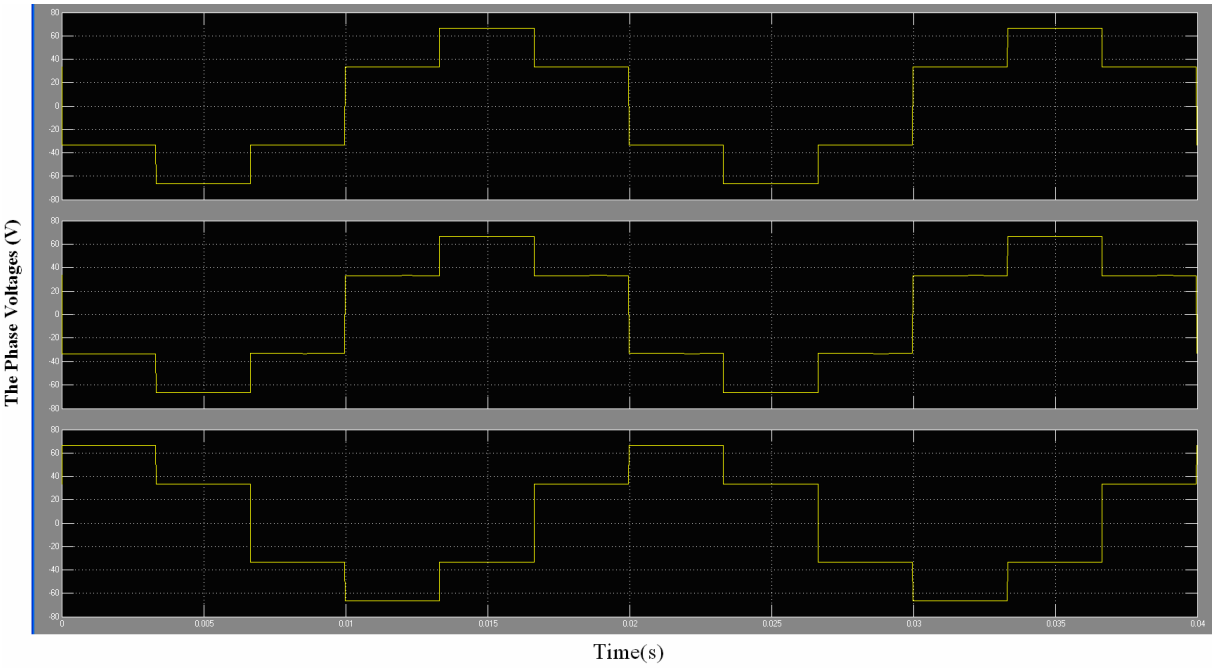


Figure 5-16: Phase voltages of motor side

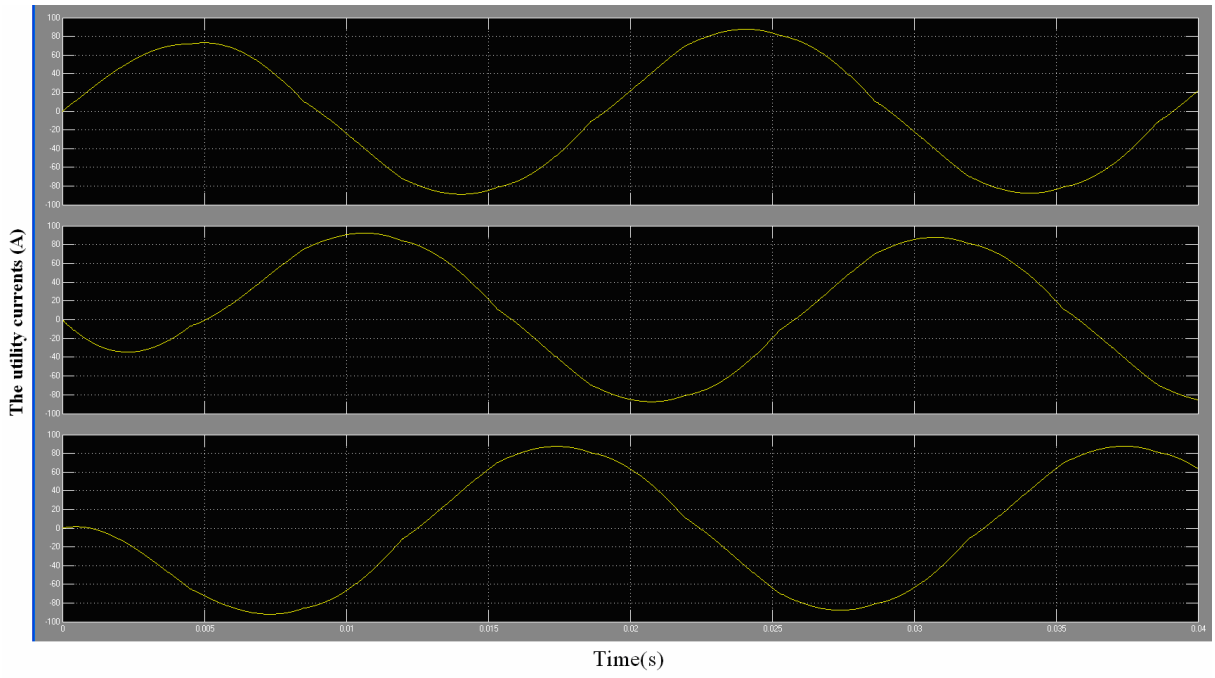


Figure 5-17: Utility currents

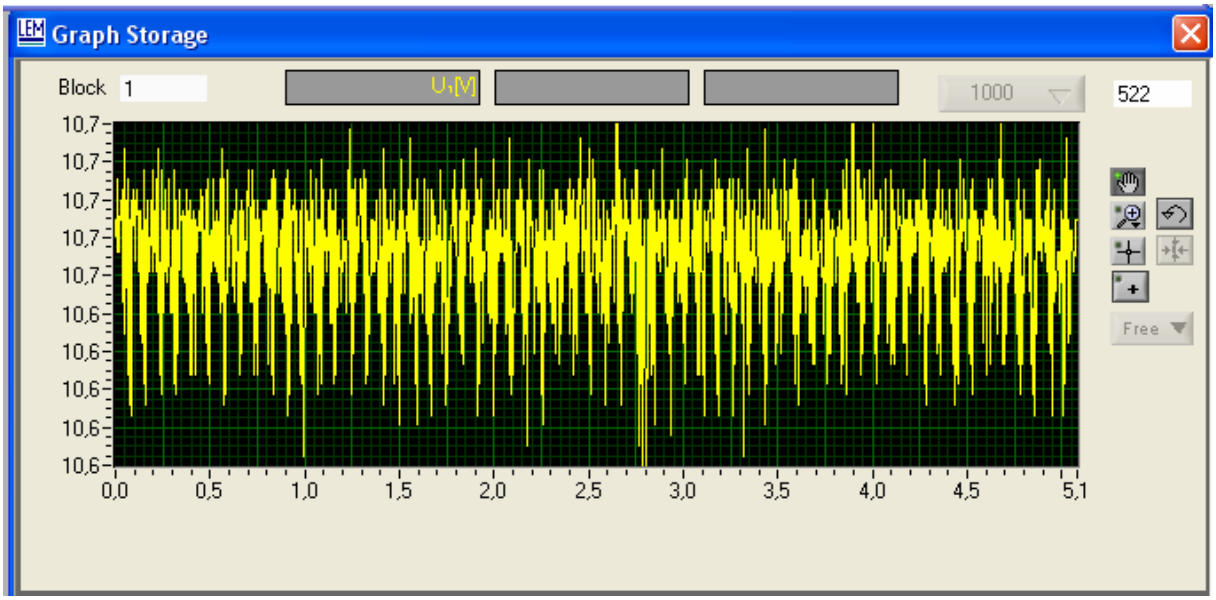


Figure 5-18: DC bus voltage

A detailed SIMULINK model for a PMSM drive system has being developed and operation below and above rated speed have been studied using hysteresis control schemes.

Hysteresis current controllers have a variable switching frequency that depends on the hysteresis band and if the bandwidth is very small it may affect the device switching capability. However, the simulation with hysteresis current controller allows faster

simulations with reduced time and computational resources. A speed controller has been designed successfully for closed loop operation of the PMSM drive system so that the motor runs at the commanded or reference speed. The simulated system has a fast response with practically zero steady state error thus validating the design method of the speed controller.

5.2.3 Rectifier Models

To simplify the simulations, all the MOSFETS (SPP20N60C3) are considered to be ideal, i.e. without any on state voltage drops, reverse recovery behaviour or power losses [68][94][124].

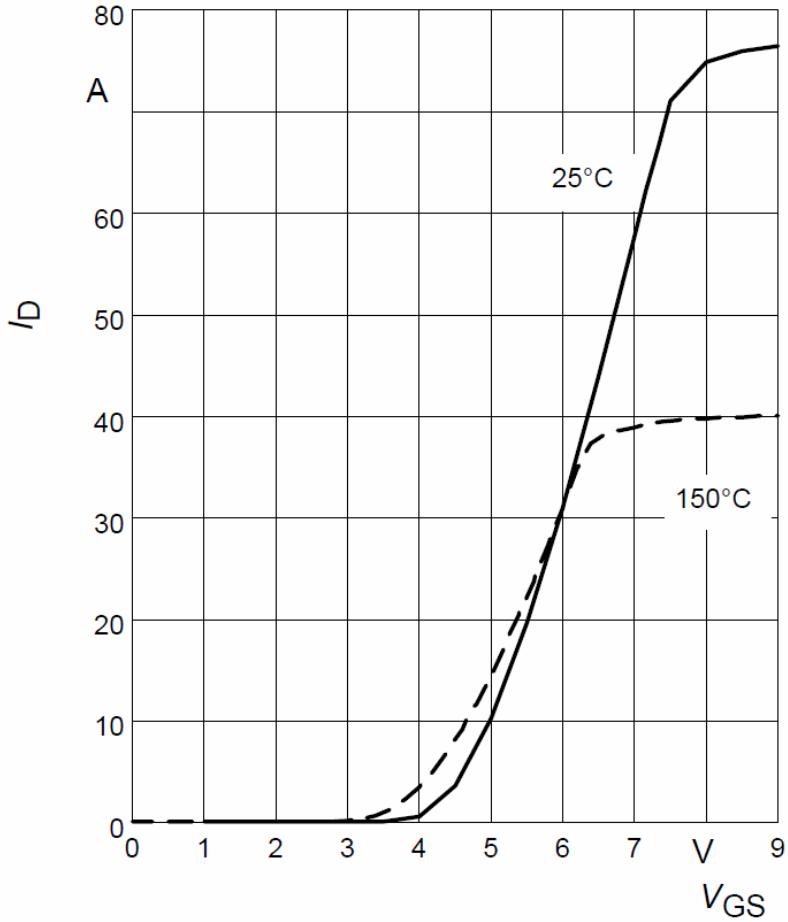


Figure 5-19: Voltage and current characteristics MOSFETS (SPP20N60C3)

5.2.4 DC Link Capacitor Models

Since that the wind turbine and generator side converter are not the main issue for this project the modified layout of the modelling system can be seen again in figure 5-21 where it represents the plant model which is composed of the off-grid side inverter fed by the DC link and connected to the load by means of a transformer [54][66].

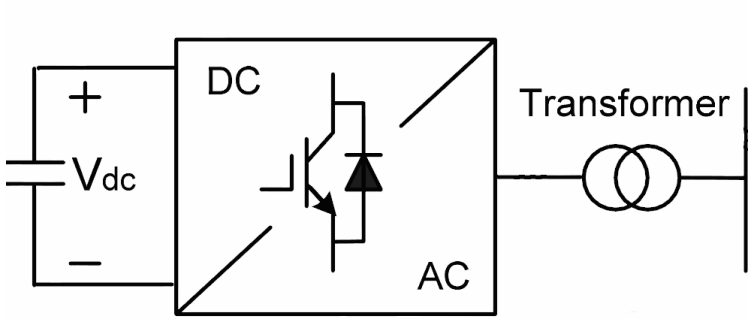


Figure 5-20: Layout of the system

Different criteria are given in the literature for the dimensioning of the dc link capacitor. Design criteria like dc link voltage ripple and dc link capacitor storage energy play important roles in sizing the dc link capacitor and they are therefore examined in this thesis in order to choose the most suitable amount and size of dc link capacitors [83].

The sum of the voltage ratings of the dc link capacitors must be greater than or equal to the overall dc link voltage [18][98]. The design factor in this case would include the dc link voltage ripple to maintain the capacitors within their safe operating range. To evaluate the converter topologies for a variety of applications, carrier frequencies of f_c = 4 kHz…20 kHz are assumed. This range is typical for available industrial medium voltage drives.

5.2.5 DC Link Voltage

The minimum dc link voltage $U_{dc,\min}$ to achieve a certain line-to-line output voltage for our idealized conditions (without any voltage drops on switches and other passive components) topology is calculated by

$$U_{dc,\min} = \sqrt{2} \times U_{primary,rms} \tag{5-7}$$

in case of $t_{\min,on} = 0$ but in practical it is not equal to zero.
To determine the nominal dc link voltage of the converter $U_{dc,n}$ a control voltage reserve of 5% is assumed, which is needed for dynamic processes and filter voltage drops.

$$U_{dc,n} = 1.05 \times U_{dc.\min} \tag{5-8}$$

where $U_{dc,n}$ is the nominal dc link voltage of H-bridge.

$$U_{phase,rms} = N.U_{\sec ondary,rms} \tag{5-9}$$

where N is the turn-ratio of transformer.

Due to the circuit structure of the SC2LHB VSCs, the minimum dc link voltage of one H-bridge $U_{dc,HB}$ depends on the number of series connected transformers M.

$$U_{dc,n} = \frac{\sqrt{2}.M.U_{phase,rms}}{7} \tag{5-10}$$

To evaluate the harmonic spectrum of the line-to-line output voltage, the weighted total harmonic distortion (*WTHD*) is being considered.

$$WTHD = \frac{\sqrt{\sum_{h=2}^{\infty}\left(\frac{U_{ll,h}}{h}\right)^2}}{U_{ll,1}} \tag{5-11}$$

where *h* denotes the order of harmonics. The weighted total harmonic distortion is a measure of the harmonic content for the output current and the harmonic losses in the load.

5.3 Design Criteria and Converter Data

This chapter defines the design criteria and technical data of the typical available medium voltage drives which will be compared in detail in chapter 6. The design process of a power converter depends on the topology and the converter specifications including line-to-neutral voltage $U_{\ln,rms}$, phase current $I_{ph,rms}$, and the apparent inverter output power S_C, which have a critical influence on the overall characteristics, performance, and cost of any design.

5.3.1 Power Semiconductor Devices

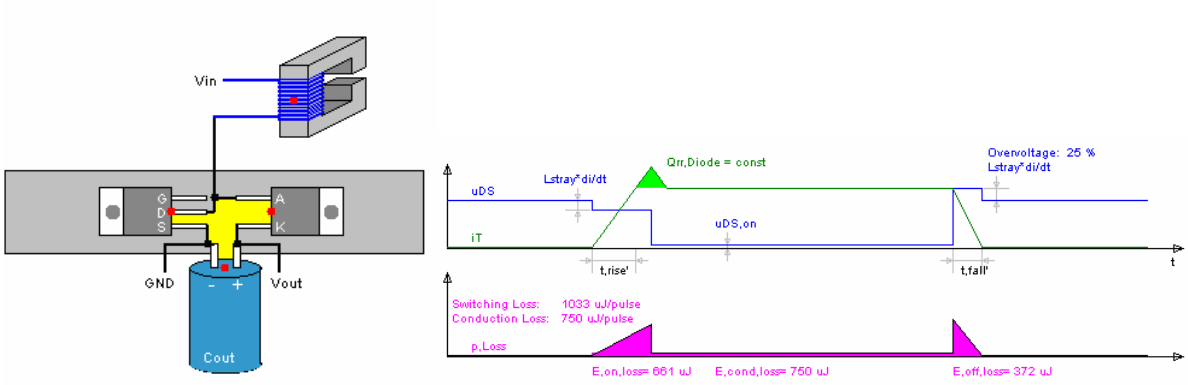
The selection of power semiconductors fundamentally determines the design and the performance as well as the investment and operating costs of power converters. IGBTs are usually used as power semiconductors in medium and high power applications, due to their technical advantages. For the low power applications, MOSFETs will be used to test the high operating frequencies due to less ΔU ($U_{ds,on}$, $P_{loss,switching}$).

Table 5-1 Ratings and specifications of MOSFET type SPP20N60C3

V_{DS} (V)	I_D (at 25°C) (A)	Pulsed drain current (A)	t_r (ns)	t_f max. (ns)	Power dissipation (at 25°C) (W)
650	20.7	62.1	5	4.5	34.5

V_{DS} =drain-source voltage; I_D (contstant at 25°C) = drain current (flowing continuously at 25°C); I_{DM} = maximum drain pulsed current; t_r = rise time; t_f = maximum fall time.

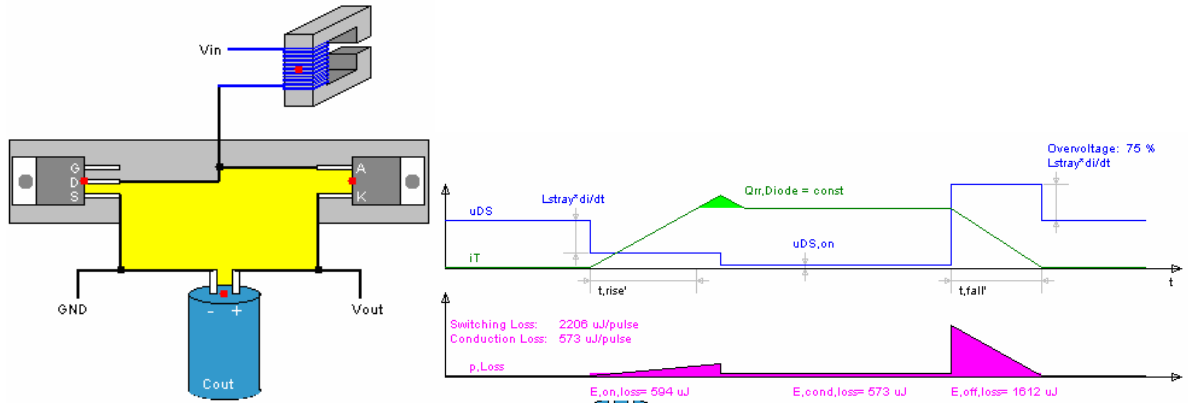
5.3.2 Influence of Wiring Inductance on Switching Losses



(a) (b)

Figure 5-21: (a) Approximated drain-source voltage and drain current during MOSFET turn-on and turn-off for a small area. (b) The approximated switching losses at every time instant [60]

In order to estimate inverter losses, the data of the switching devices, i.e., MOSFET and anti-parallel diode are considered. Inverter losses are also divided into two categories, i.e., conduction loss and switching loss in both the devices. Conduction loss is calculated using the actual currents flowing through the MOSFET and anti-parallel diodes during the conduction period of the devices.



(a) (b)

Figure 5-22: (a) Approximated drain-source voltage and drain current during MOSFET turn-on and turn-off for a large area (b) The approximated switching losses at every time instant [60]

Switching loss is estimated from the inverter full load conditions and for fixed switching frequency of 1 kHz. Switching loss comprises of MOSFET turn-on plus turnoff losses and diode reverse recovery loss. Loss estimation is done for single cell only and the total estimation is obtained by multiplication with the number of cascaded units. This is the

advantage of the proposed switching scheme for the cascaded transformer topology as the power is distributed (first inverter (20 kHz), second inverter (250 Hz), third inverter (50 Hz)) and all the units are stressed differently.

In figure 5-22 and 5-23 approximated switching characteristics shown for a MOSFET when a low gate resistance has been used. The upper diagram depicts the drain-source voltage and the drain current during a MOSFET turn-on and turn-off, and the lower diagram depicts the instantaneous values of the power losses, which are obtained by multiplying the instantaneous value for the drain-source voltage with the instantaneous value of the drain current. The integral of the lower diagram will give the total energy loss during one switching period. In order to get the total switching losses, the total energy losses should be multiplied by the switching frequency.

As mentioned above, an increase in the gate resistance implies an increase in the turn-on and turn-off times of the MOSFET since the time derivatives of the drain-source voltage and the drain current increases. Also, there is an increase in the power losses when a higher gate resistance is employed. This implies that when choosing the method with a higher gate resistance, there must be a careful consideration where the switching losses and increase in temperature are considered against the profits gained in the emission spectrum.

Table 5-2 Losses of two configurations of designs

Losses	Area cm^2	Switching μJ	Conduction μJ	E_{ON} μJ	E_{OFF} μJ
Figure 5-22	**3.5**	**1033**	**750**	**661**	**372**
Figure 5-23	**26**	**2206**	**573**	**594**	**1612**
Ratio	**7.42**	**2.13**	**0.764**	**0.764**	**4.33**

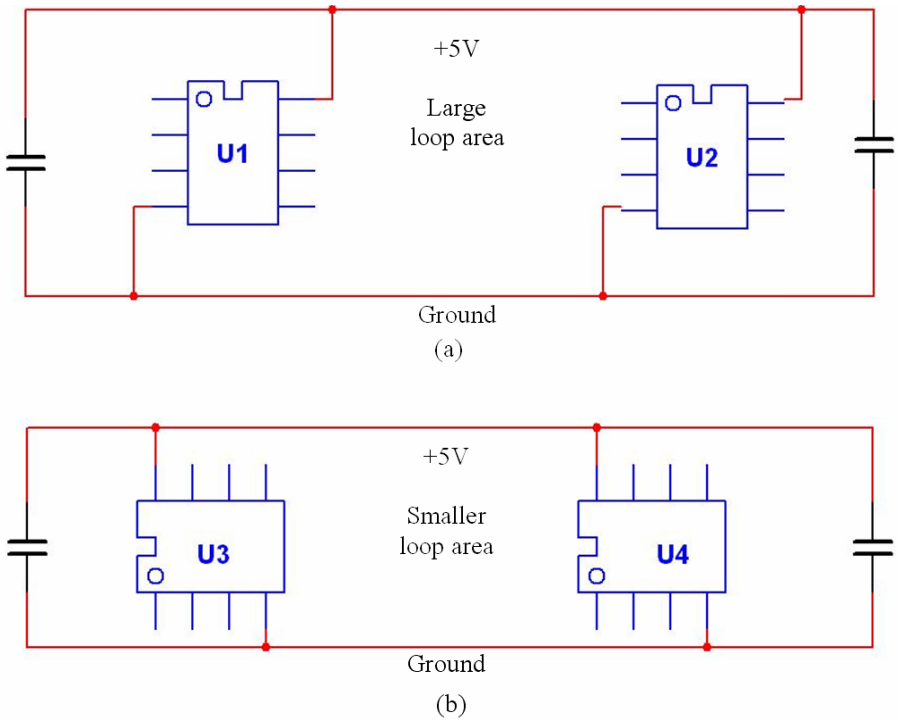


Figure 5-23: Current path causing noise emission

Preservation of the waveform along the cable path in reflection (capacitive and inductive loads), supply voltage fluctuations (transients), ground potential variation (voltage drops across the inductance of the ground line) may therefore be required in an analogous circuit as single-point ground connection [41]. For digital circuits, multi-point grounding system is generally necessary. Although shielding is an effective way of protecting against unwanted noise, the best way to protect against magnetic fields is to decrease the loop area. Considering ground as a low impedance path for current to return to the source emphasizes the importance of current flow in the ground system. The current concept of a ground is also useful in determining the proper power supply and decoupling capacitor connections.

5.4 Isolation Transformer Model

A simple model for a one-phase, two winding transformer with a three-legged iron-core is proposed in reference [47]. The estimation of transformer saturation characteristics is realized from inrush test and no-load test, and the non-linear function that represents the iron core saturation is measured [85].

Figure 5-24: Single-phase, 220V, 200VA, 50-Hz transformer

Table 5-3 Ratings and specifications of used transformers

Nominal Voltage:
Primary side (220V) and secondary side (24V)
Windings:
Primary 1 x 547 turns secondary 1 x 66 turns
Core Type:
ES 200/B

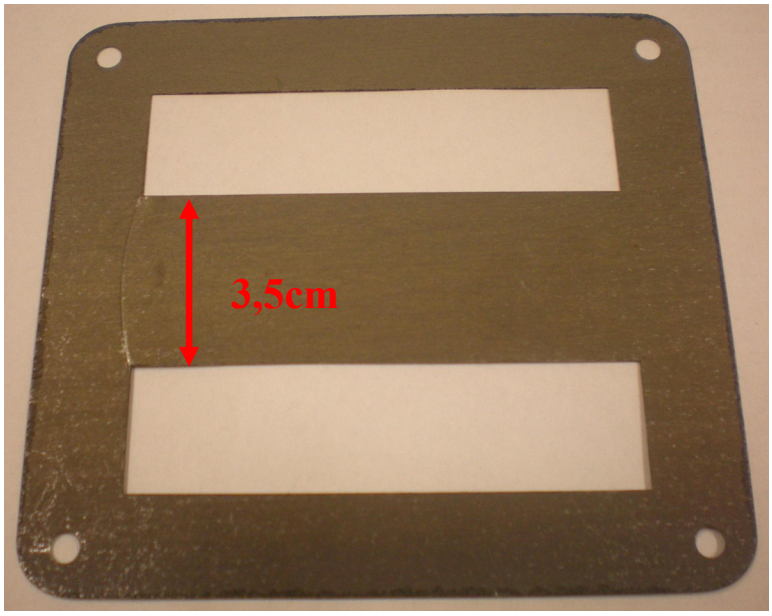


Figure 5-25: Photo of EI lamination

The area of iron core is

$$A_{fe} = 3.5cmx5.2cm = 18.12cm^2 = 18.12x10^{-4}m^2 \quad (5\text{-}12)$$

Standard tests usually do not drive transformer cores into deep saturation and may lead to large errors in the estimation of the nonlinear behaviour of the saturated reluctances, affecting significantly the estimation of transformer inrush currents. From this point of view, it will be important to ensure the stability of the whole system, testing each of the transformers separately.

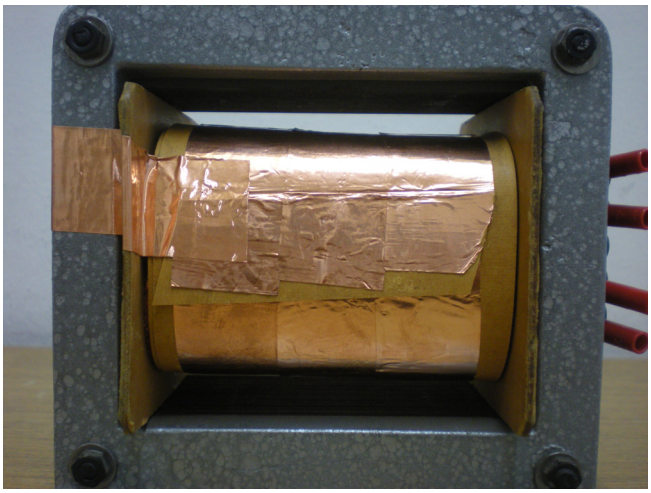


Figure 5-26: Transformer used in circuit

Table 5-4 Stray capacity of the secondary side of transformer

	with PE		without PE	
f	U_2	C_2	U_2	C_2
Hz	**mV**	**nF**	**mV**	**nF**
50	681	37.41	697	19.64
100	687	18.45	686	10.56
200	690	8.88	690	5.00
500	690	3.65	690	2.07
1000	688	1.89	687	1.08
2000	688	0.98	687	0.63
5000	687	0.56	687	0.40
10000	687	0.45	687	0.36
20000	686	0.41	686	0.34
50000	681	0.33	681	0.30

We use the transformer's leakage reactance as filter element without additional cost, and insert a shielding turn for improving high frequency filter properties. The isolation layer is bounded and further new primary (30 turns) and secondary (27 turns) windings are wounded. Fortunately, the new windings (57 windings), which are earthed, increase stray inductance and through ground capacity while reducing coupling capacity and by this way the re-

designed transformer exhibits better output power quality on reduction of THD improving a short way to earth for high frequencies.

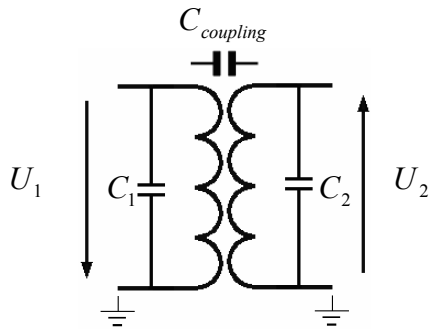


Figure 5-27: Leakage and coupling reactance of transformer

Table 5-5 Coupling and stray capacity of the transformer

	with PE		without PE	
	120	1	120	1
f	Hz	kHz	Hz	kHz
$C_{coupling}$ [pF]	720	634	740	637
C_1 [pF]	220	199	200	177
C_2 [pF]	18.45	1.89	10.56	1.08

The shielding of transformer between windings is used to decrease the unwanted signals and to increase the stray capacitance of transformers. It allows us to have a system without additional and external components filter. Using a suitable and given right length of cable will also act as a filter, reducing the whole costs and increasing the reliability [12]. The primary side capacity is measured by shorting the secondary pins of the transformer (the secondary voltage equals zero) and applying a measurement voltage from this connection to ground. The same procedure is done to measure the secondary side capacity.

The transformer windings are producing a small capacity to ground. The winding inductance and capacity are specifying the resonance frequency.

5.4.1 Single-Phase Transformer Model

The equivalent electric circuit of single-phase transformer for operating grid frequency is shown in figure 5-28, where R_p, R_s, X_p, X_s are the winding resistances and assumed being constant leakage inductances; the shunt resistance R_c accounts for the core-losses.

The equations of the single-phase transformer using the core fluxes linked by the primary windings $N_p\phi = \lambda_p$ are

$$V_p = (R_p + X_p \frac{d}{dt})i_p + \frac{d\lambda_p}{dt} \quad (5\text{-}13)$$

$$V_s = (R_s + X_s \frac{d}{dt})i_s + \frac{1}{r_{t,w}} \frac{d\lambda_p}{dt} \quad (5\text{-}14)$$

where N is the winding turn ratio ($N = N_p / N_s$), which is measurable in the laboratory.

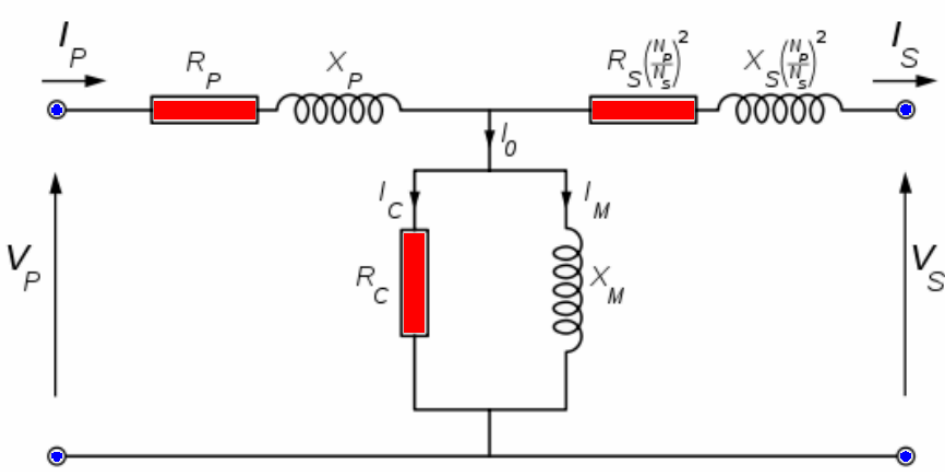


Figure 5-28: Electric equivalent circuit of a single-phase transformer model referred to the primary voltage level

The winding ratio was measured using a tertiary winding with a known number of turns. After applying a voltage to the primary winding and measuring the voltage at the tertiary winding, the number of turns in the primary winding was calculated. The turns in the secondary winding were calculated in a similar way. Finally, the winding ratio thus obtained was tested with the relation between the voltage in the primary winding and the voltage induced in the secondary winding.

The flux and the current are expressed in p.u., being the base values for the 200-VA single-phase transformer, $U_{1b} = 220V$ and $U_{2b} = 24V$.

Table 5-6 Parameters of each transformer

	S	I_{fe}	$I\mu$	R_{fe}	X_h	R_S	X_S	$R_1 = R_2 = R_{S/2}$	$X_1 = X_2 = X_{S/2}$	$[Z] = \frac{U_S}{I_1}$	$Cos\varphi_0$
	VA	**A**	**A**	Ω	Ω	Ω	Ω	Ω	Ω	Ω	°
TR1	200	0.08	0.12	2734	1899.94	14.58	2.08	7.29	1.04	14.73	0.57
TR2	200	0.05	0.12	4566	1889.65	13.55	1.93	6.77	0.97	13.68	0.38
TR3	200	0.06	0.09	3551	2388.68	15.07	3.06	7.54	1.53	15.38	0.55
TR4	200	0.05	0.11	4667	2054.45	13.92	1.98	6.96	0.99	14.06	0.39
TR5	200	0.05	0.10	4685	2314.99	13.98	1.99	6.99	1.00	14.12	0.43
TR6	200	0.05	0.11	4601	2039.36	15.28	2.18	7.64	1.09	15.43	0.40
TR7	200	0.06	0.09	3601	2343.62	15.19	3.08	7.59	1.54	15.50	0.54

Table 5-7 Short-circuit- and no-load measurements of each transformer

	U_2	I_o	I_s	U_S	P_0	P_s	R_1	R_2	$R_1(p.u)$	$L_1(p.u)$	$R_m(p.u)$	$L_m(p.u)$
	V	**A**	**A**	**%**	**W**	**W**	Ω	Ω	-	-	-	-
TR1	23.6	0.14	0.88	6.09	17.70	11.81	7.50	0.65	0.030	0.0042	11.29	7.85
TR2	26.6	0.13	0.91	5.65	10.60	11.27	5.78	0.70	0.027	0.0039	18.86	7.80
TR3	26.6	0.11	0.90	6.35	13.63	12.50	6.77	0.67	0.031	0.0063	14.67	9.87
TR4	26.7	0.12	0.92	5.81	10.37	11.75	6.57	0.70	0.028	0.0040	19.28	8.48
TR5	26.6	0.11	0.91	5.84	10.33	11.65	6.51	0.88	0.028	0.0041	19.36	9.56
TR6	26.7	0.12	0.92	6.38	10.52	12.94	6.78	0.72	0.031	0.0044	19.01	8.42
TR7	26	0.11	0.91	6.40	13.44	12.73	7.56	0.80	0.031	0.0063	14.88	9.68

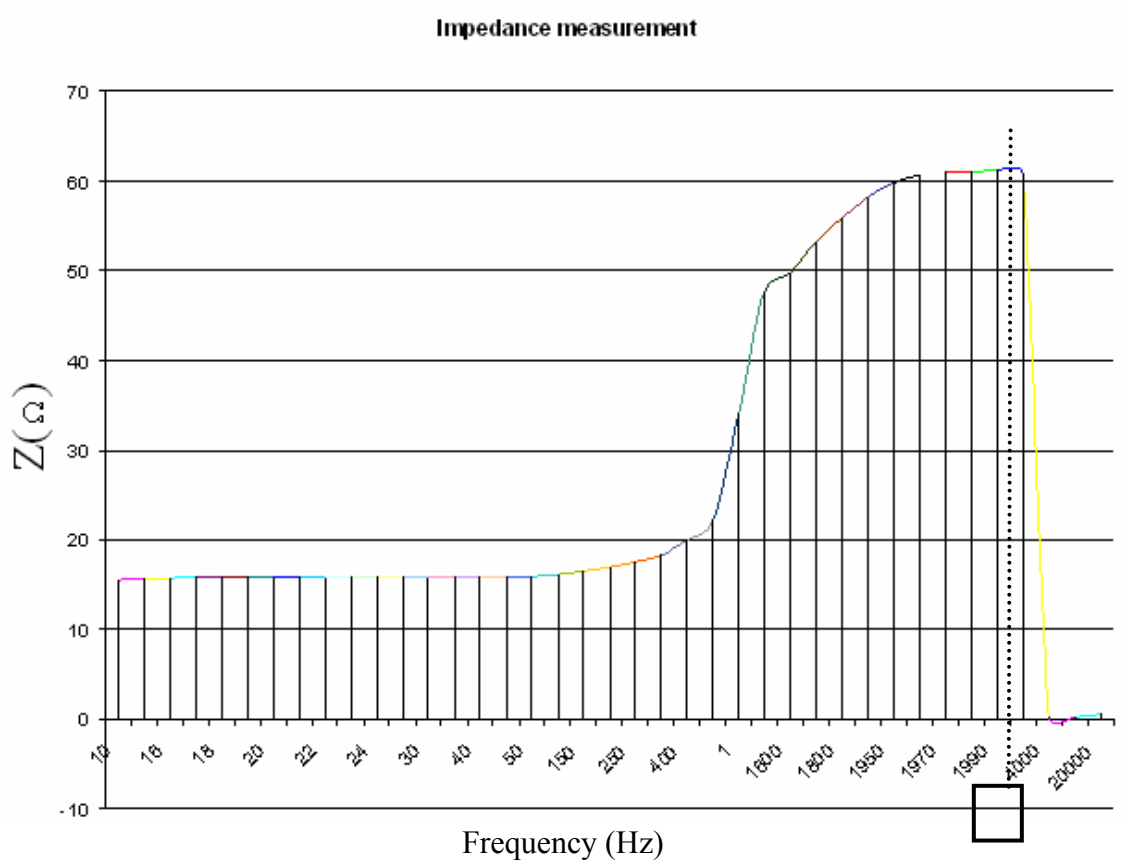
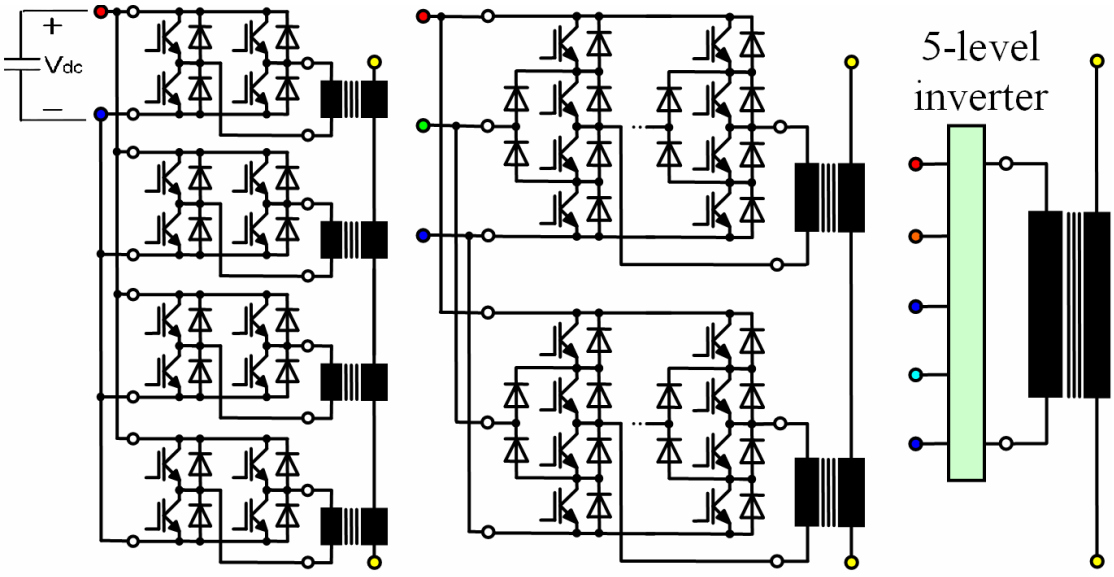


Figure 5-29: The chart shows a magnitude peak of the short-circuit impedance close to 1990 Hz (dashed line). The impedance at the resonance frequency is 61.18 Ω

Figure 5-30: 24V secondary windings



(a) 4 transformers (b) 2 transformers c) 1 transformer

Figure 5-31: 5-level systems with transformer(s) [129]

All circuits from figure 5-31 have 4 steps (in push-pull configuration, between zero and positive maximum) according to a 5-level-system as we can set-up the output voltage through 5 levels (including level 0). All circuits employ the same number 16 of individual switches, too.

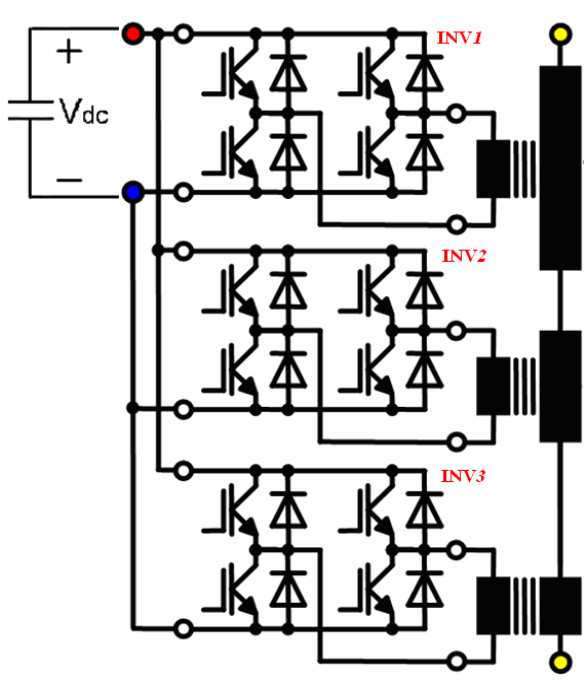


Figure 5-32: Quasi-eight-level system with adapted transformers [129]

Table 5-8 Multilevel system overview [129]

Number of levels	Basic inverter circuit, corresponding figure	Number of basic inverter	Total number of individual switches	Step size in % of peak voltage
5	2-level, fig. 5-32 (a)	4	16	25.0%
5	3-level, fig. 5-32 (b)	2	16	25.0%
5	5-level, fig. 5-32 (c)	1	16	25.0%
7	7-level	1	24	16.7%
9	9-level	1	32	12.5%
quasi-8	**2-level, fig. 5-33**	**3**	**12**	**14.1%**

Directly visible in figure 5-32, we build the total output voltage by a binary weighted sum of the individual 2-level inverter voltages. Third inverter has to contribute 4 times the voltage and hence also 4 times the apparent power as the first inverter. Second inverter has to contribute 2 times the voltage and hence also 2 times the apparent power as the first inverter.

5.5 Load Model

The load model is seen for a village for single-phase that consists of 22 buildings and 1 school. The energy injected form wind generator or photovoltaic is transferred via transformer and cables. It is assumed to be series resistive-inductive load.

5.5.1 Cable Model

The frequency response of the LCL filter was measured using a network analyzer. The applied sinusoidal signal of $2V_{p-p}$ was swept from 50 Hz to 50 kHz with frequency values in this range. For each frequency, the standard model comprises an infinite number of *LC* pairs.

Figure 5-33: Load and supply area model

The diameter of the supplied area is $2.\pi.r = 263m$. This is the necessary parameter of dimensioning the length of cable. Reducing the costs depends on the exactly measured parameters and filtering of the harmonics in a system. When filtering as closely as possible to the point of generation of the harmonics, one can be sure that filtering remains effective during the many mutations that typically occur in office buildings. The disadvantage is that more filter capacity is provided than is actually required and the individual small filters are more expensive than a centralised one [118] [127]. One benefit is that harmonic currents are limited to a smaller area of the installation. On the other hand, a centralised approach allows the combination of passive filters with power factor correction equipment. Designing these functions together allows steps to be taken to avoid resonance at harmonic frequencies [97]. Usually, combined power factor correction and filtering equipment is centralised, allowing economy of scale due to diversity, reduction in the amount of control required and the ability to correct to a higher level without the risk of self-exciting motors [99]. However, as the harmonic culture of the load changes steps must be taken to ensure that the filter remains functional.

The equivalent electrical diagram of a cable with the length Δl is shown in figure 5-34. R_l is longitudinal resistance, L_l is longitudinal inductance, C_t transversal capacitance and G_t is transversal conductance.

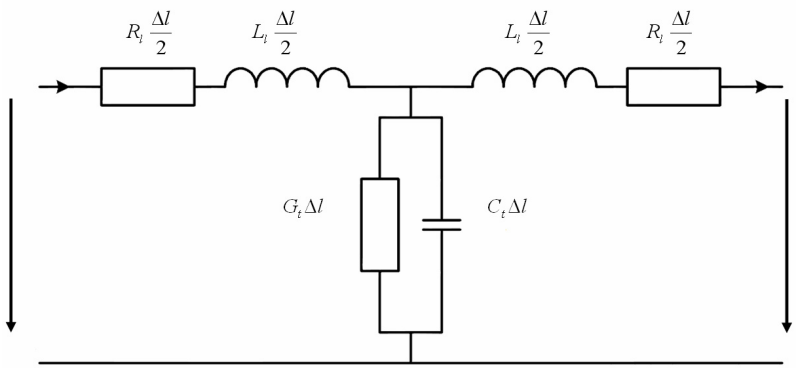


Figure 5-34: Equivalent electrical diagram per phase for a cable with the length, Δl

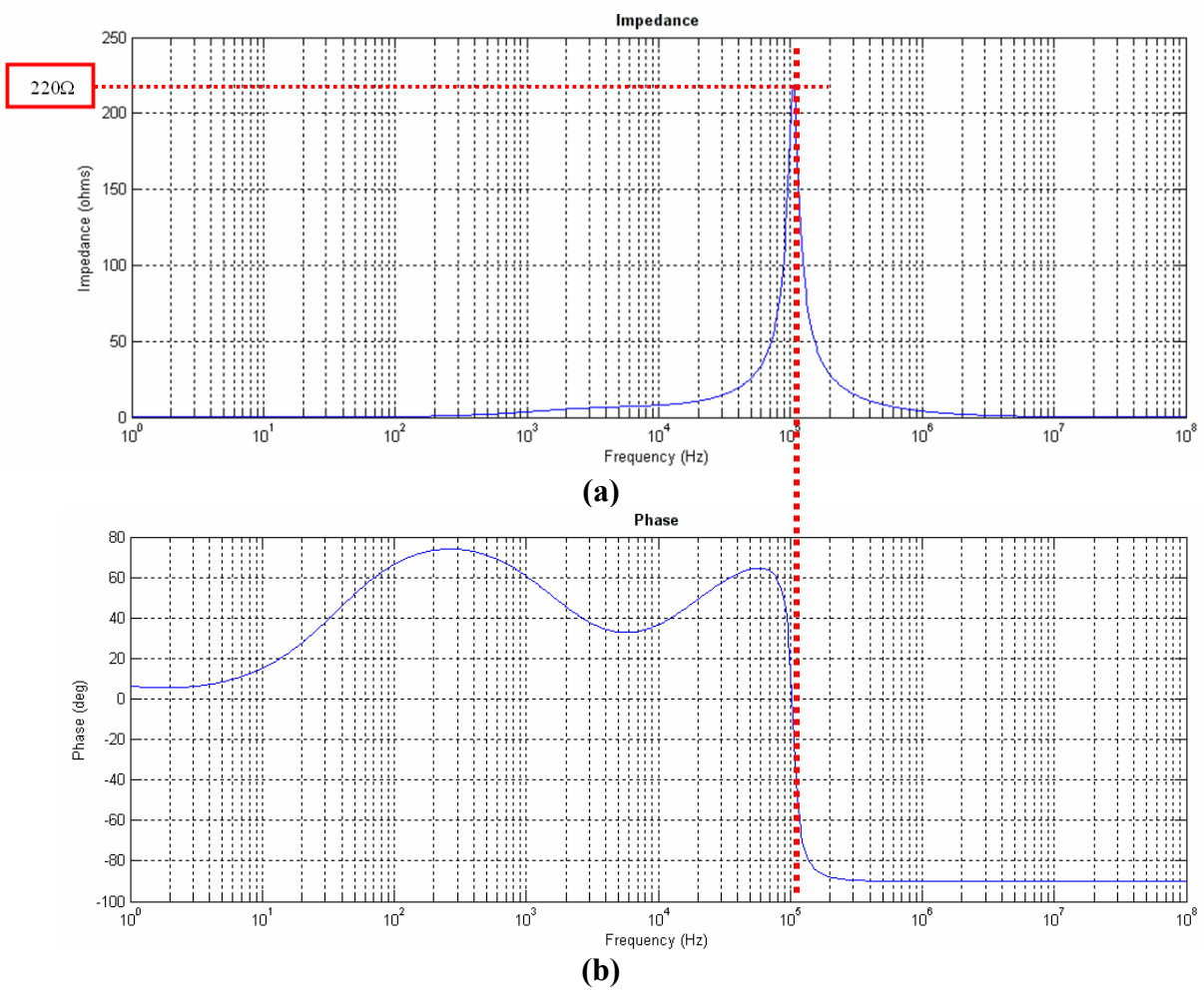
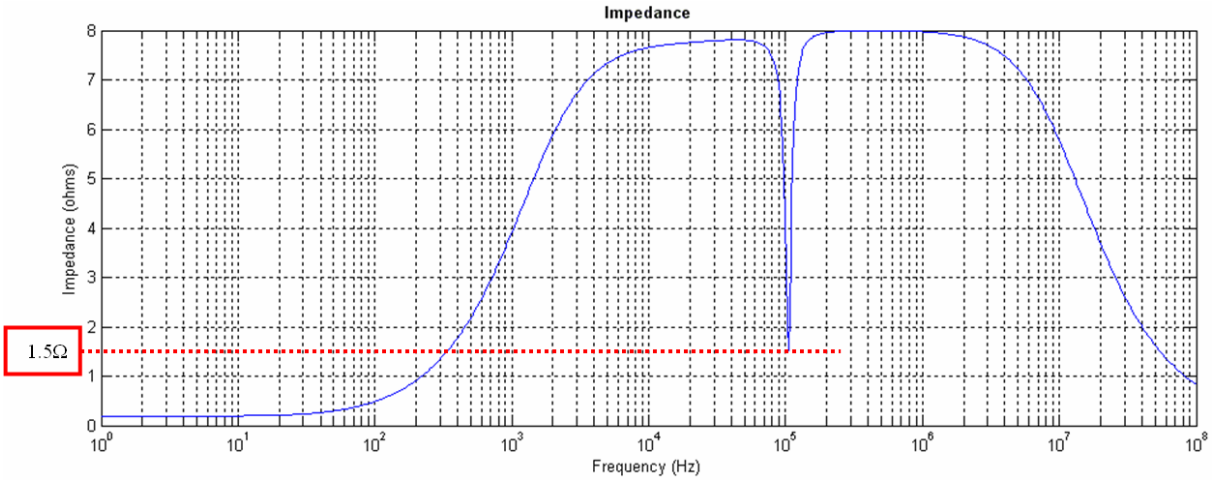
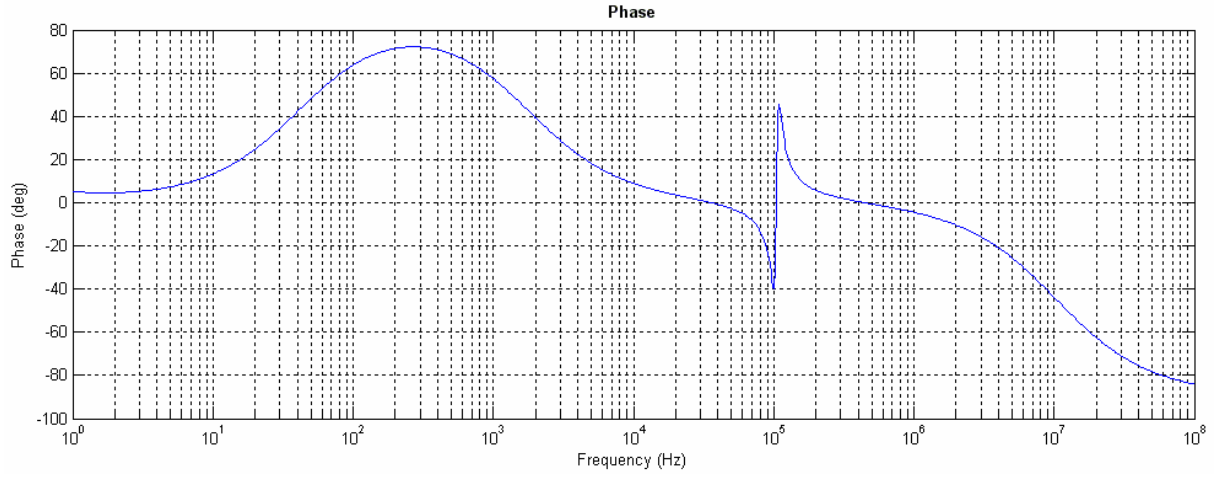


Figure 5-35: (a) Impedance versus frequency at the end of transformer (b) Phase angle of the transformer



(a)



(b)

Figure 5-36: R=0.524 (Ω/km), L=0.9337e-3 (H/km), C=12.74e-9, *l*=150m (F/km) (a) Impedance versus frequency at the end of cable (b) Phase angle of the cable

Modern electronic loads draw harmonic currents, cause harmonic voltage disturbance and impose high frequency noise on the network [74]. As the reactance of a capacitor is inversely proportional to the frequency, these high frequencies can cause the current rating of the capacitor to be exceeded.

The network as seen from figure 5-36 (a) has very low impedance at about 100 kHz frequencies, where the most harmonic generation takes place. The capacitor used in this system will absorb most of the current at this frequency.

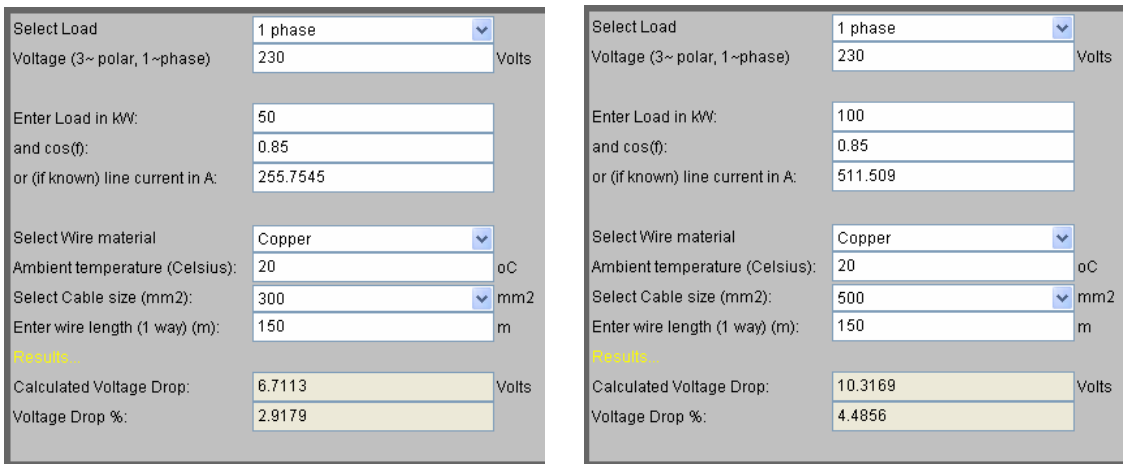


Figure 5-37: Load model [61]

The requirements for the voltage drop are restricted to less than 3% and the value is acceptable.

Table 5-9 Parameters of cable

Resistance per conductor, r	0.08	mW/m
Line current, I	255	A
power factor, cos(φ)	0.85	-
Length, l	150	m
Total power losses, P	0.780	kW
Relative voltage drop (%)	1.56	<0.5%

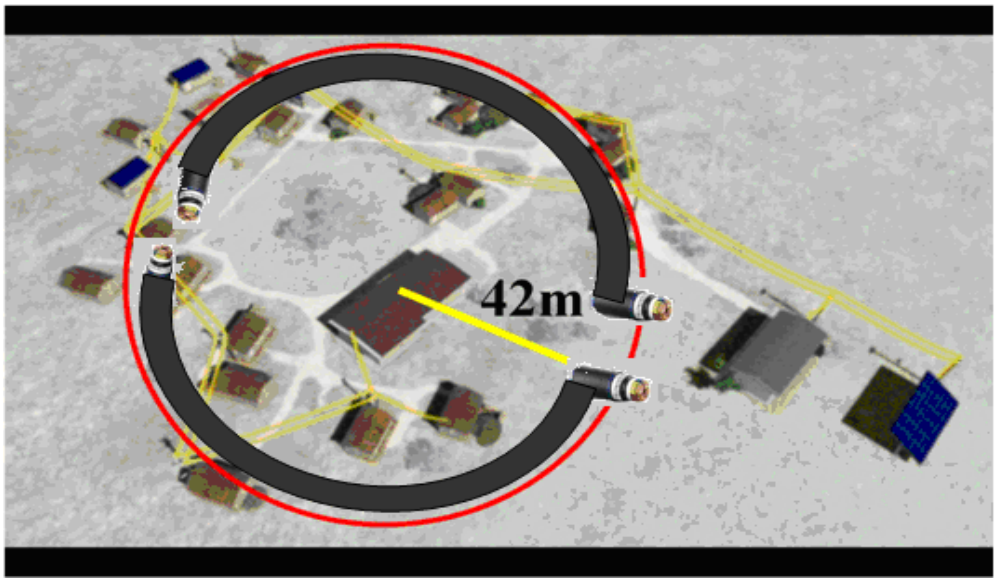


Figure 5-38: Load model

This thesis sets out the minimum requirements for achieving energy efficient design of electrical installations without sacrificing the power quality, safety, health, comfort or productivity of occupants or the building function. The requirements for energy efficient design of electrical installations in this village are classified into the following four categories:

(a) Minimising losses in the power distribution system.
(b) Reduction of losses and energy wastage in the utilisation of electrical power.
(c) Reduction of losses due to power quality problems.
(d) Appropriate metering and monitoring facilities.

The copper loss should be restricted with 0.5% of the total active power transmitted along the circuit conductors at rated circuit current. The cross-sectional area of neutral conductors should not be less than that of the corresponding phase conductors. In any electrical circuit some electrical energy is lost as heat which, if not kept within safe limits, may impair the performance and safety of the system. This energy (copper) loss, which also represents a financial loss over a period of time, is proportional to the effective resistance of the conductor, the square of the current flowing through it and the duration of operational time [100]. A low conductor resistance therefore means a low energy loss. The length of the main distribution circuit conductors connecting the transformer should be as short as possible.
For a 1-phase circuit, the apparent power transmitted along the circuit conductors in VA is:

$$S = U_L I_b \tag{5-16}$$

Active power transmitted along the circuit conductors in W is:

$$P = U_L I_b \cos\varphi \tag{5-17}$$

Total copper losses in conductors in W are:

$$P_{copper} = I_b^2 .r.L \tag{5-18}$$

where U_L line to line voltage, I_h design current of the circuit in ampere $\cos\varphi$ displacement power factor of the circuit, $r = A.C.$ resistance per meter per conductor (2-ways) at the conductor operating temperature, L length of the cable in metre.
Percentage copper loss with respect to the total active power transmitted,

$$e\% = \frac{I_b^2 .r.L}{U_L I_b \cos\theta} \tag{5-19}$$

where e is the loss in percent and indicates the relationship among circuit design current (I_b) and effective current-carrying capacity of conductor (I_z) for an electrical circuit.

The minimum cable size for compliance with the Electricity (Wiring) Regulations is determined as follows:

$$A = \frac{2.P.L}{K.\mathrm{e}\%.\mathrm{U}^2\sqrt{3}} \tag{5-20}$$

$$K = 56\frac{m}{mm^2\Omega} \tag{5-21}$$

This maximum copper loss requirement is deemed to comply with for any 3-phase balanced circuit with linear characteristic, if feeder circuits are designed to the conventional safety requirement of the Electricity (Wiring) Regulations.

The conventional method of cable sizing for 1-phase system can briefly be described as follows:

$$\%e = \frac{2.P.L}{\rho.\mathrm{A}.\mathrm{U}^2} \tag{5-22}$$

For a 1-phase 4-wire circuit, active power transmitted via the circuit conductors,

$$P = U_L I_1 \cos\varphi \tag{5-23}$$

Total copper losses in conductors,

$$P_{copper} = (I_b^2 + I_N^2).r.L \tag{5-24}$$

where U_L line to line voltage is, I_b is design current of the circuit in ampere, I_1 is fundamental current of the circuit in ampere, I_N is neutral current of the circuit in ampere.

Percentage copper loss with respect to the total active power transmitted,

$$\text{relative copper loss}(\%) = \frac{(I_b^2 + I_N^2).r.L}{\mathrm{P}} x100 \tag{5-25}$$

Another problem in this system is the unbalanced power sharing between two parallel cables.

$$S = \sqrt{P^2 + Q^2} \tag{5-26}$$

$$\cos\varphi = \frac{P}{S} \tag{5-27}$$

$$P_{INV} = P_1 + P_2 + ... + P_n \tag{5-28}$$

The instantaneous power gained from the sinusoidal one phase system in steady state is

$$P_{out} = u_{L1} i_{L1} = \hat{u}\sin(\omega_{grid} t).\hat{i}\sin(\omega_{grid} t - \varphi) \tag{5-29}$$

where $\hat{u}$ and $\hat{i}$ indicate the peak values of the phase voltage and current respectively. The angle φ is the phase shift between the voltage and current. If the phases of the line voltage and current are identical, that is $\varphi = 0$, the instantaneous power becomes

$$P_{out} = \hat{u}\hat{i}\sin^2(\omega_{grid}t) \tag{5-30}$$

This indicates that the output power should also fluctuate in a similar way to gain a purely sinusoidal line current behaviour and unity power factor.

$$P_{out} = \frac{u_{\max} i_{\max}}{2}\cos\varphi(1+\cos 2\omega t) + \frac{u_{\max} i_{\max}}{2}\sin\varphi(\sin 2\omega t) \tag{5-31}$$

Problems arise when a small DC-link capacitor is used. The DC-link voltage is by far not constant and fluctuates rapidly. To illustrate the problem an approximate equation for the change of DC link voltage is

$$-i_{INV} = C\frac{du_{DC}}{dt} \tag{5-32}$$

$$\Delta u_{DC} = -\frac{1}{C} i_{INV}\Delta t_{SW} \tag{5-33}$$

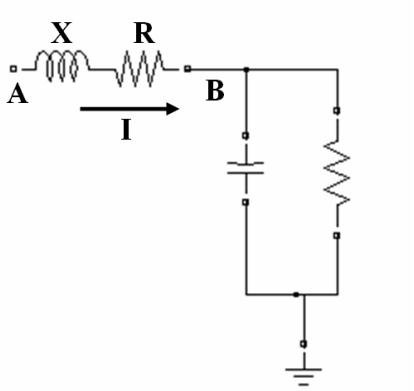


Figure 5-39: Parallel compensation reduces the voltage drop

5.5.2 Shielding

The grounding system must protect electronics by providing a low impedance path to interconnect equipment. High frequency currents can be a bigger problem as far as function is concerned. It will be good ff the noise currents can be transported to earth without producing noise voltage drop. This requires a connection to earth that has low impedance at all frequencies and the path should run close to the supply conductors.

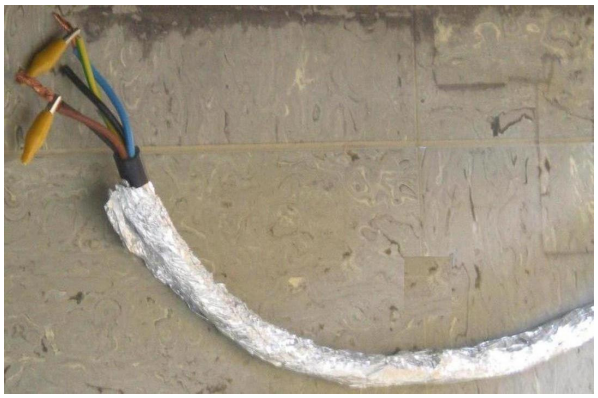


Figure 5-40: Shielded cable

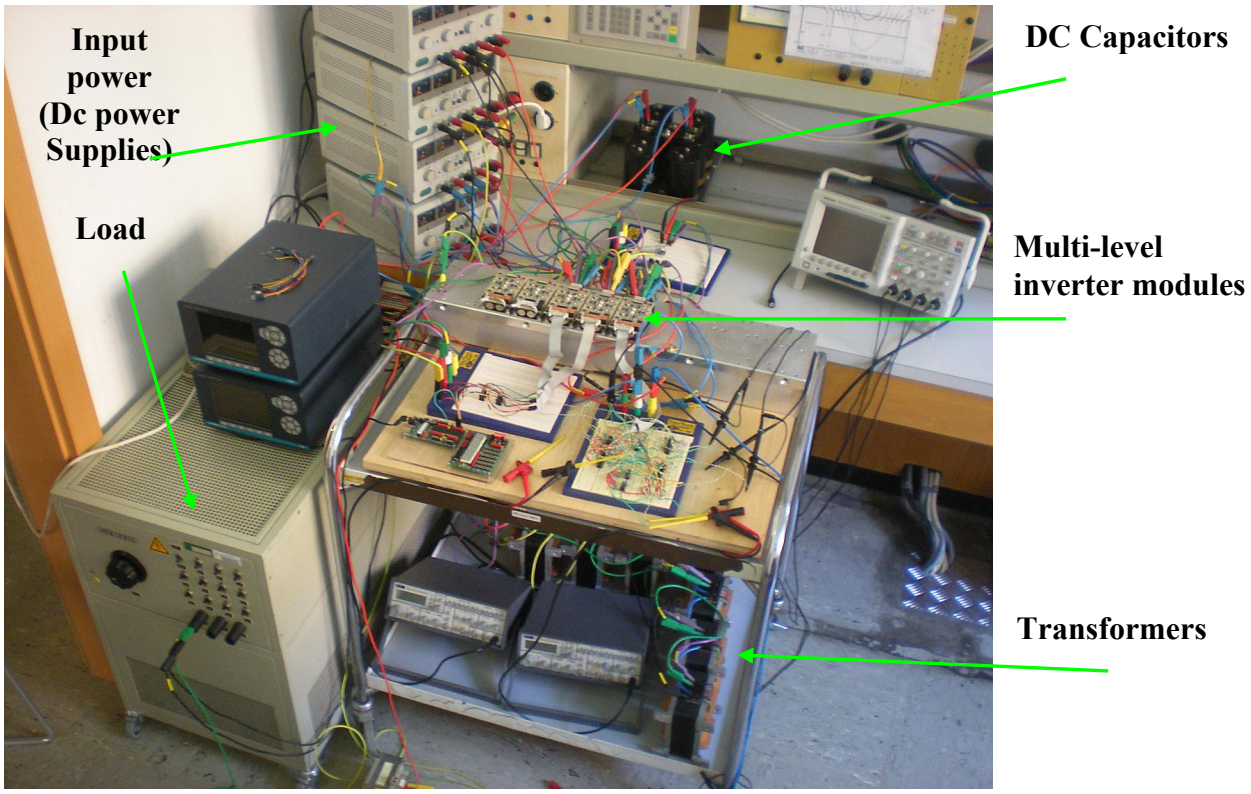


Figure 5-41: (a) Photograph of overall test arrangement

Two battery banks and seven insulation transformers complete the hardware. DSP boards and all the stuff related to the control part of the system control the gate signals of MOSFETs.

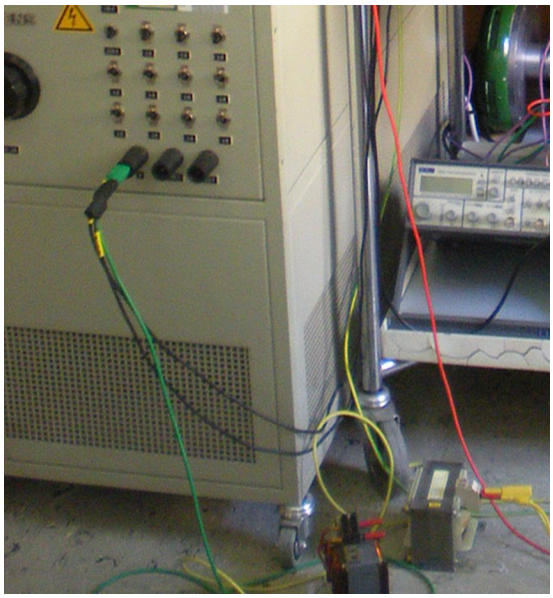


Figure 5-42: Photograph of a resistor and inductor

A 1-phase load has been connected to the converter. The load is composed of a resistor and an inductor connected in series. The resistors and the 1-phase inductor used are shown in figure 5-42. The 1-phase inductor is wound on a metal core. For experimental set-up, different load conditions have been chosen as total resistance and total inductance values.

6 Experimental Layouts

6.1 Control System Hardware Description

6.1.1 Controller Board

The ATmega16 is a low-power CMOS 8-bit microcontroller [111][125]. By executing powerful instructions in a single clock cycle, the ATmega16 achieves throughputs approaching 1 MBPS per MHz of clock frequency allowing the system designer to optimize power consumption versus processing speed. Detailed description of ATmega16 is given in Appendix A.

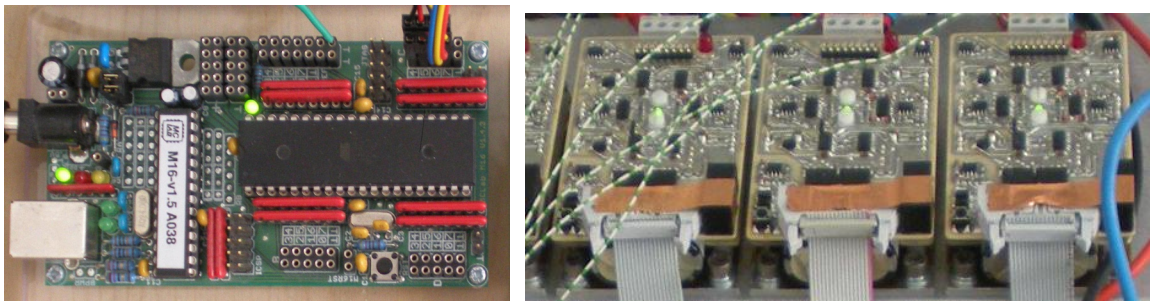
Controller board processes capabilities to implement the control algorithms and fulfil the application requirements [23][55]. It's capable of calculation, storage and timer properties must be also high enough so that the system design has a simple structure in order to increase reliability and has a reasonable cost as a part of the whole system. The controller board is programmable from programme language C and assembler environment. It provides a large selection of interfaces, including 10 bit-I/O channels, 8 A/D channels. A slave-DSP supports the main processor with additional inputs and outputs. The features of microprocessor are detailed described in Appendix A.

2-level inverter system has been implemented, rated for different powers. The full scale converter is rated 30 V DC and 4 A RMS output current. The second and third inverters are built using discrete components: all eight switches are realized by several power MOSFETs in parallel connection [87]. This converter has been implemented using two integrated 1- phase 2-level inverters designed by Wenzel Maier ®. These power modules are rated for 450 V over the DC bus and 10 A as maximum phase current output RMS value: the voltage limits are largely greater than the 48 V effectively applied by battery banks.

The performance of the proposed single-phase two-leg inverter is verified by the computer simulation and experimental results based on a laboratory scaled-down prototype circuit. The system is simulated using the MATLAB/SIMULINK software package to draw the balanced sinusoidal line currents from the ac source [92]. The circuit parameters of the adopted inverter in the simulation are: line voltage= 230 Vrms, line frequency= 50 Hz, r= $15\,\Omega$, L=80 mH and C= $3300\,\mu F$. The dc-link voltage is 300 V. The line current, dc-link voltage and source voltage are measured with current sensors, opt coupler and potential transformer. The line currents are sinusoid in phase with phase voltages.

Programming the μC for the second and third inverter with constant frequency (50 Hz) and amplitude (7 V) is achieved. Writing different frequency values in the heading (#define FREQ 50) of programme, changes the operating frequency of the system, will be shown in Appendix A.

In this chapter all the parts composing the 2-level inverter will be described in detail and analysed. Electrical insulation among first inverter, second inverter, third inverter and control boards are used in this system. A fault in the insulation may critically invalidate the right operation of the converter [107]. The MOSFETs of the pulse inverter are pressed onto a heat sink to improve heat transfer. The important major issues with the power conditioning systems are cost, efficiency, reliability and isolation.



(a) **(b)**

Figure 6-1: Two level inverter implementations. a) Controller board; b) Full scale inverter

In figure 6-1 on the left there are the connectors with the expansion board and microprocessor. These boards are fed by the power sources provided with the input power (DC power supplies). One external power source is needed to feed interface and four for power boards. An external insulated power supply is needed for the circuitry feeding each inverter.

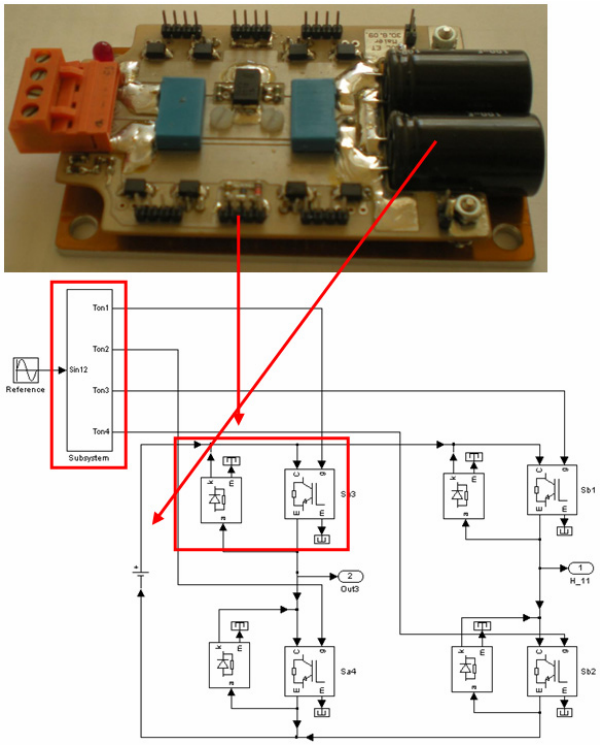


Figure 6-2: Structure of the pulse inverter

It can be seen that the discrete method presented herein relies on computation directly from the duty cycles and therefore it is not necessary to define triangle waveforms or voltage vectors [63]. For this reason, it is preferably to use microprocessors for the second and third inverter control algorithm while sine-triangle modulation is useful in that it can provide a

straightforward method of describing multilevel modulation of synchronization between first inverter and the second and third inverter control system respectively. The rest of the hardware has been limited as much as possible to reduce its cost and as well as to increase the electrical and mechanical reliability.

The simulation is based on the hardware structure to have as accurate results as possible where the parameters of MOSFETs are given into system. The problems seen in workbench actually can not be modelled in simulation and therefore simulation has better measurement results.

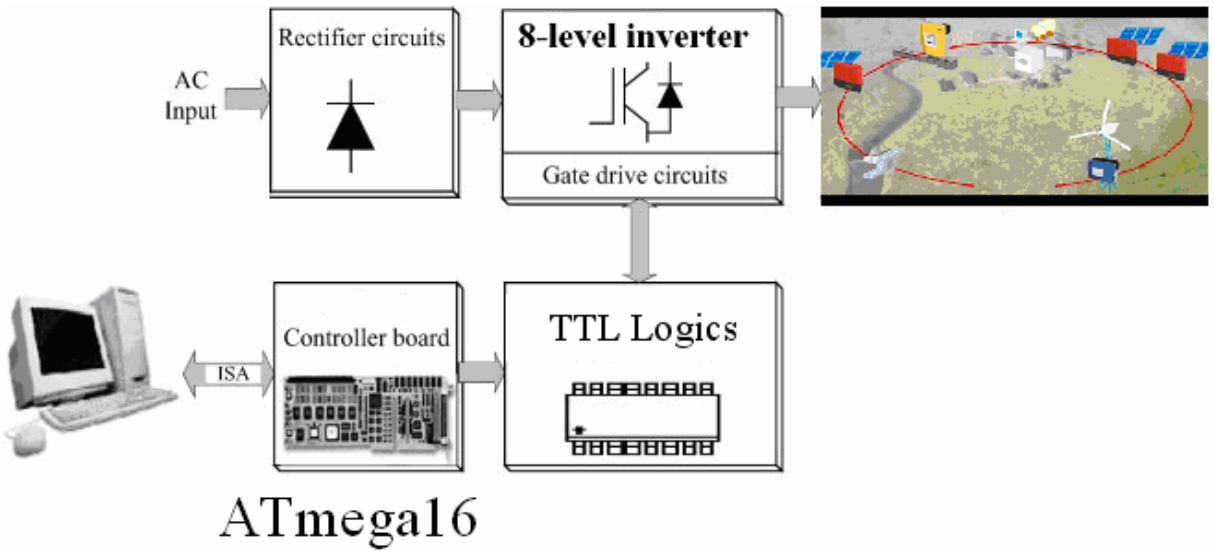


Figure 6-3: Infrastructure of the proposed system design

The implemented system is seen in figure 6-3, where the computer aided system is designed.

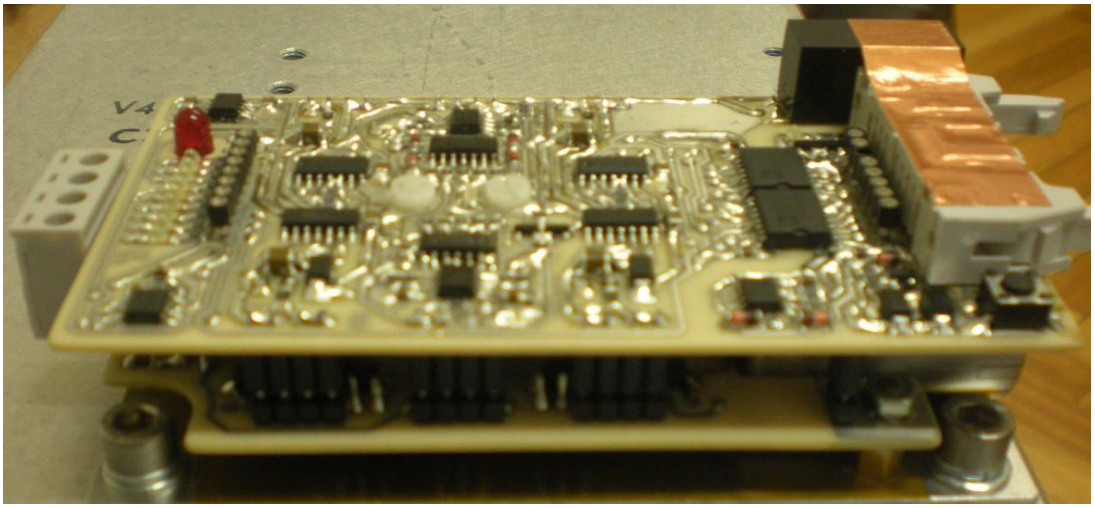


Figure 6-4: MOSFET inverter module with driver circuit

Table 6-1 Technical data of the PWM-pulse inverter

Description	Value
Battery voltage	0…400 V
Supply voltage for power electronics	+12 V
Control signals on ATmega16 system	+5Volt supply voltage, TTL-Level

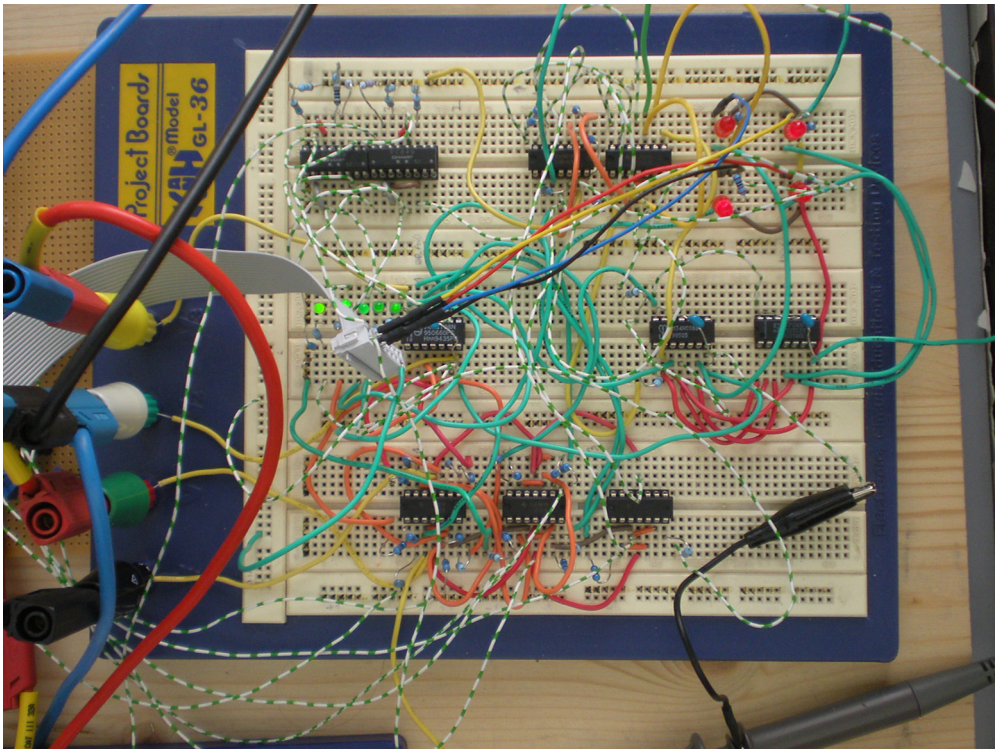


Figure 6-5: Structure of the first analogous inverter

A property of the ATmega16 system is that when it is turned on (if not a program is loaded), all digital outputs are at "high" potential. Even in the case of a program error (e.g. "real-time-error, by the overflow of integrators) the digital outputs are switched to" high ". Only if a program on the main processor of the ATmega16 is executed, system will switch the outputs, as they were defined in the program. While the application is compiled, it adjusts itself to a "high" potential output.

6.1.2 Digital Signal Processor and Control Hardware

The expansion board provides connectors, potentiometers, switches and all the conditioning circuitry necessary to obtain clean input signals inside the voltage bands allowed by DSP. To allow fast communications and minimize the noise related to bit transmissions, the board to-board connection between expansion board and evaluation was preferred to ribbon-cables.

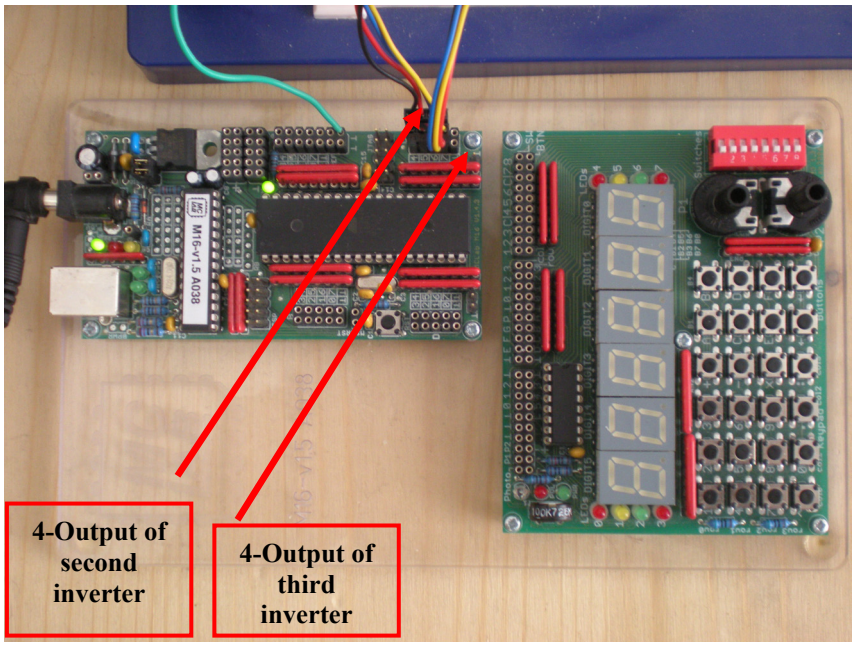


Figure 6-6: DSP board

To ensure the one insulated ground required by the utility, seven insulation transformers in series connection are used necessarily. They have to provide insulation between control, first inverter, second inverter, third inverter and the utility (Figure 3-3). If insulation transformers were not used, there would be a path for the common mode current and the system would loose multilevel converters properties.

6.2 Software

6.2.1 Implemented Algorithms

For the purpose of this dissertation, only the algorithm implemented on the reduced scale converter is described. It is a bit different to the one simulated for two reasons mainly. First of all, the DSP used is a fixed-point architecture in MATLAB/SIMULINK and most of the functions used in simulation can not be implemented on it or their implementation will require a lot of resources and program memory. Second, the algorithm used in simulation can not be implemented using standard PWM based on the comparison between carriers and references.

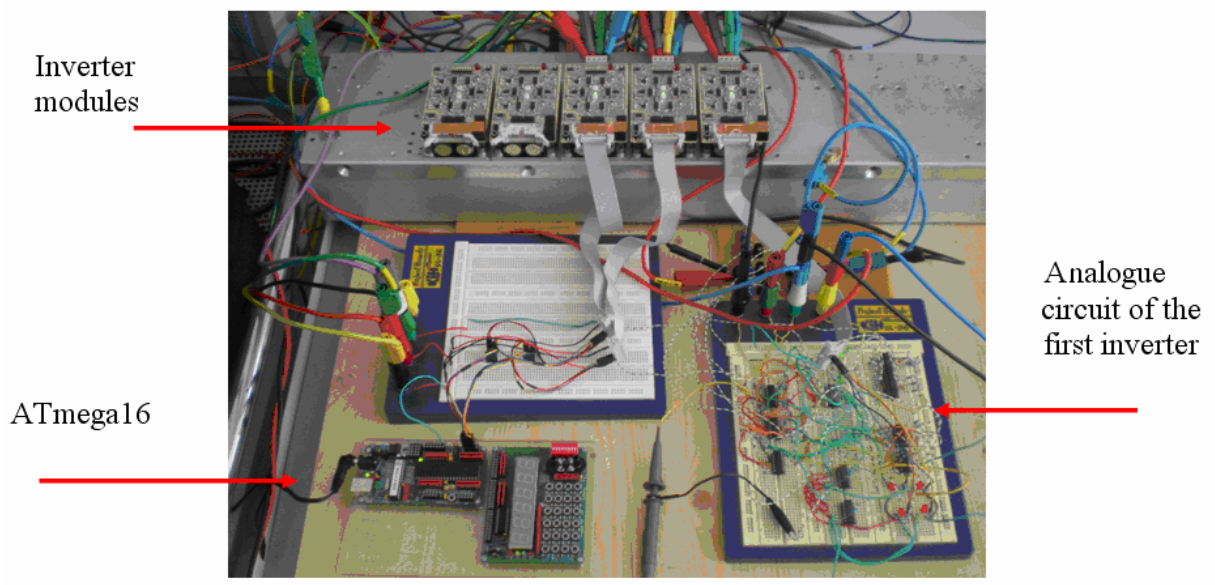


Figure 6-7: Analogue and digital control system working with inverters

6.2.2 Inverter Control

Figure 6-9 shows the logic implementation for the first inverter. The reference sinusoidal signal is compared with constant DC voltages and with the help of AND, NOT and OR gates, the necessary signals in order to produce "+", "-" and "0" states are obtained.

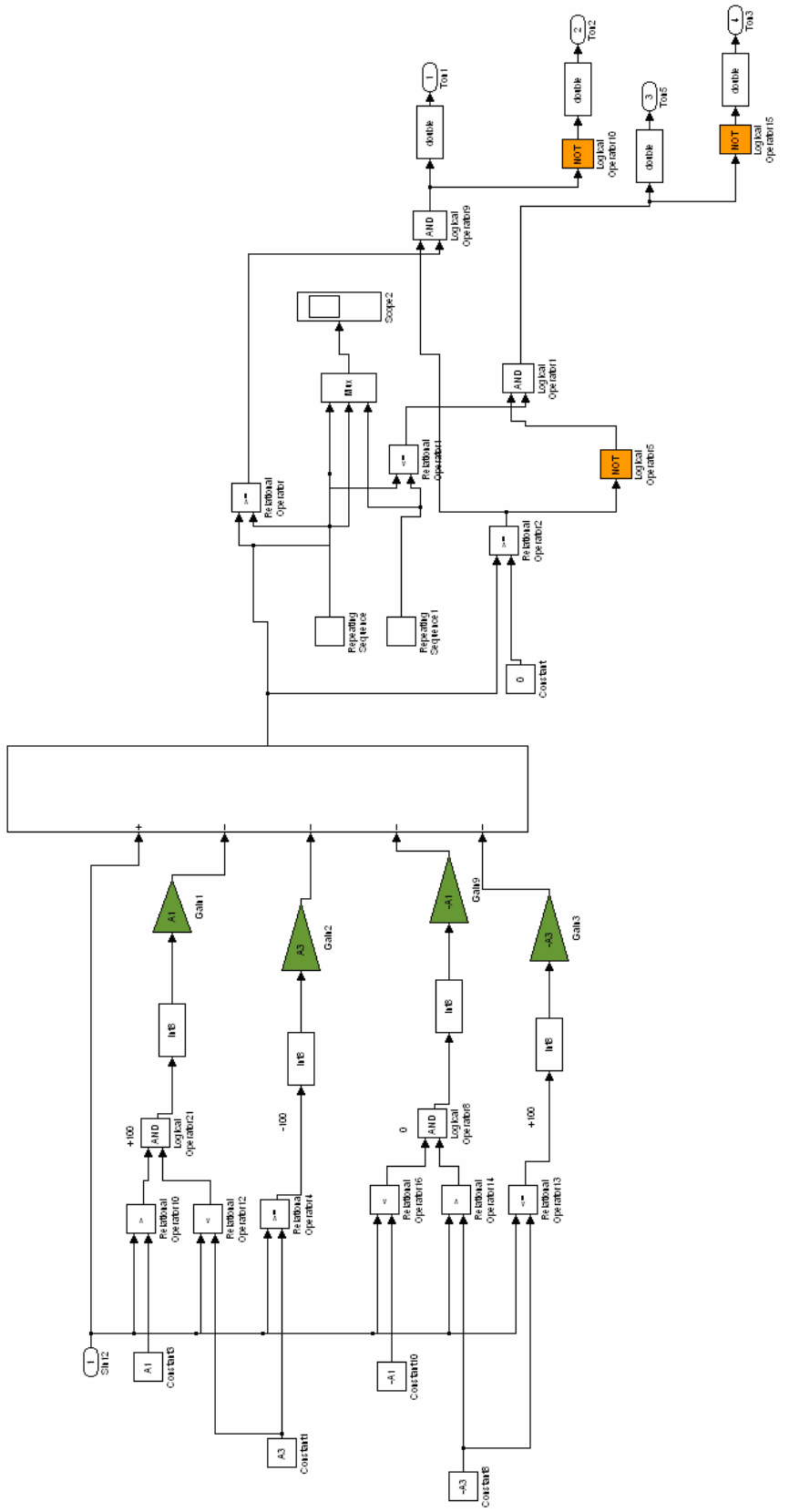


Figure 6-8: Logic map of PWM signal implementation

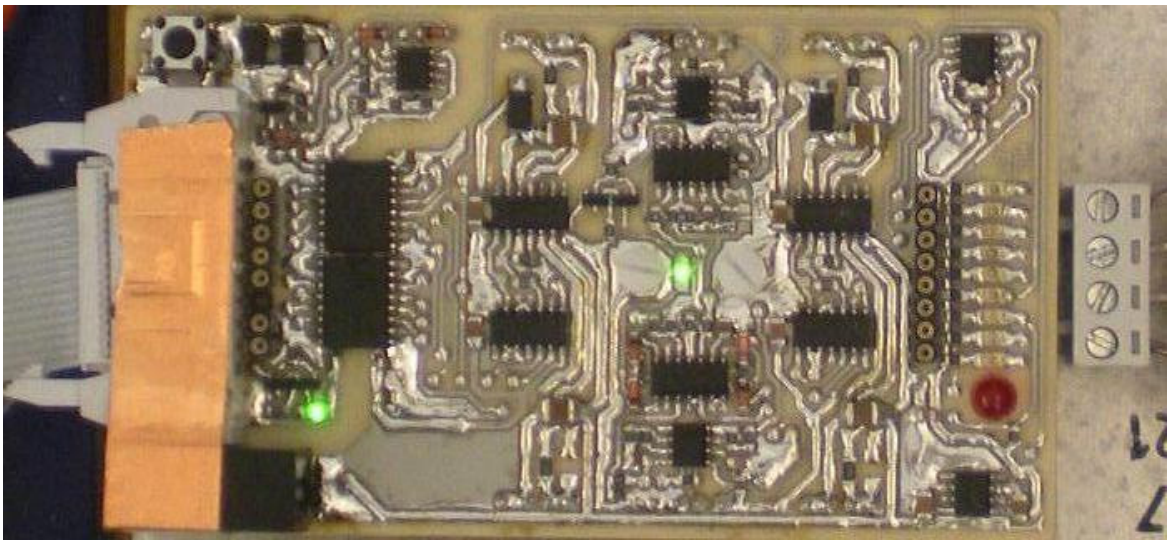


Figure 6-9: Circuit board of MOSFET Inverter [Maier©]

Table 6-2 4-pin screw terminal assignment

Pin	Symbol	Function			Voltage level		Current level	
		Definition	Type	Construction	Min	Max	Sink	Source
1	+Z	negative supply of DC**	Supply	All voltages given here are based on -Z	-	-	-	-
2	PhA	Phase output A**	Output power	MOSFET Half-bridge (SPP20N60C3)	0V	410V	12A (Current limited)	20A (maximum)
3	PhB	Phase output B**	Output power	MOSFET Half-bridge (SPP20N60C3)	0V	410V	12A (Current limited)	20A (maximum)
4	-Z	positive supply of DC**	Supply	100µF DC condensator	0V	410V	-	-

* *Pin 1 of the connector is located next to the red 5 mm LED*
** *Potential separation: Drive signals are galvanically isolated from power section. (Up to 5 kV see ADuM2400)*

6.2.3 Protection Concept

PWM inverter must protect itself from faulty over-currents that can easily occur in the testing phase. In addition, in case a malfunction of the software on the pulse inverter, damage must not occur due to incorrect pulsing of the valves.

In order not to destroy the valves of the pulse inverter the control pulse were checked for accuracy. Very important is the delay of the switching-time of 1 µs. It is important to ensure that an overshoot of the control signals (see Figure 6-11) during the on-off states. The control pulses were measured at the working board and the control signals from the valve, Q1-upper and Q3-lower are recognized.

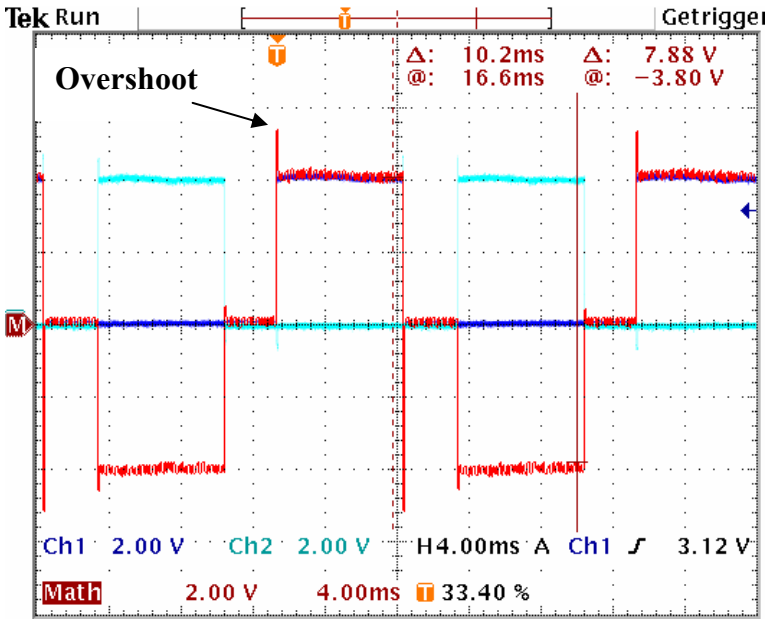


Figure 6-10: Output signals of MOSFET Inverter

The PWM inverter is connected to a battery of 30V in order to handle several conditions during the working process. When DC Voltage is greater than 50V, the red LED turns in to dark in order to show the danger of high voltage. Red SMD is also active if any fault appears. Furthermore, the inverter has protection against high voltage (>410V), under voltage, over temperature ($>80^{o}C$) and over current (12A). After solving the faults problem, the inverter can be again operated by pressing the reset-key.

The current is determined by voltage drop across the resistors and then detected by a comparison with a reference voltage at the comparators. The comparators prevent the destruction of the valves by turning off in the microseconds range.

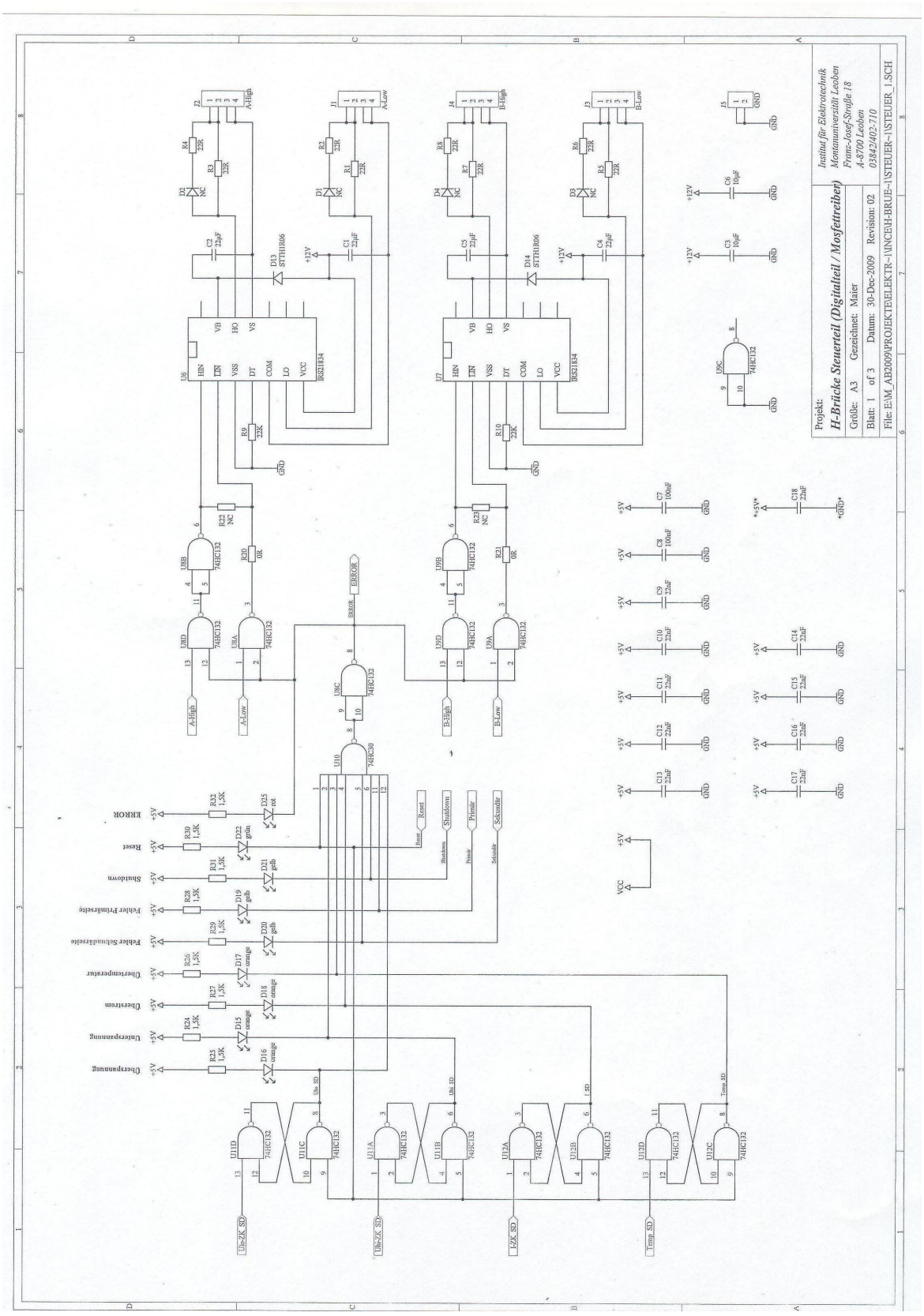


Figure 6-11: The control part of H-Bridge with drive and protection circuit

6.3 Converter Comparison

This chapter compares 10V, 20V, and 30V medium voltage converters on the basis of the 5L- and 8L-SC2LHB VSCs topologies applying 650V MOSFETs. The design of semiconductors and passive components, the semiconductor loss distribution, converter losses, the installed switch power, and the harmonic spectrum will be compared in detail.

6.3.1 Comparison of Power Semiconductor Utilization

Table 6-3 summarizes the design of the power semiconductors of f_c = 4 kHz, 8 kHz, 10 kHz and 20 kHz at a phase current of $I_{ph,rms,l}$ = 2.87A and a maximum junction temperature of $T_{j,\max}$ = 125°C for converter voltages of 6.02V, 12.04V, and 18.06V in all investigated topologies.

In a first step, a constant carrier frequency (f_c = 4 kHz/20 kHz) is assumed for all considered converter topologies. For line-to-line output voltages of 6.02V, 12.04V, and 18.06V, the SC2LHB VSCs enable a maximum converter output power $S_{c,\max}$. The total converter losses, efficiencies, the loss distribution, and the harmonic spectrum of the investigated converter topologies are shown.

Table 6-3 Power semiconductor design for *Iph, rms* = 2.87A, *fc* = 4 kHz/ 20 kHz

Converter line-to-line voltage U_{rms} = 6.02V				
Dc link voltage $U_{dc,n}$	10V			
Converter topology	8L-SC2LHB			
Rated device voltage $U_{CE,n}$	650V MOSFET SPP20N60C3			
	4 [kHz]	8 [kHz]	10 [kHz]	20 [kHz]
Rated MOSFET current [A]	0.933	0.942	0.920	0.926
Maximum apparent inverter output power $S_{c,\max}$ [VA]	7.58	7.64	7.52	7.54
Converter line-to-line voltage U_{rms} = 12.04V				
Dc link voltage $U_{dc,n}$	20V			
Converter topology	8L-SC2LHB			
Rated device voltage $U_{CE,n}$	650V MOSFET SPP20N60C3			
	4 [kHz]	8 [kHz]	10 [kHz]	20 [kHz]
Rated MOSFET current [A]	1.93	1.926	1.929	1.9
Maximum apparent inverter output power $S_{c,\max}$ [VA]	13.2	13.2	13.2	13.2
Converter line-to-line voltage U_{rms} = 18.06V				

Dc link voltage $U_{dc,n}$	30V			
Converter topology	8L-SC2LHB			
Rated device voltage $U_{CE,n}$	650V MOSFET SPP20N60C3			
	4 [kHz]	8 [kHz]	10 [kHz]	20 [kHz]
Rated MOSFET current [A]	2.87	2.87	2.87	2.87
Maximum apparent inverter output power $S_{c,\max}$ [VA]	28.9	28.9	28.9	28.9

Table 6-4 Maximum phase current and apparent converter output power for constant carrier frequency (*Iph, rms= 2.87A, ma = 0.9, cos φ = 0.9*)

Converter line-to-line voltage U_{rms} =6.02V				
Converter topology	8L-SC2LHB			
Device part number	SPP20N60C3			
Carrier frequency f_c [Hz]	4 [kHz]	8 [kHz]	10 [kHz]	20 [kHz]
Maximum apparent inverter output power $S_{c,\max}$ [VA]	7.58	7.64	7.52	7.54
Total harmonic distortion THD [%]	16.6	17	15	16.6
Converter line-to-line voltage U_{rms} =12.04V				
Converter topology	8L-SC2LHB			
Device part number	SPP20N60C3			
Carrier frequency f_c [Hz]	4 [kHz]	8 [kHz]	10 [kHz]	20 [kHz]
Maximum apparent inverter output power $S_{c,\max}$ [VA]	13.2	13.2	13.2	13.2
Total harmonic distortion THD [%]	15.2	14.9	17.6	17.7
Converter line-to-line voltage U_{rms} =18.06V				
Converter topology	8L-SC2LHB			
Device part number	SPP20N60C3			
Carrier frequency f_c [Hz]	4 [kHz]	8 [kHz]	10 [kHz]	20 [kHz]
Maximum apparent inverter output power $S_{c,\max}$ [VA]	28.9	28.9	28.9	28.9
Total harmonic distortion THD [%]	17.2	17.3	17.3	16.3

The *THD* decreases when the number of levels increases. The *WTHD* of the 8L-SC2LHB VSC is clearly lower than that of other topologies due to the seven-level characteristic of the output voltage.

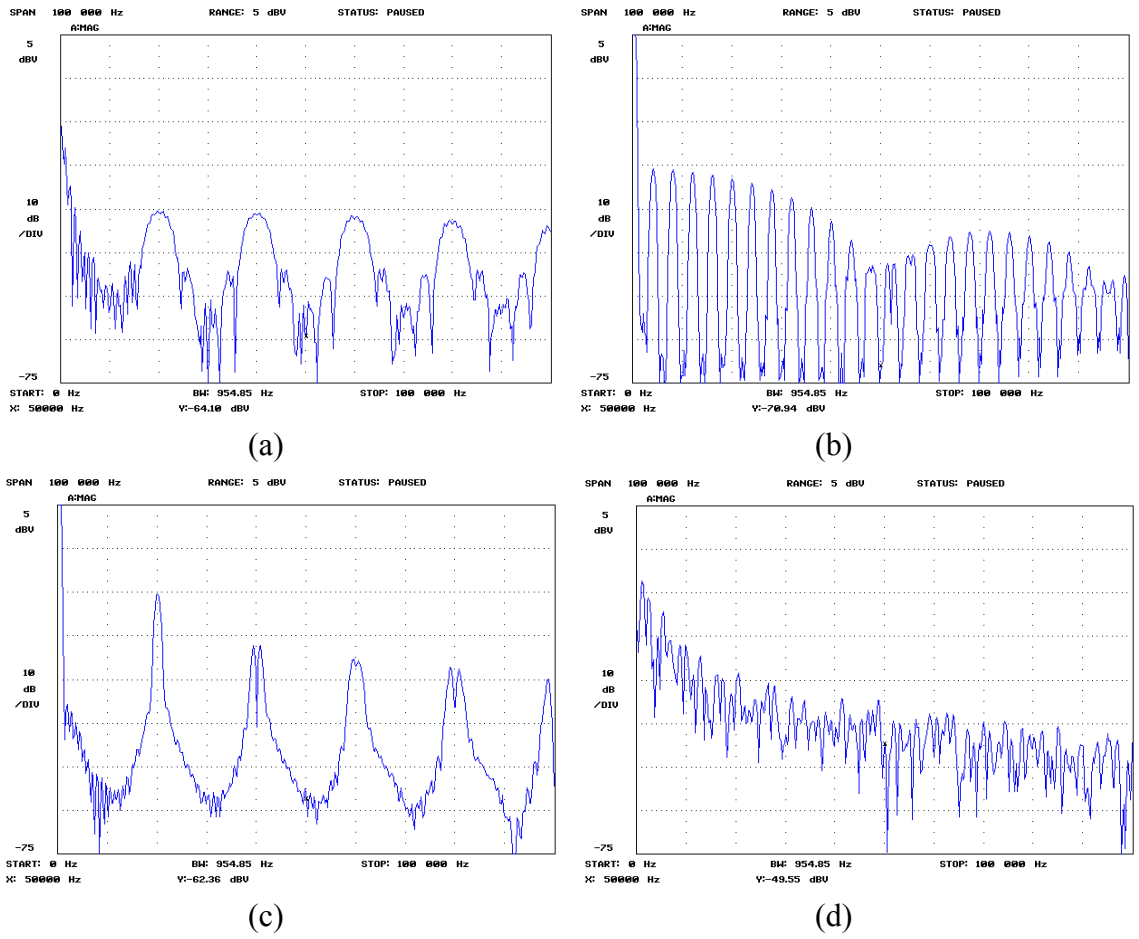


Figure 6-12: (a) *ma*=0.14 and *fcar*=20 kHz, THD=17.2% (b) *ma*=0.14 and *fcar*=4 kHz, THD=18.1% (c) *ma*=1.15 and *fcar*=20 kHz, THD=22.4% (d) *ma*=1.15 and *fcar*=4 kHz, THD=22.4%

The harmonic spectrum of the line-to-neutral output voltage of the considered converter is shown in Figure 6-12. It illustrates that the first carrier band of the line-to-neutral output voltage of the 8L- SC2LHB VSC occurs around the carrier frequency. Hence, an output filter of the SC2LHB VSCs could be smaller than the corresponding filters of other topologies.

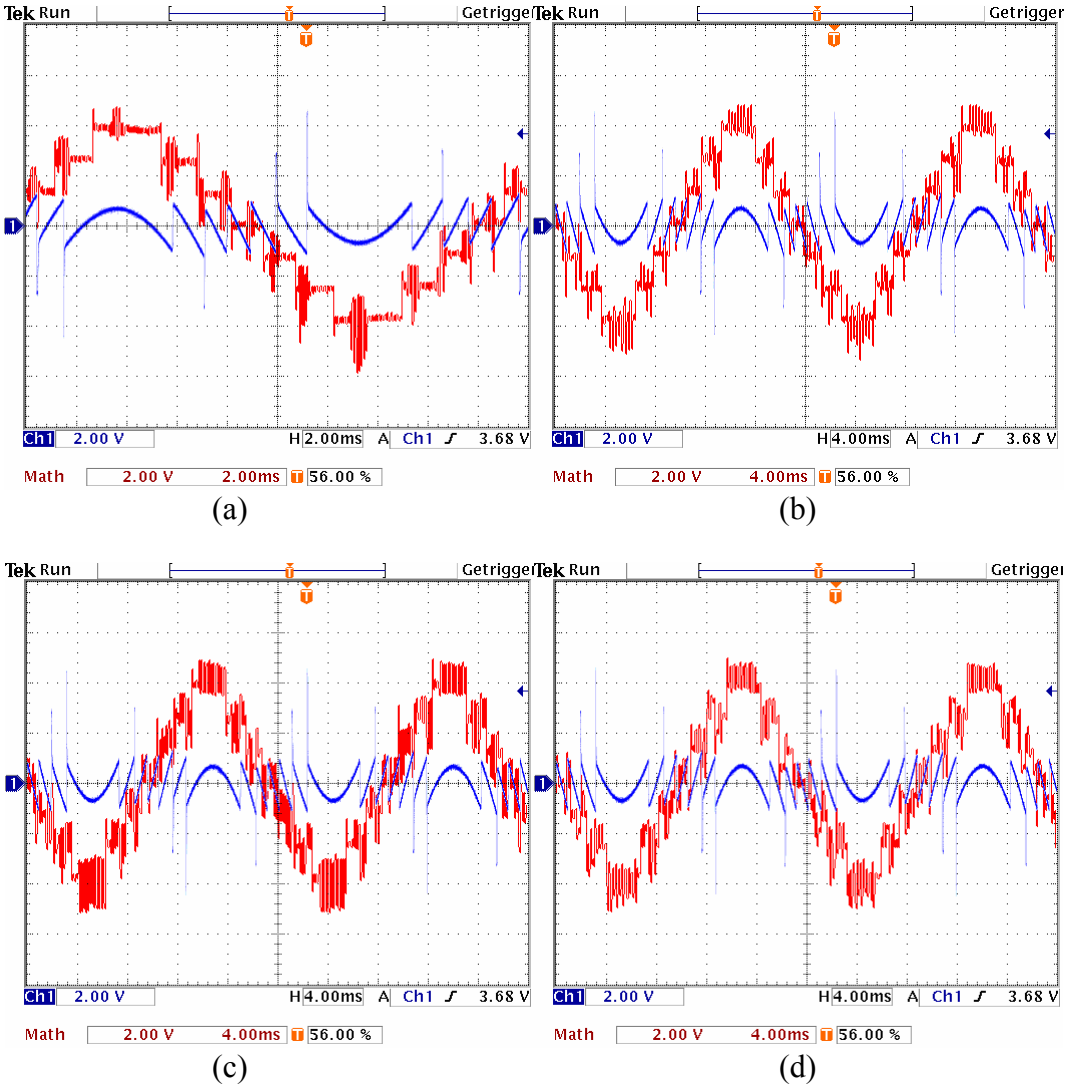


Figure 6-13: (a) *ma*=0.14 and *fcar* =20 kHz, THD=17.2% (b) *ma*=0.14 and *fcar* =4 kHz, THD=17.9% (c) *ma*=1.15 and *fcar* =20 kHz, THD=22.4% (d) *ma*=1.15 and *fcar* =4 kHz, THD=21.7%

The experimental output quality, especially at low modulation indexes, is not good. It should be noted that the level of steps is actually reduced when modulation is less than 0.5.

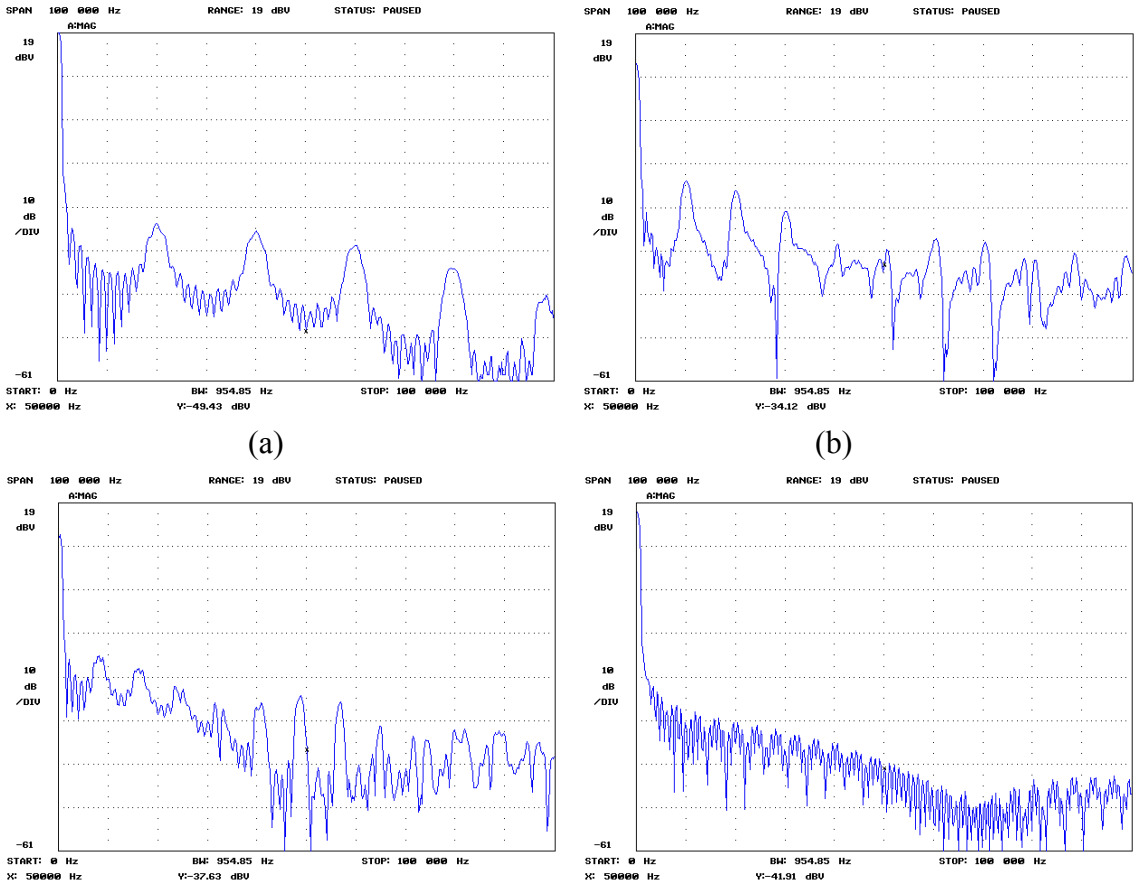
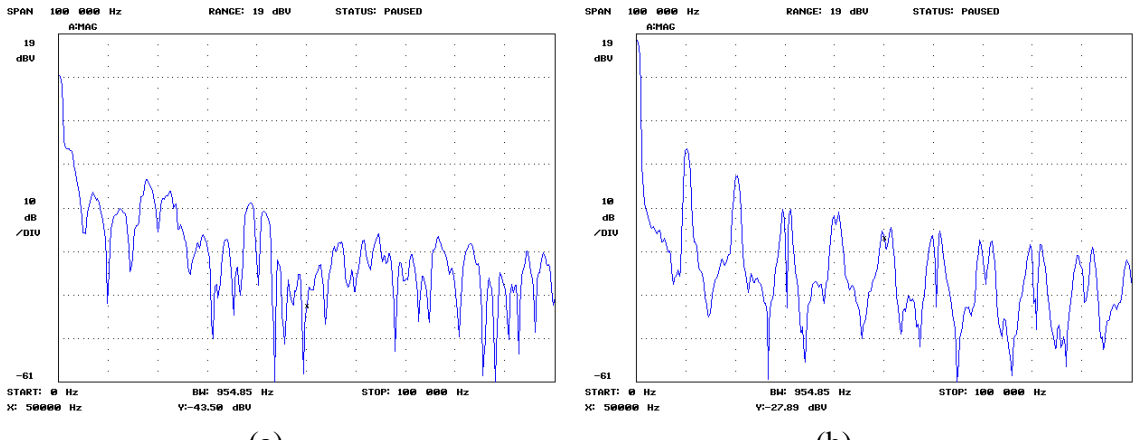
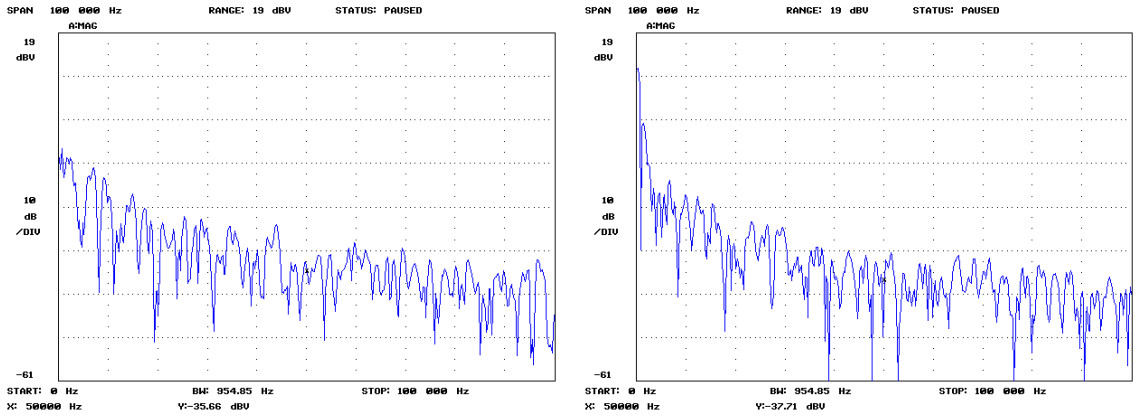


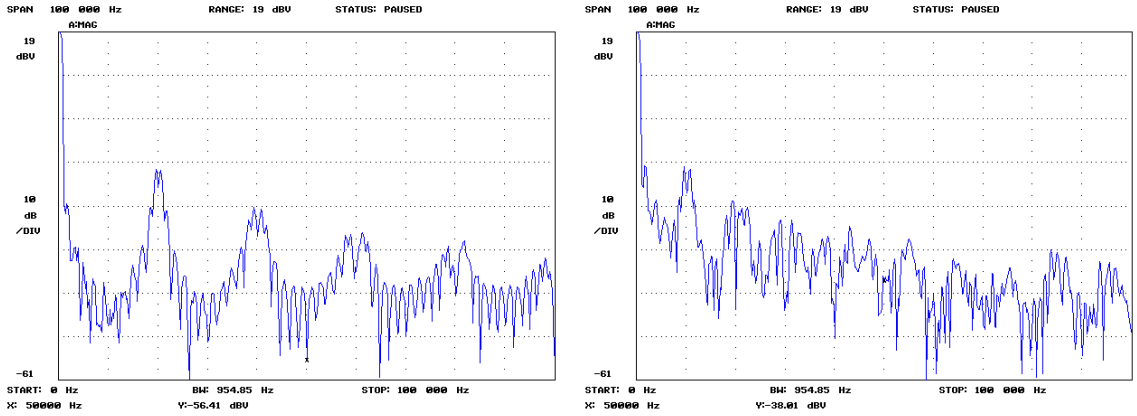
Figure 6-14: ma=0.14 (a) *fcar* = 20 kHz, THD=17.2% (b) *fcar* = 10 kHz, THD=18.1% (c) *fcar* = 8 kHz, THD=22.4% (d) *fcar* = 4 kHz, THD=23.4%



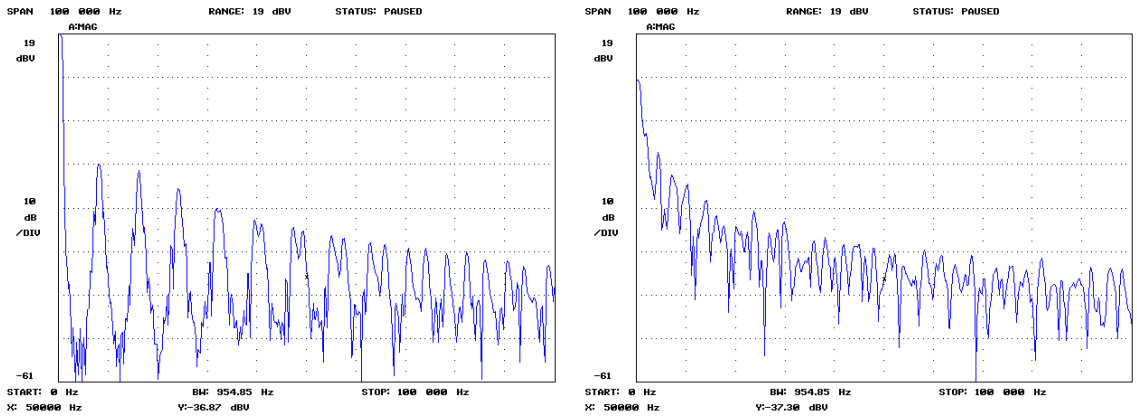


(c) (d)

Figure 6-15: *ma*=0.4 (a) *fcar* = 20 kHz, THD=23.4% (b) *fcar* = 10 kHz, THD=22.1% (c) *fcar* = 8 kHz, THD=22.7% (d) *fcar* = 4 kHz, THD=23.2%



(a) **(b)**



(c) **(d)**

Figure 6-16: *ma*=0.8 (a) *fcar* = 20 kHz, THD=26.9% (b) *fcar* = 10 kHz, THD=26.1% (c) *fcar* = 8 kHz, THD=26.3% (d) *fcar* = 4 kHz, THD=23.4%

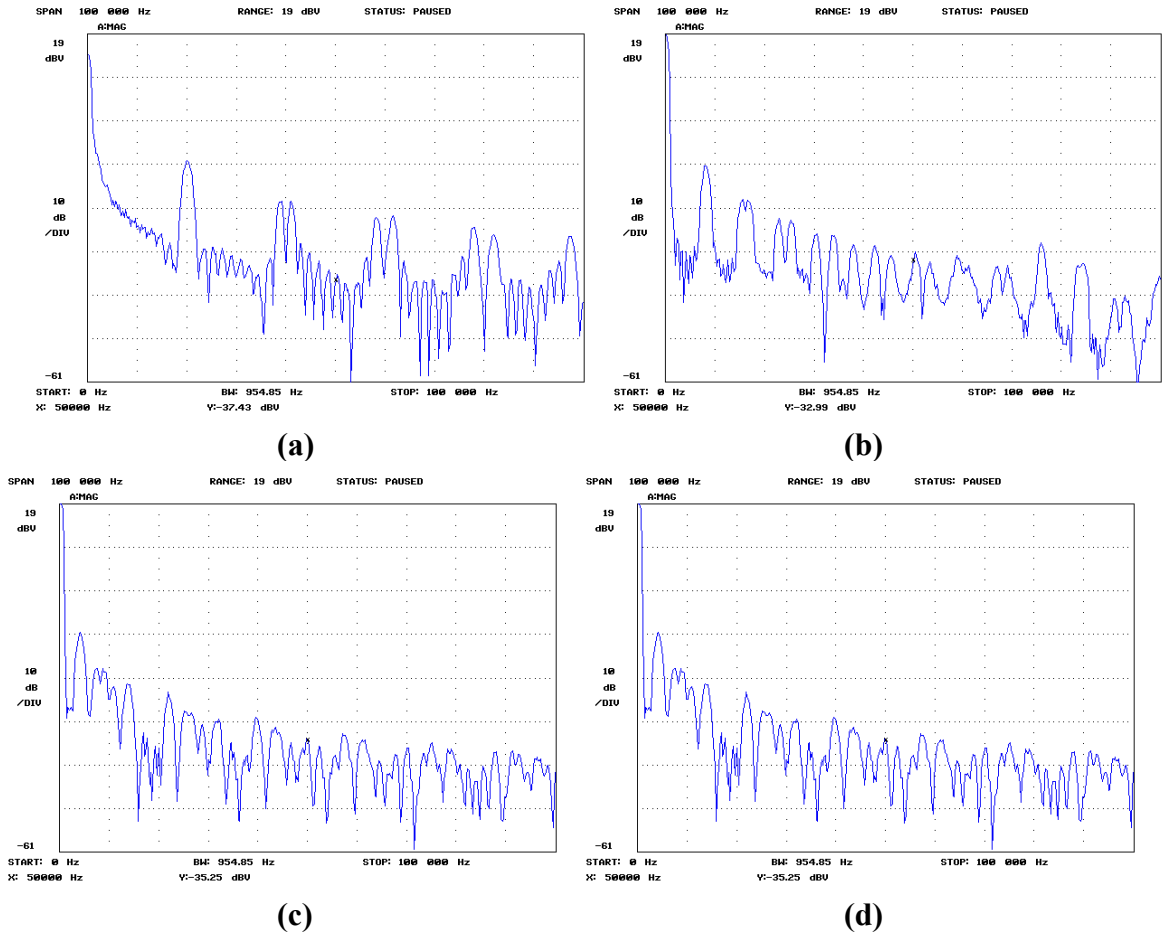
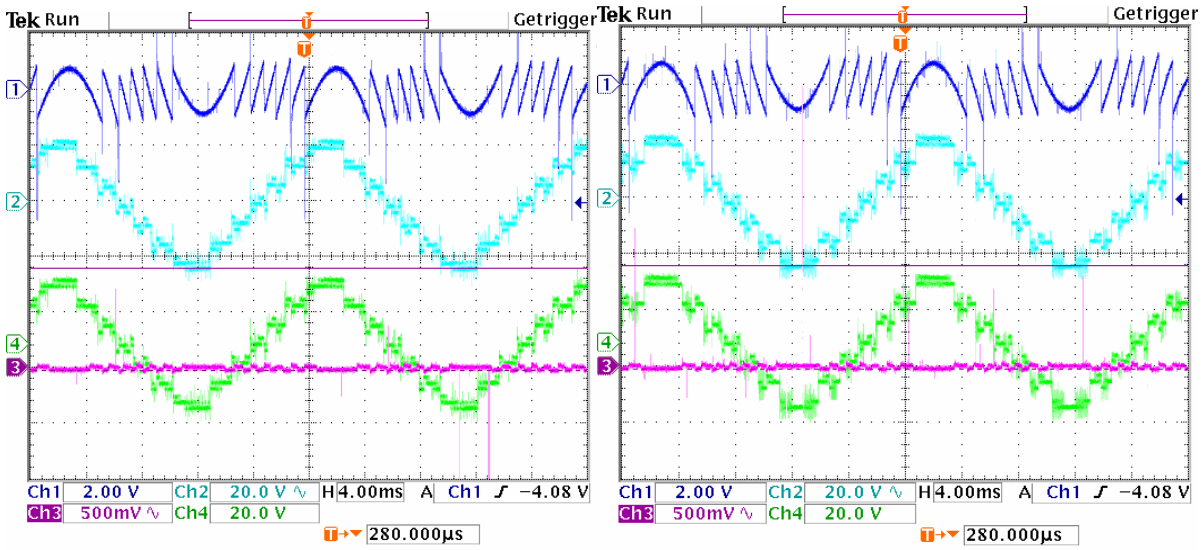


Figure 6-17: *ma*=1 (a) *fcar* =20 kHz, THD=29.2% (b) *fcar* = 10 kHz, THD=28.6% (c) *fcar* = 8 kHz, THD=28.8% (d) *fcar* = 4 kHz, THD=28.7%

Figure 6-13 – 6-18 show simulation and experimental results of phase voltage and load current with the modulation index of 1.0, 0.85, 0.4, and 0.1. The experimental line voltage spectra in dB are also resented in figure 6-18. As expected, the results show that 5^{th} and the 7^{th} harmonics of the line voltage are very small in magnitudes. Because of 120 degree phase shift among phase voltages, all triple harmonics in line voltages are also very small. The experimental results match with the calculated and simulated results.

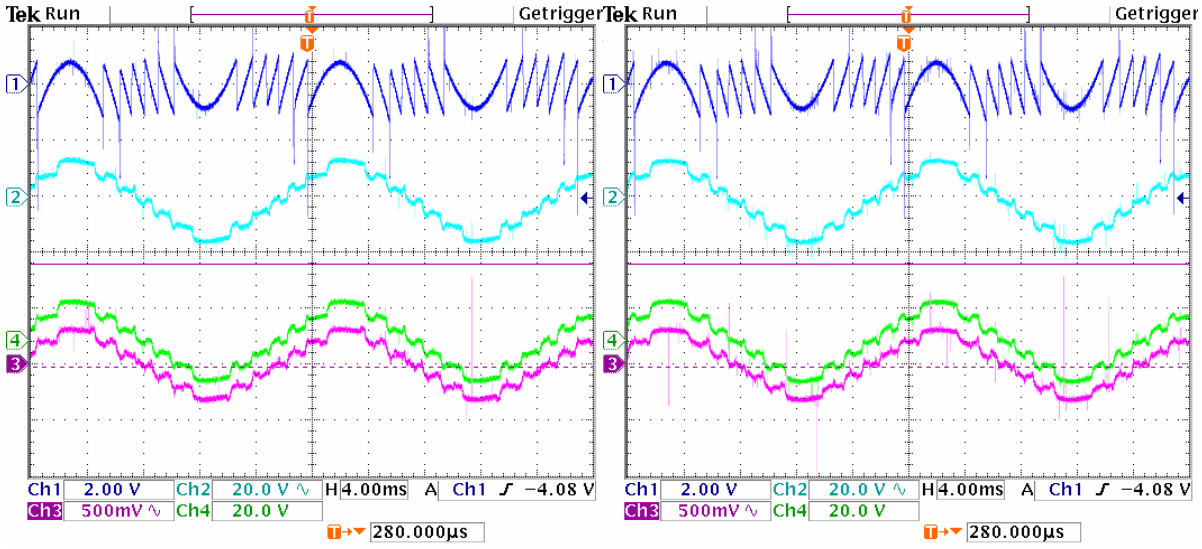
According to measurements, the maximum switching frequency results from the losses and junction temperatures of the mostly stressed devices ($T_{j,\max}$ = 125°C) at critical operating points.

Comparing the *WTHD* at the maximum possible carrier frequency, the 8L-SC2LHB VSC features the minimum value of 0.61% since the harmonics of the first carrier band (f_c = 8 kHz) are strongly reduced by switching frequency and modulation index.



(a) (b)

Figure 6-18: (2) Inverter output voltage (4) Cable output voltage. Output voltage according to different switching frequencies without load (a) 4 kHz 30V and (b) 20 kHz 30V



(a) (b)

Figure 6-19: (2) Inverter output voltage (3) Load current (4) Cable output voltage. Output voltage and load current according to different switching frequencies with load (a) 4 kHz 3.6Ω and (b) 20 kHz 3.6Ω

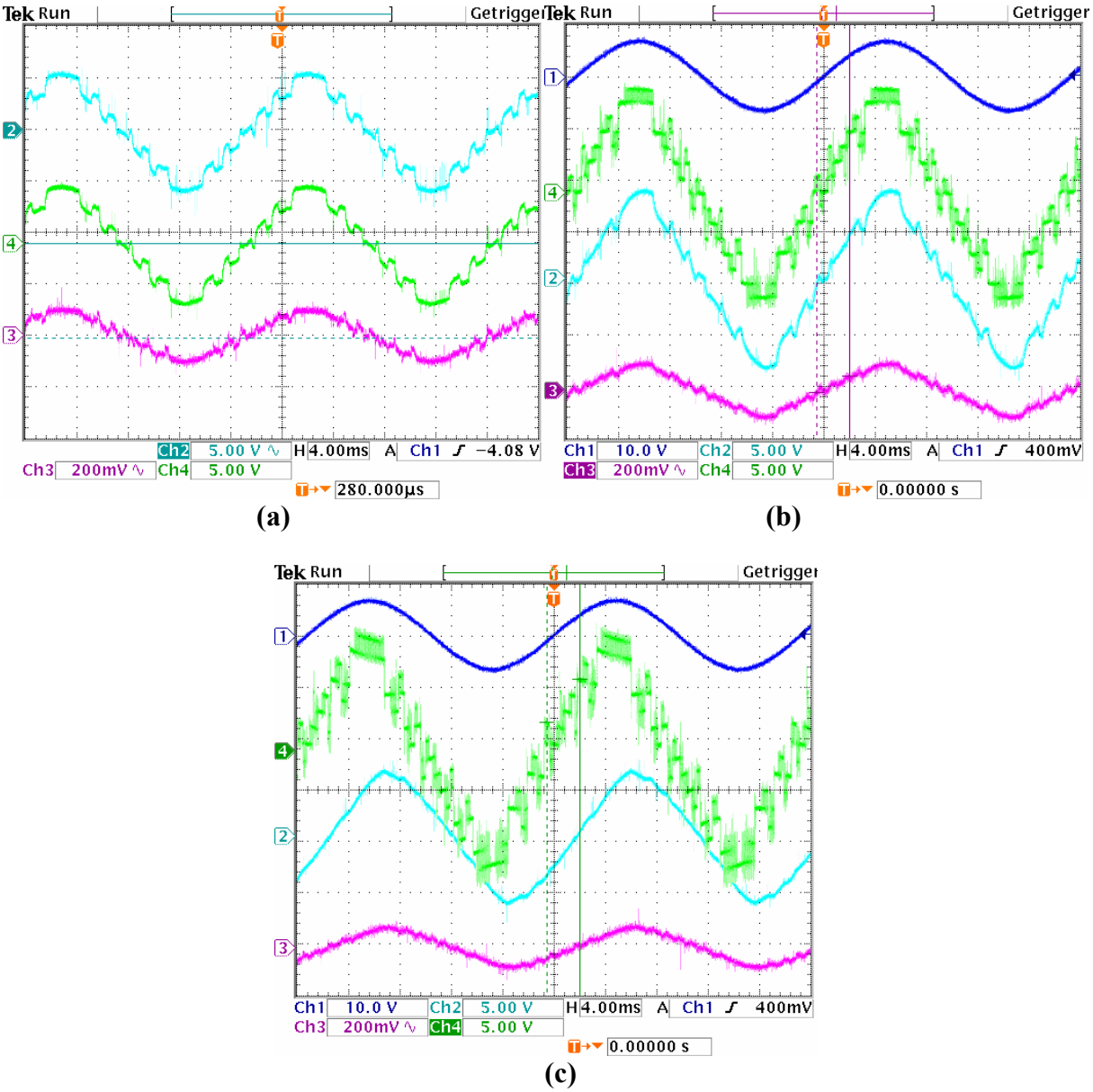
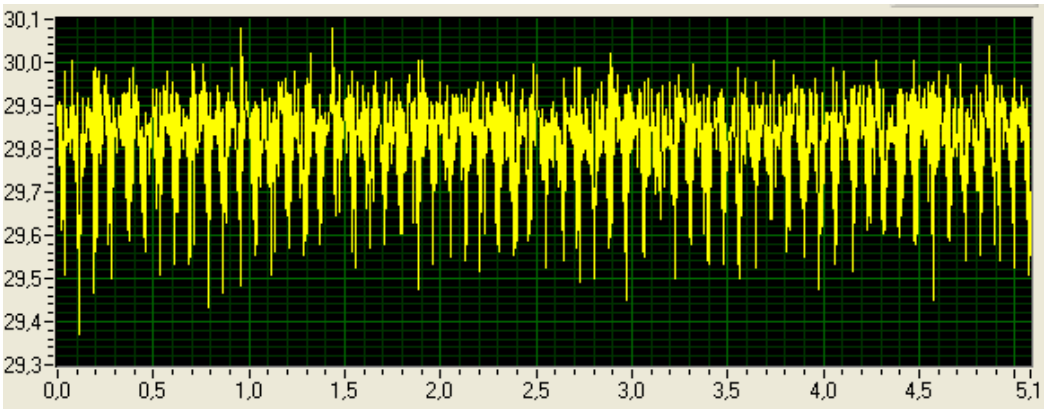


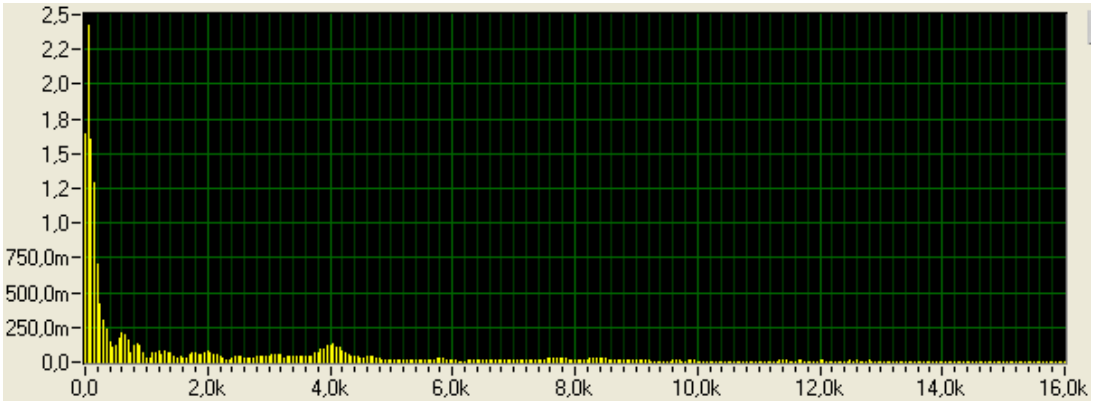
Figure 6-20: (4) Inverter output voltage (3) Load current (2) Cable output voltage. Output voltage and load current according to different switching frequencies with load (a) 12Ω and 1.65mH at 4 kHz (b) 12Ω and 1.65mH at 20 kHz (c) 12Ω and 12.56mH at 20 kHz

The THD of the output voltage and output current are 22.7%, 8.3%, respectively. The *WTHD* of the 8L-SC2LHB VSC is clearly the smallest, since the distortion of the output voltage is at a minimum due to the applied seven levels.



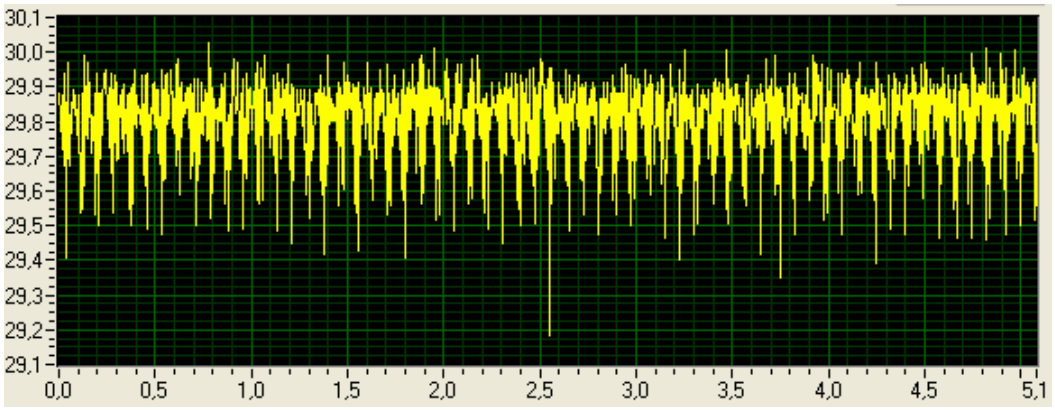
(a)

(b)

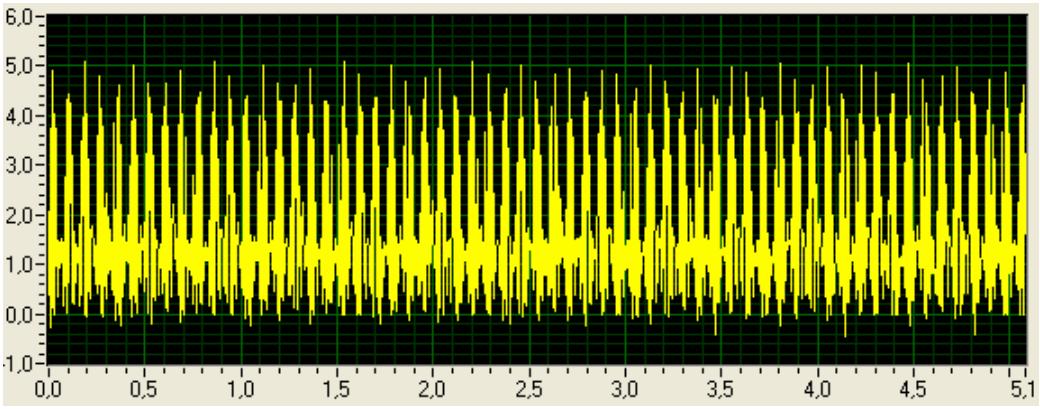


(c)

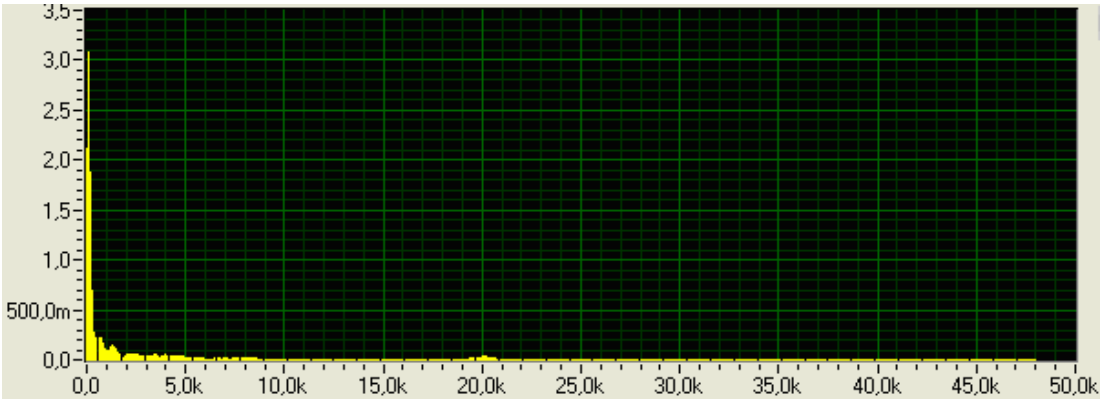
Figure 6-21: (a) DC link voltage ripple (b) DC link current (c) DC link voltage harmonic spectra in the 8L-SC2LHB *(C = 3.3mF, DC=30V, fcar = 4 kHz, fcar = 50 Hz, ma = 0.9,Vll,rms = 12.04V, Iph,rms,l= 2.98A, cos φ = 0.9)*



(a)



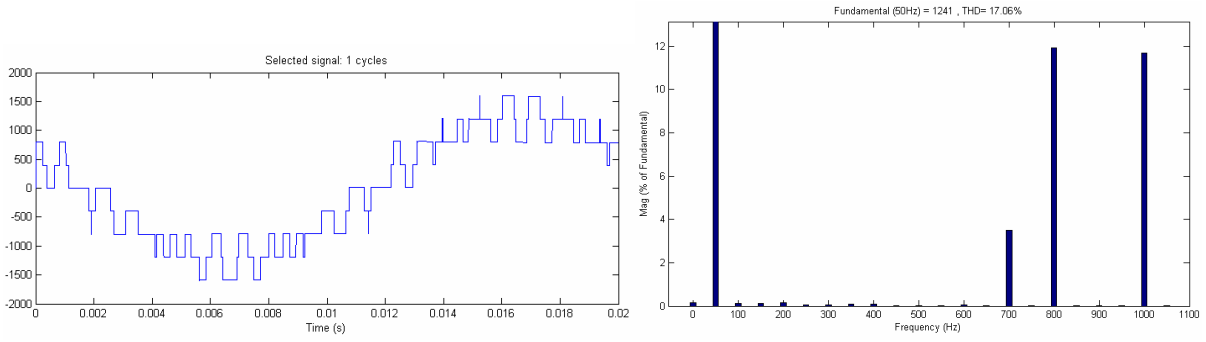
(b)



(c)

Figure 6-22: (a) DC link voltage ripple (b) DC link current (c) DC link voltage harmonic spectra in the 8L-SC2LHB *(C = 3.3mF, DC=30V, fcar = 4 kHz, fcar = 50 Hz, ma = 0.9,Vll,rms = 12.04V, Iph,rms,l= 2.98A, cos φ = 0.9)*

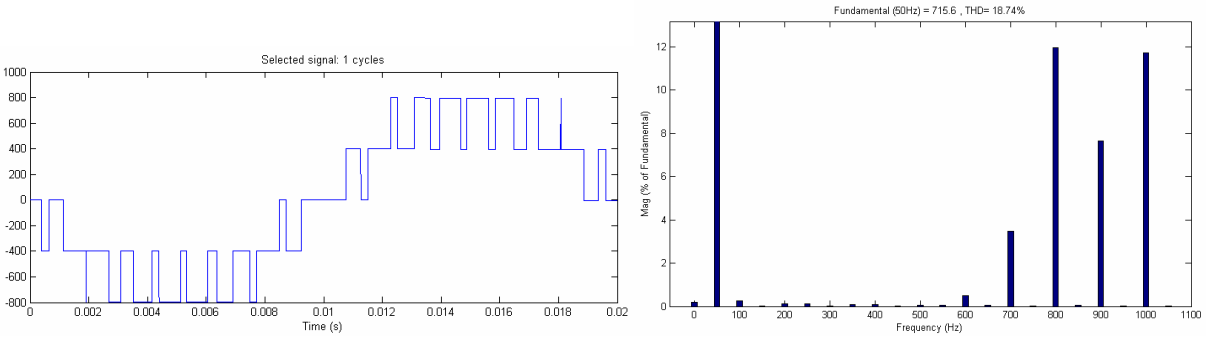
DC link voltage ripple increases with high switching frequencies and can be reduced in order to select high capacity condensators.



(a) (b)

Figure 6-23: 5L-SC2LHB VSC (IGBT) with APOD method (a) line-to-line voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*

Figure 6-24 shows the line voltage waveform with hysteresis control and the corresponding harmonic spectrum. The value of THD calculated using Simulink is 17.06%.



(a) (b)

Figure 6-24: 5L-SC2LHB VSC (IGBT) with APOD method (a) line-to-neutral voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*

Figure 6-25 shows the phase voltage waveform with PWM control and the corresponding harmonic spectrum. The value of THD calculated using Simulink is 18.74%.

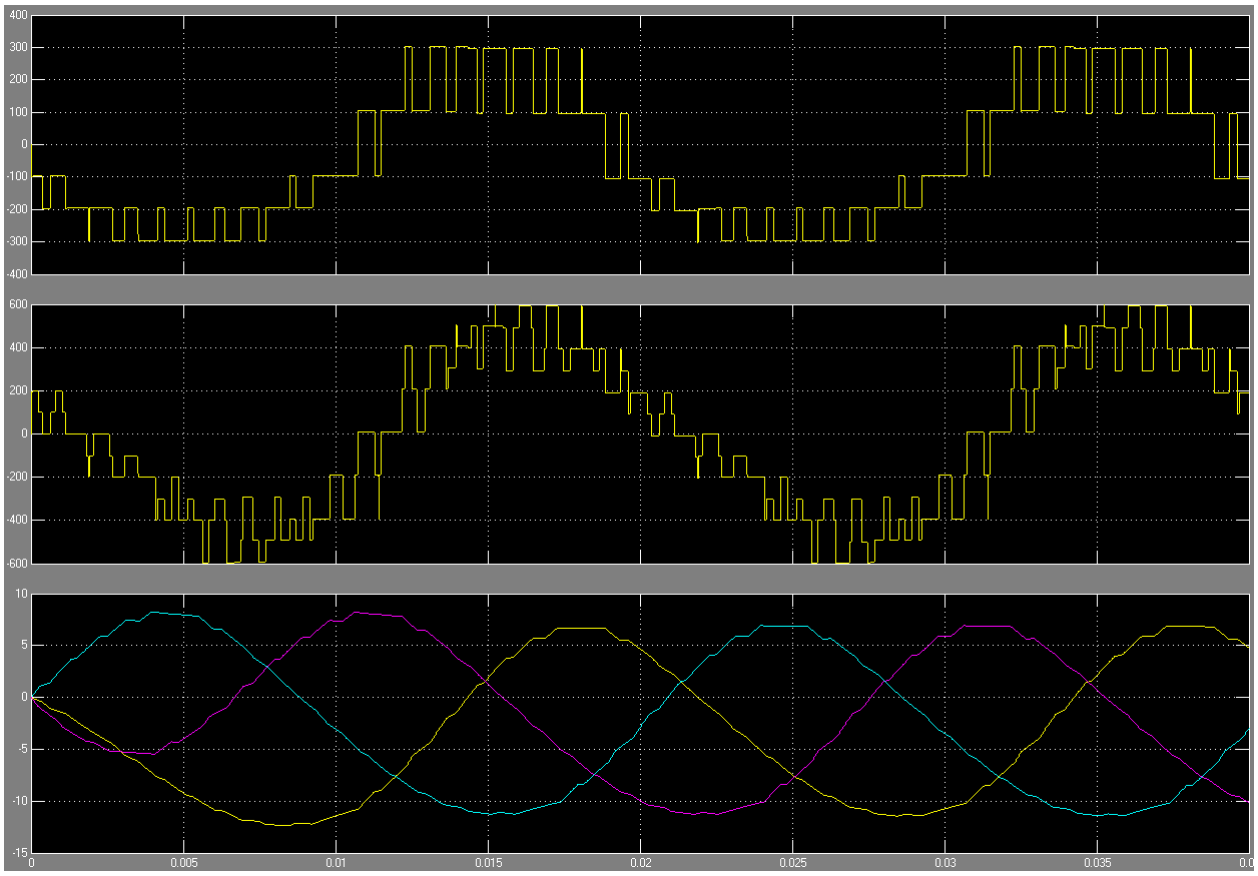
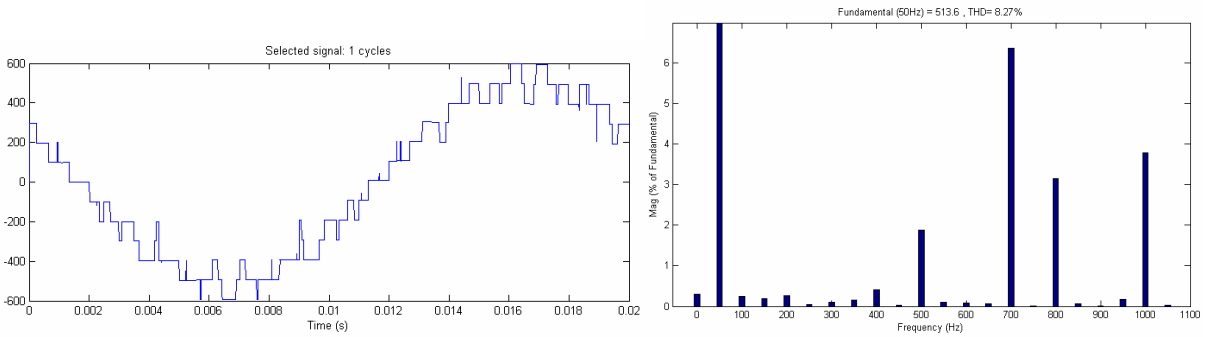
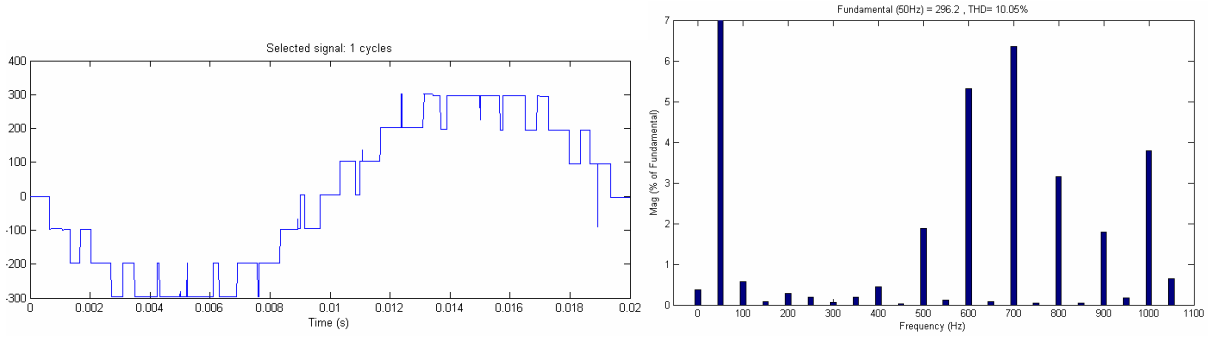


Figure 6-25: 5L-SC2LHB VSC (IGBT) with APOD method (a) line-to-neutral voltage (b) line-to-line voltage (c) phase currents *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*



(a) (b)

Figure 6-26: 5L-SC2LHB VSC (IGBT) with NEW method (a) line-to-line voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*



(a) (b)

Figure 6-27: 5L-SC2LHB VSC (IGBT) with NEW method (a) line-to-neutral voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*

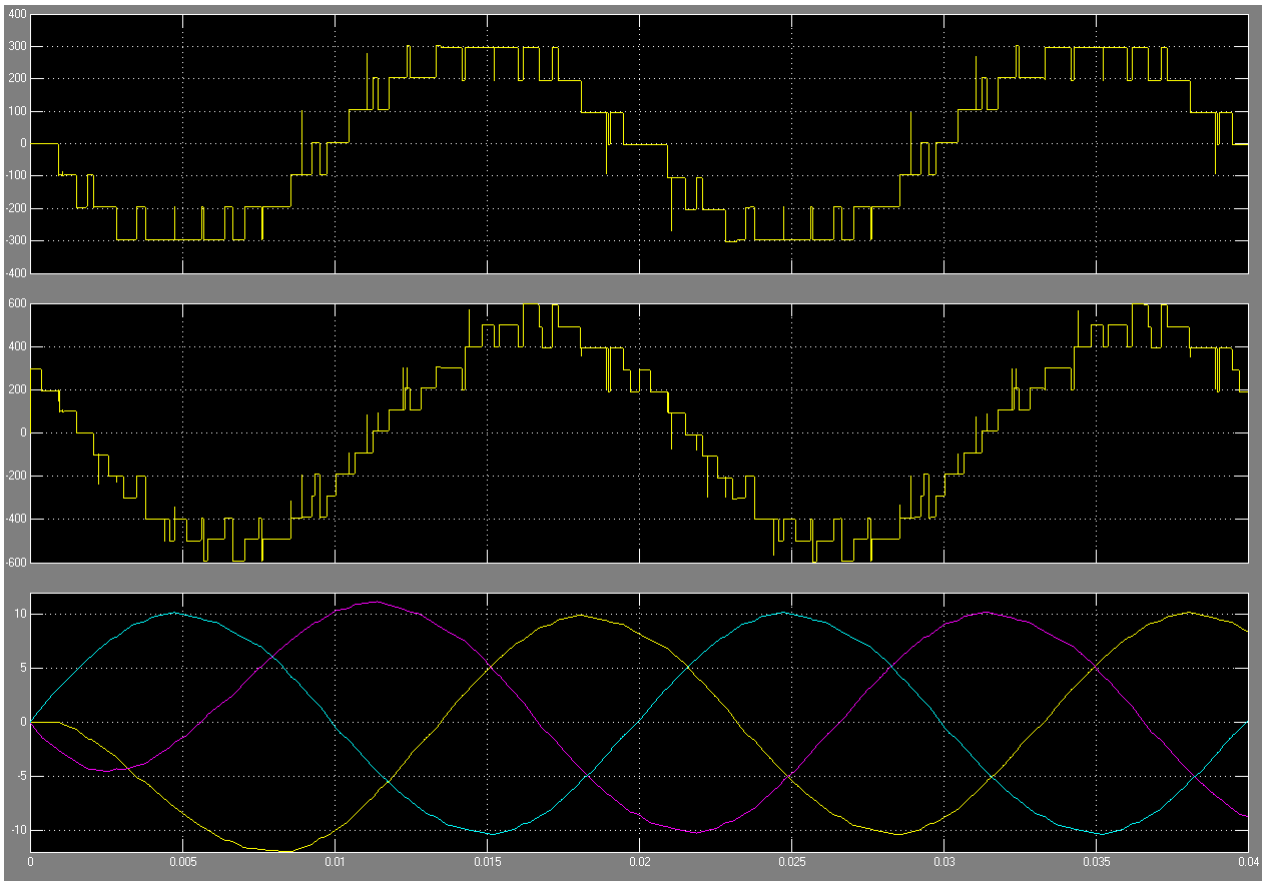
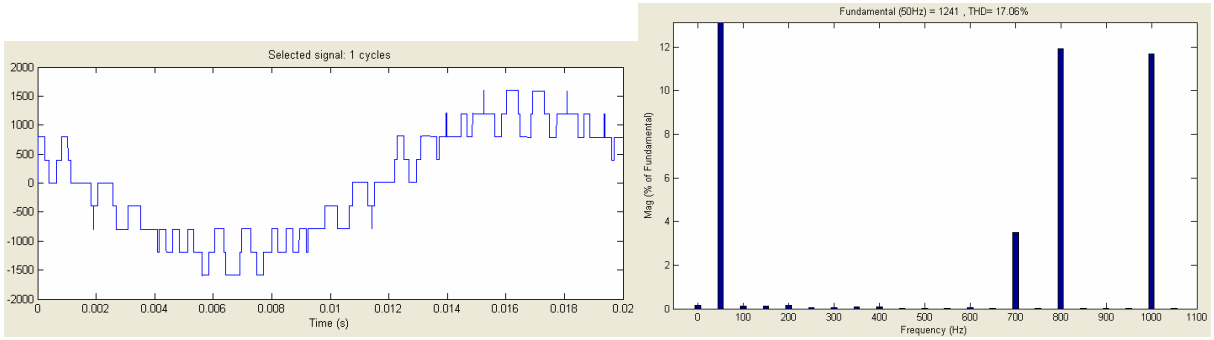
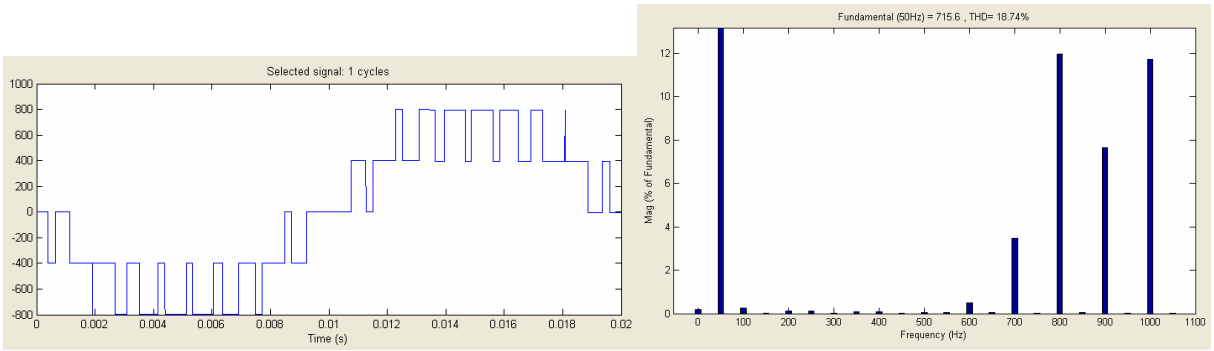


Figure 6-28: 5L-SC2LHB VSC (IGBT) with NEW method (a) line-to-neutral voltage (b) line-to-line voltage (c) phase currents *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*



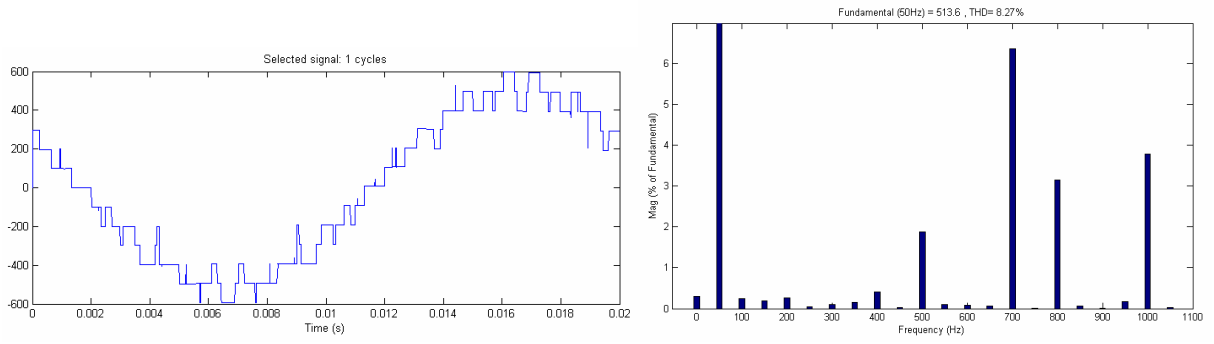
(a) (b)

Figure 6-29: 5L-SC2LHB VSC (MOSFET) with APOD method (a) line-to-line voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*



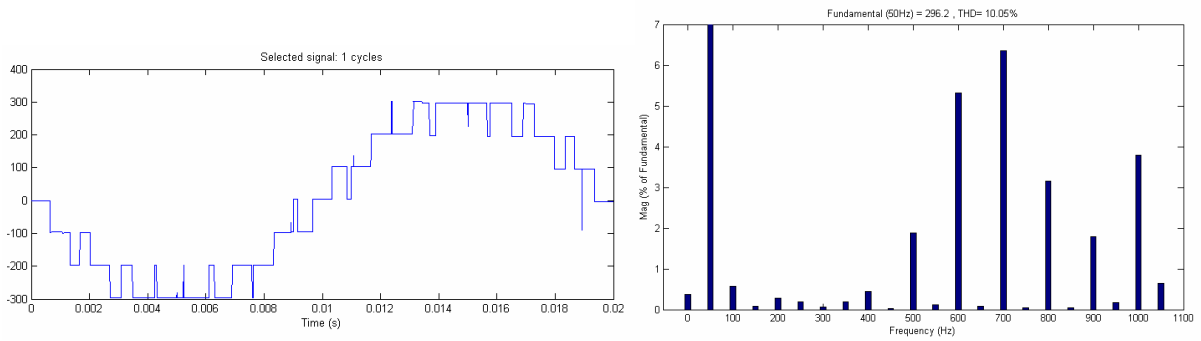
(a) (b)

Figure 6-30: 5L-SC2LHB VSC (MOSFET) with APOD method (a) line-to-neutral voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*



(a) (b)

Figure 6-31: 5L-SC2LHB VSC (MOSFET) with NEW method (a) line-to-line voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*



(a) (b)

Figure 6-32: 5L-SC2LHB VSC (MOSFET) with NEW method (a) line-to-neutral voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*

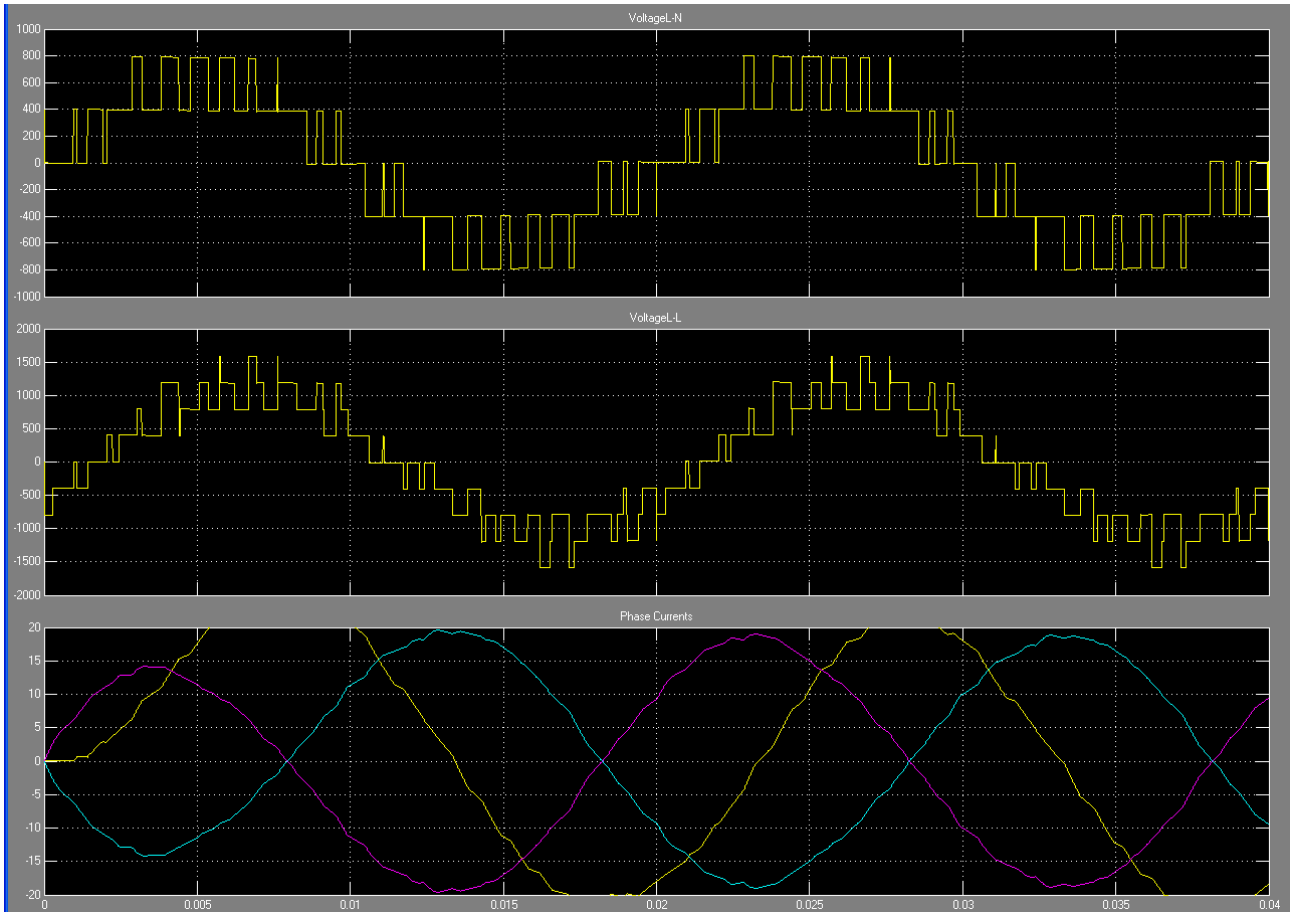
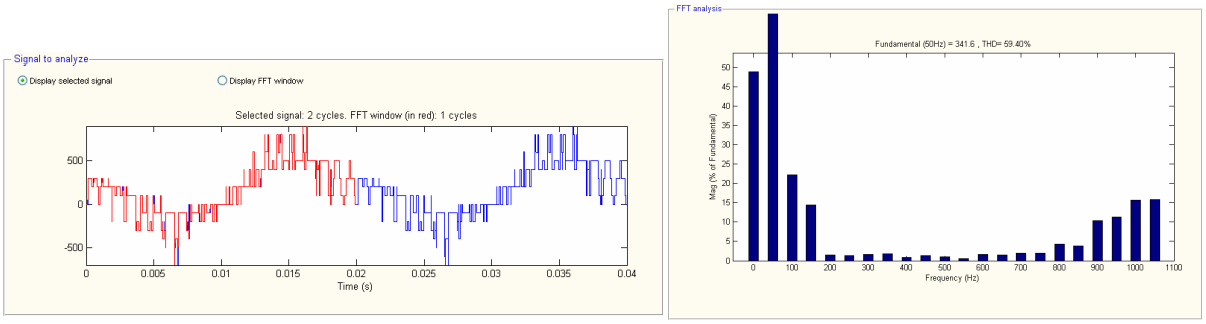
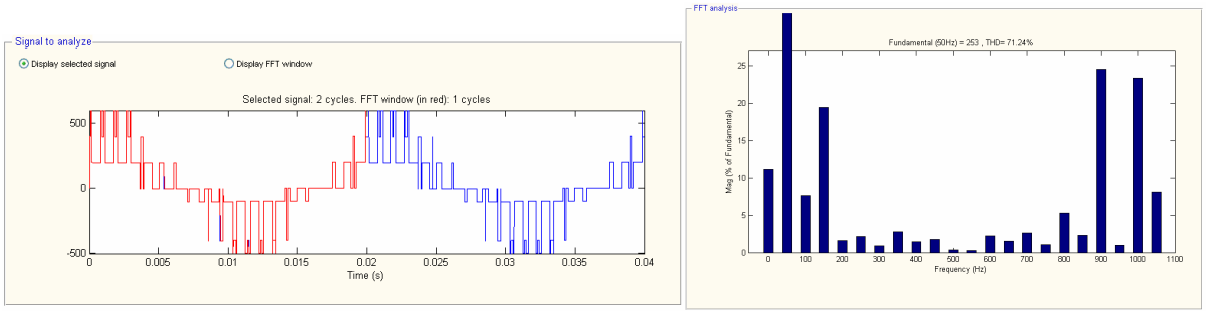


Figure 6-33: 5L-SC2LHB VSC (MOSFET) with NEW method (a) line-to-neutral voltage (b) line-to-line voltage (c) phase currents *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*



(a) (b)

Figure 6-34: 8L-SC2LHB VSC (IGBT) with APOD method (a) line-to-line voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*



(a) (b)

Figure 6-35: 8L-SC2LHB VSC (IGBT) with APOD method (a) line-to-neutral voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*

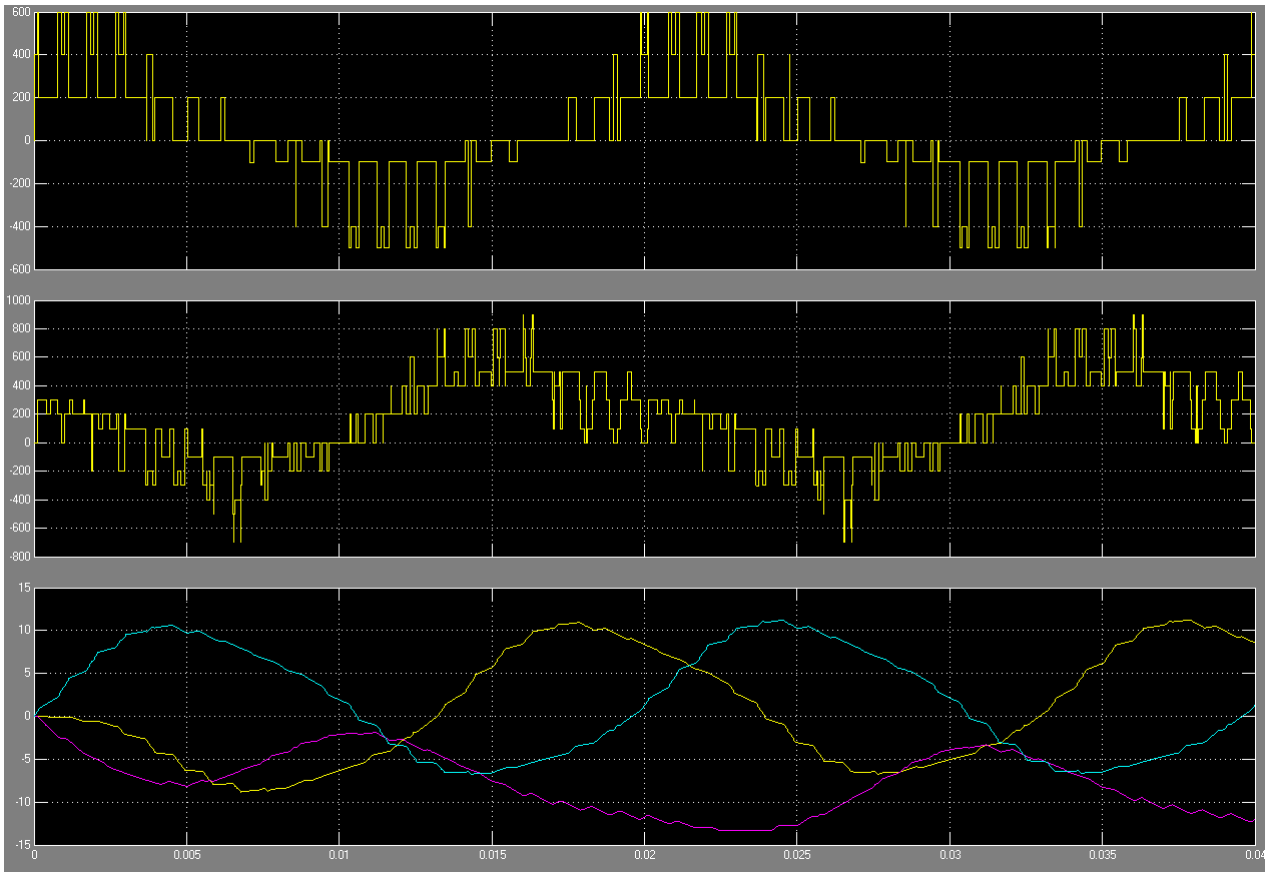
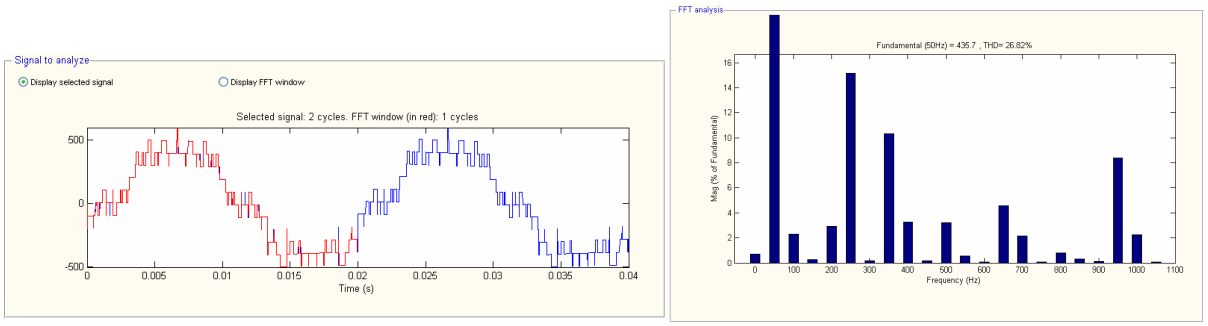
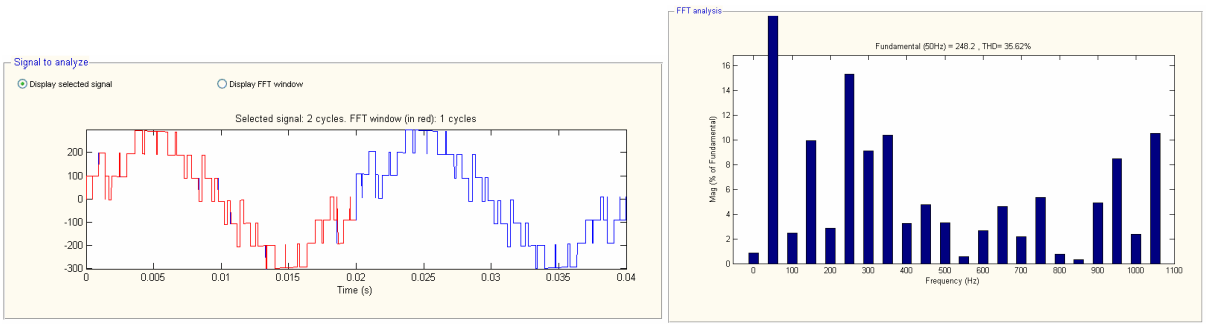


Figure 6-36: 8L-SC2LHB VSC (IGBT) with APOD method (a) line-to-neutral voltage (b) line-to-line voltage (c) phase currents *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*



(a) (b)

Figure 6-37: 8L-SC2LHB VSC (IGBT) with NEW method (a) line-to-line voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*



(a) (b)

Figure 6-38: 8L-SC2LHB VSC (IGBT) with NEW method (a) line-to-neutral voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*

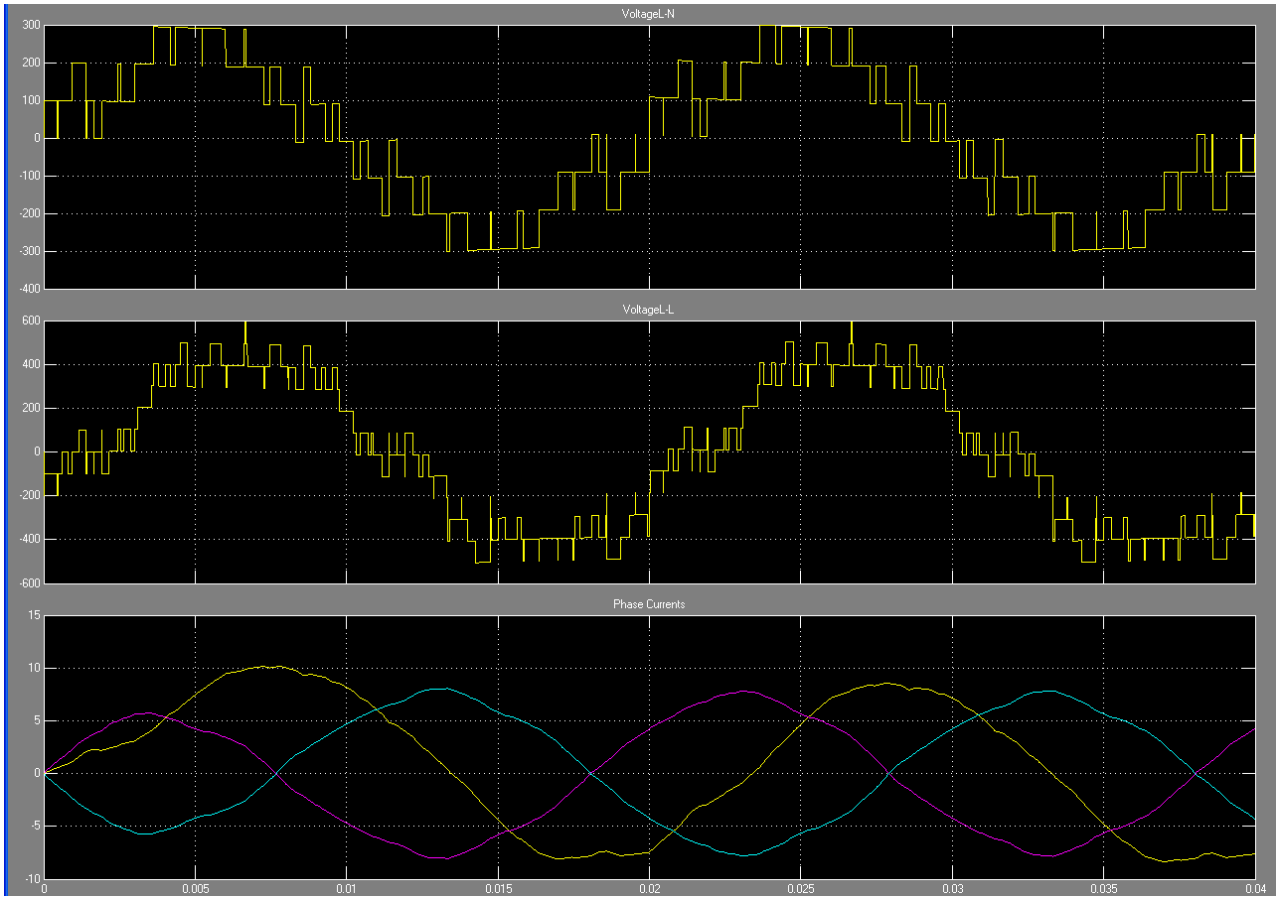
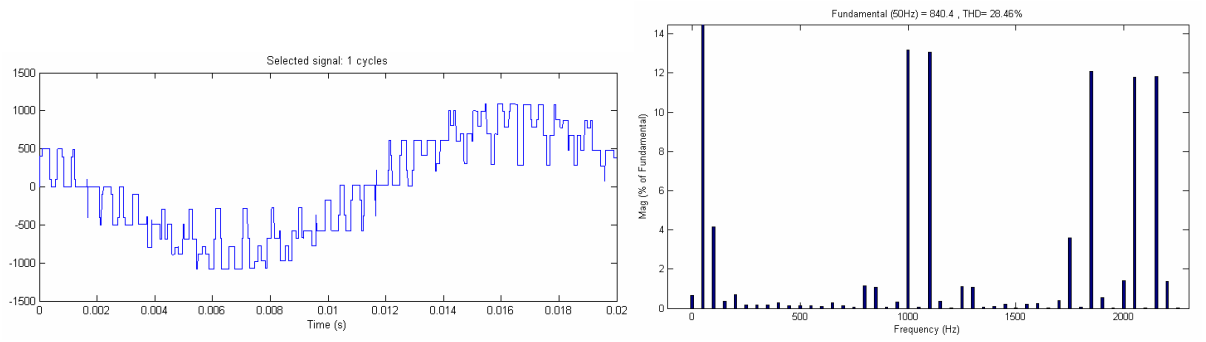
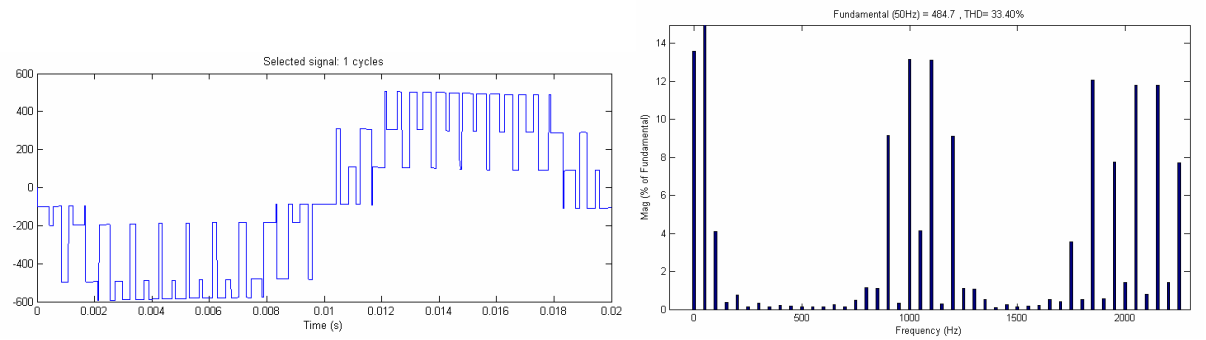


Figure 6-39: 8L-SC2LHB VSC (IGBT) with NEW method (a) line-to-neutral voltage (b) line-to-line voltage (c) phase currents *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*



(a) (b)

Figure 6-40: 8L-SC2LHB VSC (MOSFET) with APOD method (a) line-to-line voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*



(a) (b)

Figure 6-41: 8L-SC2LHB VSC (MOSFET) with APOD method (a) line-to-line voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*

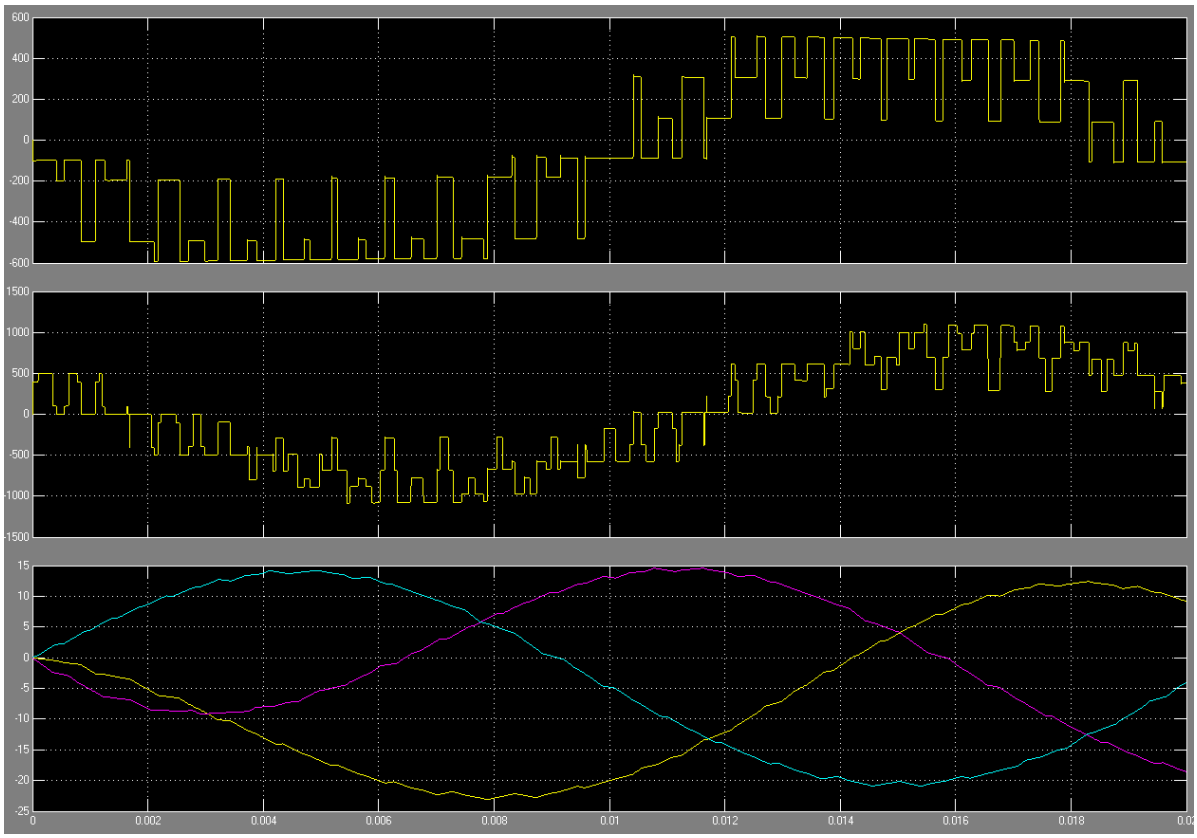
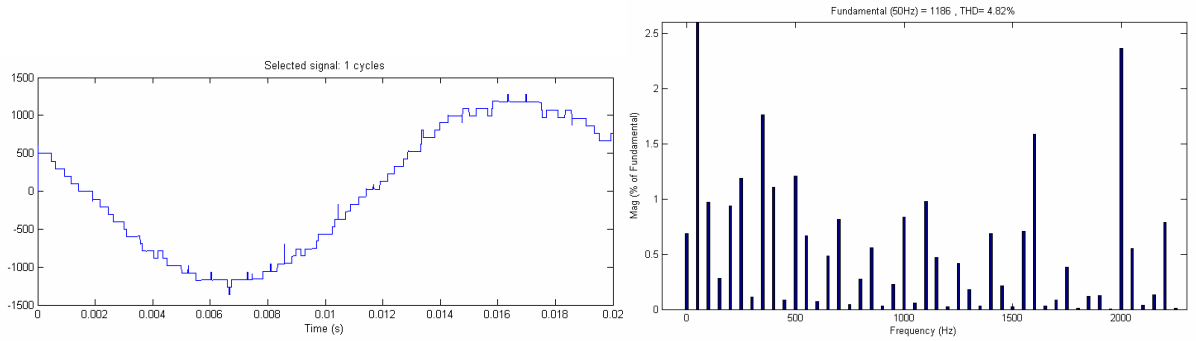


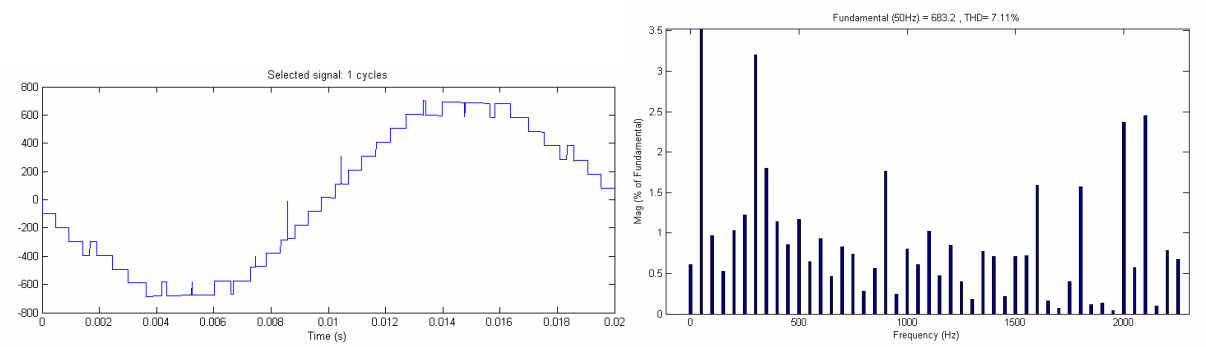
Figure 6-42: 8L-SC2LHB VSC (MOSFET) with APOD method (a) line-to-neutral voltage (b) line-to-line voltage (c) phase currents *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*



(a) (b)

Figure 6-43: 8L-SC2LHB VSC (MOSFET) with NEW method (a) line-to-line voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*

Figure 6-45 shows the line voltage waveform with PWM control and the corresponding harmonic spectrum. The value of THD is 4.82% and meets IEEE 519 limits.



(a) (b)

Figure 6-44: 8L-SC2LHB VSC (MOSFET) with NEW method (a) line-to-neutral voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*

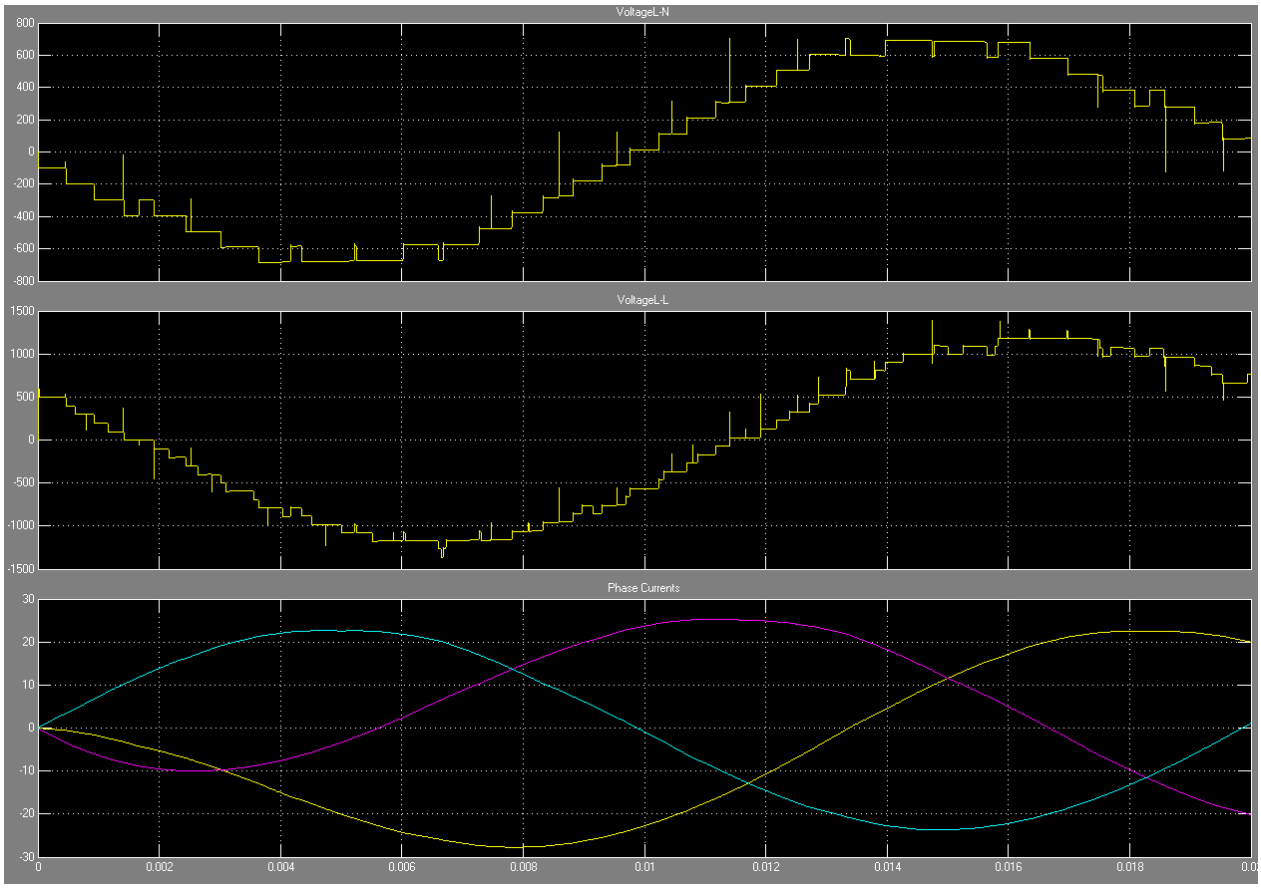
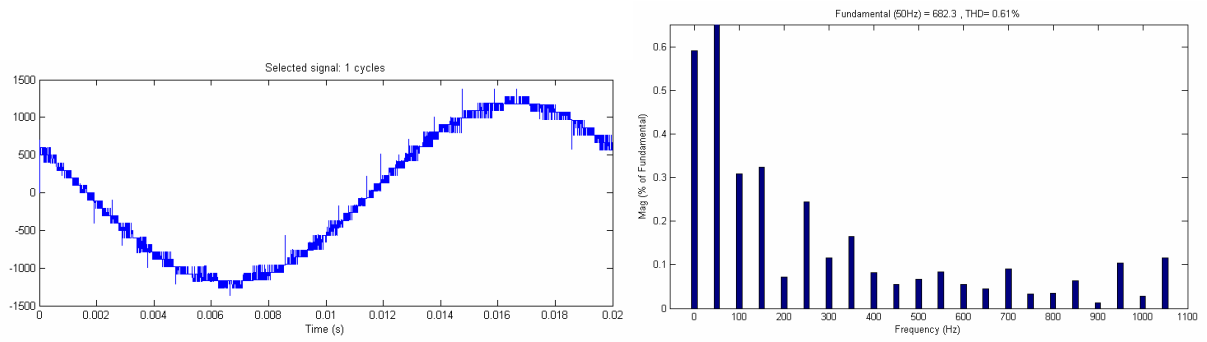


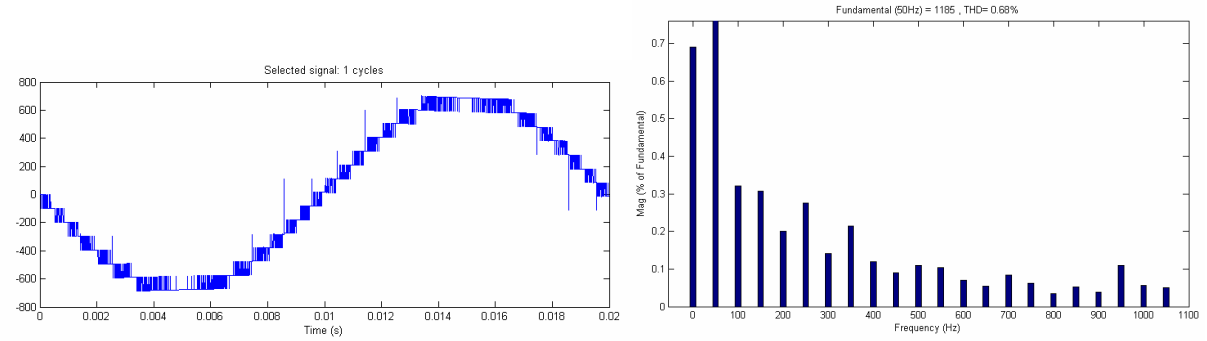
Figure 6-45: 8L-SC2LHB VSC (MOSFET) with NEW method (a) line-to-neutral voltage (b) line-to-line voltage (c) phase currents *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*



(a) (b)

Figure 6-46: 8L-SC2LHB VSC (MOSFET) with NEW method (a) line-to-line voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*

Figure 6-48 shows the line voltage waveform with PWM control and the corresponding harmonic spectrum. The value of THD calculated using Simulink is 0.61% and meets IEEE 519 limits.



(a) (b)

Figure 6-47: 8L-SC2LHB VSC (MOSFET) with NEW method (a) line-to-neutral voltage (b) voltage harmonic spectra *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*

Figure 6-49 shows the phase voltage waveform with PWM control and the corresponding harmonic spectrum. The value of THD calculated using Simulink is 0.68% and meets IEEE 519 limits.

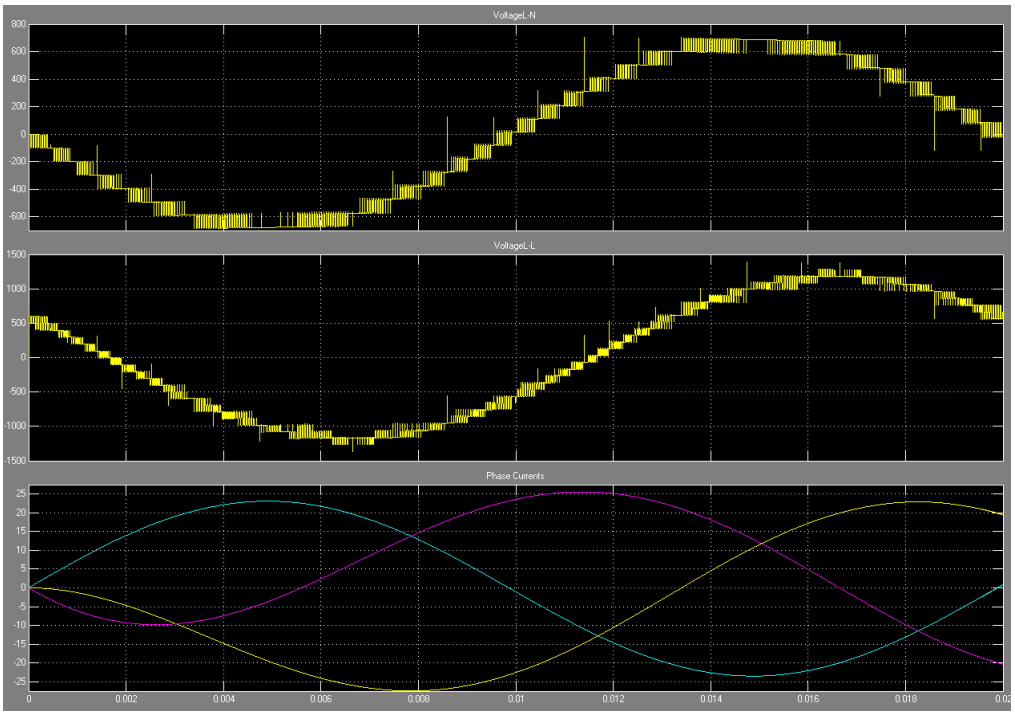


Figure 6-48: 8L-SC2LHB VSC (MOSFET) with NEW method (a) line-to-neutral voltage (b) line-to-line voltage (c) phase currents *(C = 3.3mF, fcar =1100 Hz, fo = 50 Hz, ma = 0.9)*

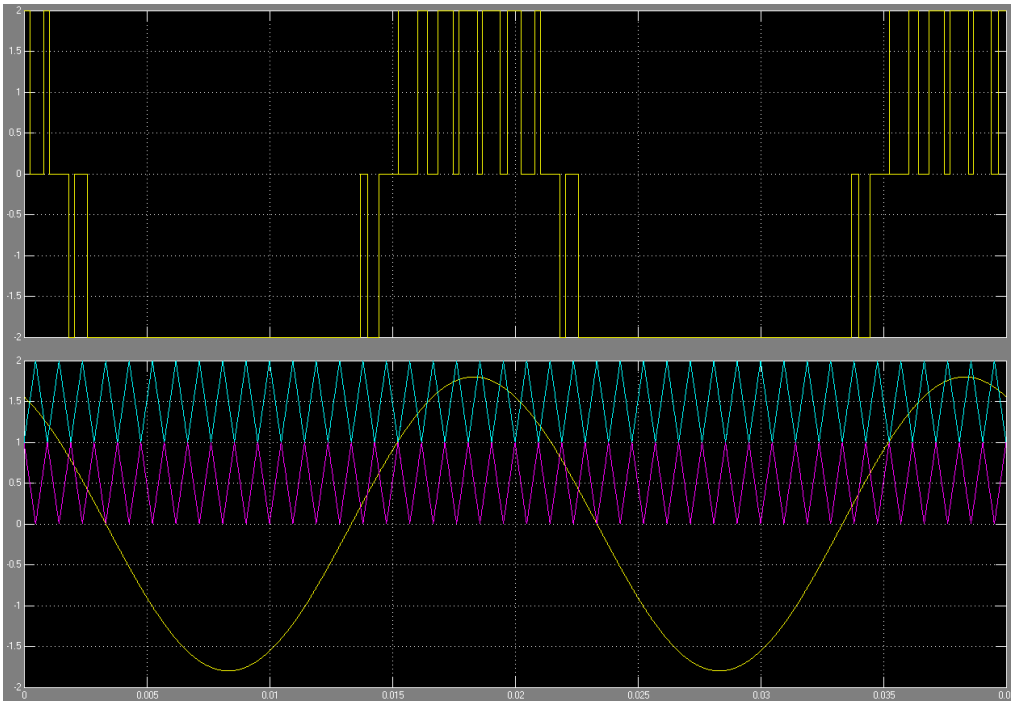


Figure 6-49: Inverter (IGBT /MOSFET cell) participating PWM control. Reference and carriers waveforms of APOD scheme

Table 6-5 Comparison of 8L SC2LHB VSC regarding to IGBTs and MOSFETs

	8L-SC2LHB VSC		
	MOSFET		
	APO	NEW	
	fs=1050Hz m=0.9	fs=1050Hz m=1	fs=8kHz m=1
	THD %	THD %	THD %
Vline-to-neutral	33.4	7.11	0.67
Vline-to-line	28.46	4.82	0.61

The Simulink simulation allows performance study of PM motor drives with control techniques. Table 6-5 presents the areas of performance study and detailed simulation results. From the results it is seen that NEW control technique is superior to APODPWM controller. It is able to maintain the speed error within an extremely small limit. This method also gives lower harmonic contents in utility voltage waveforms. PWM has constant switching frequency. In both methods the voltage THD% is higher than current THD% which demonstrates that the transformer acts like a filter for the high order harmonics (low pass filter). The voltage and currents THD% for both methods are within IEEE 519 recommended limits.

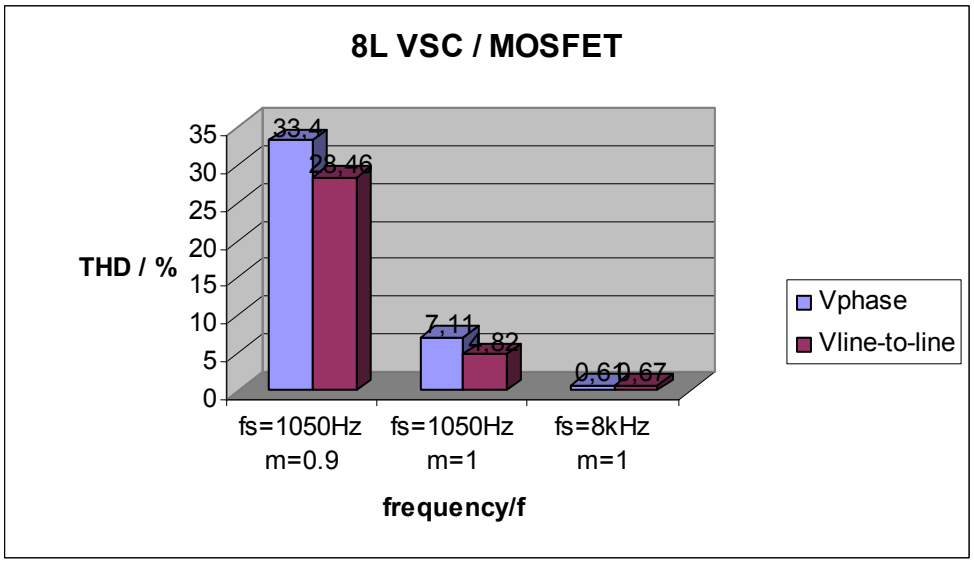


Figure 6-50: Comparison of APOD and NEW modulation techniques within 8L-SC2LHB VSC (IGBT) and 8L-SC2LHB VSC (MOSFET)

The simulation results (regarding the converter losses, the semiconductor loss distribution, the efficiency, and the harmonic spectrum) have been investigated, assuming a maximum junction temperature of $T_{j,\max}$ = 125°C at a phase current of $I_{ph,rms,l}$ = 2.87A and a carrier frequency of f_c = 4 kHz...20 kHz.

7 Conclusions and Future Work

7.1 Conclusions

Computer simulations show that employing the proposed concept results in substantial improvement in the harmonic minimization as well as extending the operating range of the inverter, compared to the conventional methods with common DC source voltage multi-level inverters.

In this thesis, SC2LHB VSCs multi-level converter has been investigated in terms of the feasibility of its utilization in medium voltage applications. The medium voltage drive in the 1.4kVA with voltage rating has been studied, applying 650V MOSFET modules. The modelling of the converter has been derived and the principles of operation that include the structure, the design of the power semiconductor devices and passive components, the design of the dc link capacitor, and the function of the isolation transformer have been discussed.

The weighted total harmonic distortion WTHD of the 8L-SC2LHB VSC was significantly lower than that of other topologies due to the eight-level characteristic of its output voltage.

Another dominant advantage of the SC2LHB is its circuit layout flexibility. Each level has the same structure and there are no extra clamping diodes or voltage balancing capacitors, which are required in the NPC and the FLC topologies. The number of output voltage levels can then be easily adjusted by changing the number of H-bridge cells. Moreover, redundancy can be easily applied to enhance the reliability of the entire system. The high converter switch utilization, the high maximum carrier frequencies, and the low total harmonic distortions of the converter voltage and current are attractive features of the SC2LHB VSC topology, compared to the 3LNPC VSC which is widely used in MV applications today.

Multi-level converters are becoming more attractive in high voltage and high efficiency applications. Because of their multi-step output voltage waveforms, the total harmonic distortion (THD) of the multi-level converter voltages is relatively low compared to the 2L-VSC. Moreover, the effective switching frequency of the multi-level converters is a function of its number of voltage levels. In other words, to achieve the same voltage THD, a higher level converter can operate at a lower switching frequency. Obviously, the theoretical superiority of a multi-level converter is proportional to its number of voltage levels assuming ideal switches. However, the number of voltage levels is limited by its control complexity, complication of the system structure, cost and conduction losses.

The state of the art and developments of 2L and multilevel VSCs for high-power-drive applications is reviewed. The analyzed operating principles, relevant characteristics, established modulation methods, and latest developments of these converters show that all described topologies (2L VSCs, NPC, and CHB) feature specific technical advantages and disadvantages which justify their existence on the market.

Increasing the number of levels does not affect the total voltage blocking capability of the active devices in each phase leg because lower device ratings can be used. The inverter also should be able to shutdown in case of voltage, frequency changes, failure and inverter malfunction.

7.2 Future Work

Future work of the present project includes:

- design and implementation of other control strategies for the utility side converter in order to do a comparison between methods of control
- implementation of harmonic compensation techniques
- utility side inverter control in case of line voltage asymmetry

Finally, innovations in the field of high-power semiconductors and converter topologies, including modulation schemes and redundancy options, will strongly influence the future development of power converters. For any chosen objective function, the optimal switching pattern depends on the desired modulation index. There could be different control algorithms for inverters and filters implemented, even within the same type, thus comparing them with each other will be precious.

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11 List of Abbreviations

Variable	Meaning
$\|Ux\|$	Magnitude of input voltage
1:a	Transformer turn ratio of the output of the second inverter
1:2a	Transformer turn ratio of the output of the third inverter
1:4a	Transformer turn ratio of the output of the first inverter
A, B, C	Output signals of reference voltages
abc	Phase transformation
C2	Secondary side stray capacitance
$\cos\varphi$	Load power factor
Cs	Snubber capacity
Ct	Transversal capacitance
d	Error tolerance
D_1	H-bridge diodes (upper leg A)
D_2	H-bridge diodes (upper leg B)
D_3	H-bridge diodes (lower leg A)
D_4	H-bridge diodes (lower leg B)
E	Total switching losses
E_{dc}	DC voltage
E_{off}	Turn-off losses
E_{on}	Turn-on losses
f_{car}	Carrier wave frequency
f_m	Reference wave frequency
f_o	Converter output frequency
g_s	Logical gate signal
G_t	Transversal conductance
h	Order of harmonics
I^*	Sign of the commanded current
$\hat{i}$	Peak values of the phase current
I_μ	Magnetizing current
I_2	Secondary idling current
I_{abc}	Phase currents
I_c	Collector current
I_{cm}	Maximum collector pulsed current
I_d	Drain current
I_{fe}	Iron core currents
I_g	MOSFET gate-driver's sink/source current
I_1	Load curent
I_{low}	Lower band current
INV_1	First inverter

INV_2	Second inverter
INV_3	Third inverter
i_{ph}	Output phase current
I_{ref}	Reference current
I_{up}	Upper band current
K	Voltage region
L_d	D-axis inductance
L_1	Longitudinal inductance
L_m	Magnetizing inductance
L_q	Q-axis inductance
M	Number of series connected transformers
M_a	Modulation index
m_f	Frequency modulation ratio
N	Turn-ratio of transformer
P_{copper}	Total copper losses
$\hat{i}_{ph}$	Peak value of the phase current
Ph_A	Phase output A
Ph_B	Phase output B
P_{inv}	Total inverter losses
P_o	Idling power
P_s	Short-circuit power
Q_1	H-bridge MOSFET (upper leg A)
Q_2	H-bridge MOSFET (upper leg B)
Q_3	H-bridge MOSFET (lower leg A)
Q_4	H-bridge MOSFET (lower leg)
R	Load resistance
R_1	Resistance of primary side
R_2	Resistance of secondary side
R_{fe}	Resistance of iron core
R_g	Gate resistance
R_m	Magnetizing resistance
R_p	Resistance of primary side
R_s	Short circuit resistance of transformer
S_o	Power transfer value
S_c	Apparent inverter output power
$S_{c,\max}$	Maximum converter output power
t	Time
T_f	Maximum fall time
T_j	Junction temperature

T_{on1}	Control signal for the H-Bridge (upper leg A)
T_{on2}	Control signal for the H-Bridge (upper leg B)
T_{on3}	Control signal for the H-Bridge (lower leg A)
T_{on4}	Control signal for the H-Bridge (lower leg B)
T_r	Rise time
t_{switch}	Switching time
$\hat{u}$	Peak values of the phase voltage
U_2	Secondary capacitance voltage
U_{ag}	Output leg voltages
U_{an}	Line-to-neutral voltage
U_c	Reference of DC-link voltages
U_{c1}	Upper triangular voltage waveform
U_{c2}	Lower triangular voltage waveform
U_{dc}	DC link voltage for 2L-VSC
$U_{dc.\min}$	Minimum dc link voltage
$U_{dc,n}$	Nominal dc link voltage
U_m	Peak input voltage
U_{ng}	Output phase voltage
U_R	Peak value of the reference voltage
V_{abc}	Phase voltages
V_{ce}	Collector-emitter voltage
V_{ds}	Drain-source voltage
V_{gs}	Gate-drain voltage
V_o	Output voltage
$V_{off-set}$	Off-set voltage of function generator
V_{pp}	Peak-to-peak voltage of function generator
w	Fundamental angular frequency
X_h	Leakage reactance
X_p	Reactance of primary side
X_s	Reactance of short-circuit
Z_1	Short-circuit impedance
ΔU_c	DC link capacitor voltage ripples
η	Efficiency
μC	Micro controller
φ	Load current angle

12 Appendix A

Features of ATmega16

• High-performance, Low-power AVR® 8-bit Microcontroller
• Advanced RISC Architecture
– 131 Powerful Instructions – Most Single-clock Cycle Execution
– 32 x 8 General Purpose Working Registers
– Fully Static Operation
– Up to 16 MIPS Throughput at 16 MHz
– On-chip 2-cycle Multiplier
• High Endurance Non-volatile Memory segments
– 16K Bytes of In-System Self-programmable Flash program memory
– 512 Bytes EEPROM
– 1K Byte Internal SRAM

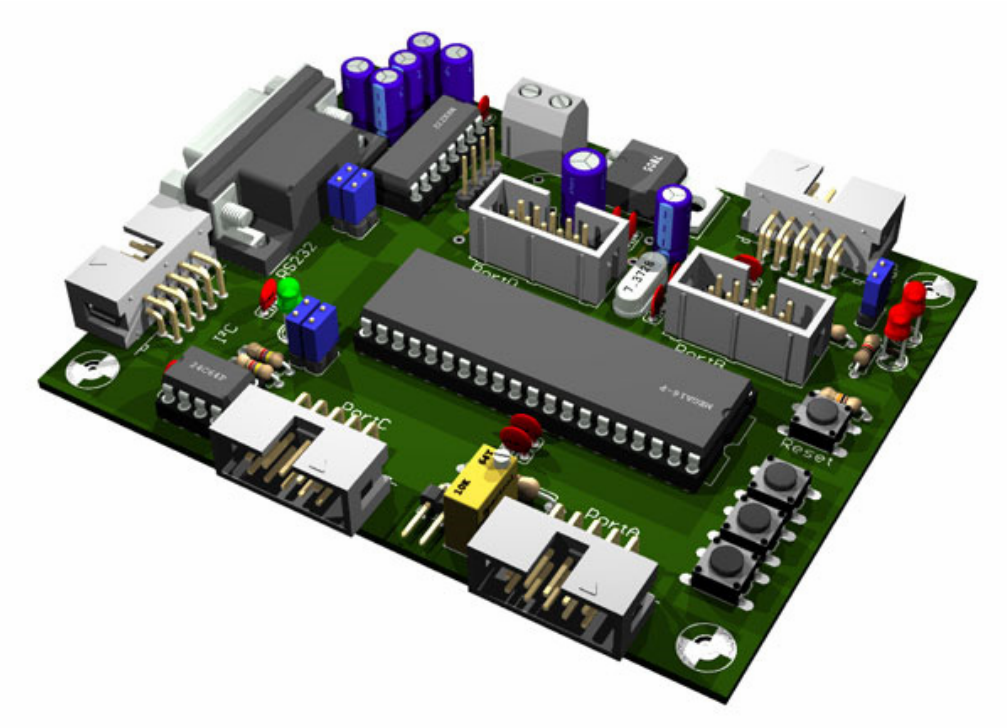

Figure 12-1: ATmega16/32 test board v2.0 [59]

Mode
– Four PWM Channels
– 8-Channel, 10-bit ADC
8 Single-ended Channels
– Programmable Serial USART
– Master/Slave SPI Serial Interface
– On-chip Analogue Comparator
• Special Microcontroller Features
– 32 Programmable I/O Lines
– 40-pin PDIP, 44-lead TQFP, and 44-pad QFN/MLF
• Operating Voltages

– 4.5 - 5.5V for ATmega16
• Speed Grades
– 0 - 16 MHz for ATmega16
• Power Consumption @ 1 MHz, 3V

C-Program of Microcontroller

```
#include <avr/io.h>
#include <avr/signal.h>
#include <avr/interrupt.h>
#include <math.h>

volatile int count;
volatile int ocr = 22;

#define		DDR	DDRC
#define		PORT	PORTC


void init_ports()
{
	DDR = 0xFF;
	PORT = 0xAA;
}

void update_ocr(unsigned int data)
{
	OCR1A = data * ocr - 100;
}

void init_timer()
{
	TCNT1 = 0x00;
	update_ocr(453);// * ocr;
	TCCR1B = (1 << WGM12) | (1 << CS10);

	TIMSK = (1 << OCIE1A);
	sei();
}

int main()
{
	count = 1;
	init_ports();
	init_timer();

	while(1)
		;

	return 0;
}
```

```
SIGNAL(SIG_OUTPUT_COMPARE1A)
{
	// A --> 0101
	// 9 --> 1001
	// 6 --> 0110
	switch(count) {
		case 0:
			update_ocr(454);// * ocr;
			PORT = 0xAA;
			count++;
			break;
		case 1:
			update_ocr(956);// * ocr;
			PORT = 0xA9;
			count++;
			break;
		case 2:
			update_ocr(1122);// * ocr;
			PORT = 0x9A;
			count++;
			break;
		case 3:
			update_ocr(4936);// * ocr;
			PORT = 0x99;
			count++;
			break;
		case 4:
			update_ocr(1122);// * ocr;
			PORT = 0x9A;
			count++;
			break;
		case 5:
			update_ocr(952);// * ocr;
			PORT = 0xA9;
			count++;
			break;
		case 6:
			update_ocr(908);// * ocr;
			PORT = 0xAA;
			count++;
			break;
		case 7:
			update_ocr(950);// * ocr;
			PORT = 0xA6;
			count++;
			break;
		case 8:
			update_ocr(1130);// * ocr;
			PORT = 0x6A;
			count++;
```

```
                        break;
                case 9:
                        update_ocr(4930);// * ocr;
                        PORT = 0x66;
                        count++;
                        break;
                case 10:
                        update_ocr(1120);// * ocr;
                        PORT = 0x6A;
                        count++;
                        break;
                case 11:
                        update_ocr(960);// * ocr;
                        PORT = 0xA6;
                        count++;
                        break;
                case 12:
                        update_ocr(460);// * ocr;
                        PORT = 0xAA;
                        count = 0;
                        break;
        }
}
/*
 * Ex6.1 comparator.c : Analog Comparator
 */

#include <avr/io.h>
#include <avr/interrupt.h>
#include <avr/signal.h>

int main (void)
{
        // set PC4 as output (LED)
        DDRC |= (1 << PC4);
        PORTC &= ~(1 << PC4);

        // set AIN0 (PB2) and AIN1 (PB3) as inputs
        DDRB &= ~( (1 << PB2) | (1 << PB3) );

        // enable interrupt
        ACSR |= (1 << ACIE);

        sei();

        // enable sleep
        MCUCR = (1 << SE);

        while (1)
                asm("sleep");
}
```

```
SIGNAL(SIG_COMPARATOR)
{
	// if AC0 is on ACSR Register set than PC4 to high
	// else PC4 to low
	if ( ACSR & (1 << ACO) )
		PORTC |= (1 << PC4);
	else
		PORTC &= ~(1 << PC4);
}

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% APOD for IGBT [5L SCHB-VSC]
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Max step size
Ta=1e-5;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% VOLTAGE LEVELS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
E1=400 % DC Voltage of H1
E2=400 % DC Voltage of H2
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% IGBT PARAMETERS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Ron=0.01; %Resistance of IGBT
Lon=1e-6 %Inductance of IGBT
Tf=1e-6 % Current 10% fall time
Tt=2e-6 % Current tail time
Vf=1 %the forward voltage of IGBT
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% DIODE PARAMETERS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Ron_Diode=0.01 %resistance the of internal diode, in ohms
Lon_Diode=0
Vf_diode=0.8 % forward voltage of internal diode, in volts (V)
Rs=100; %Snubber resistance
Cs=220e-9; %Snubber capacitance
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% UTILITY PARAMETERS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
L=80e-3; % Load inductance
R=15; % Load resistance
f=50; % grid frequency
%Vr/Vtri
% changing the M causes the change of the output main voltage
M=1.8 %M= Modulation index.
fs=1050 %switching frequency
T= 1/fs
Mf=fs/f %modulation frequency
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% new method for IGBT [5L SCHB-VSC]
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Max step size...
Ta=1e-5
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% VOLTAGE LEVELS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
E1=100 %
E2=200 %
Vtotal=E1+E2
A1=Vtotal/3 % is divided by 3 in case of [5L SCHB-VSC]
A2=(Vtotal/3)*2
A3=Vtotal
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% IGBT PARAMETERS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Ron=0.01 %Resistance of IGBT
Lon=1e-6 %Inductance of IGBT
Tf=1e-6 % Current 10% fall time
Tt=2e-6 % Current tail time
Vf=1 %The forward voltage of IGBT
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% DIODE PARAMETERS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Ron_Diode=0.01 %The resistance the of internal diode, in ohms
Lon_Diode=0
Vf_diode=0.8 %The forward voltage of internal diode, in volts(V)
Rs=100; %Snubber resistance
Cs=220e-9; %Snubber capacitance
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% UTILITY PARAMETERS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
L=80e-3 % Load inductance
R=15 % Load resistance
fgrid=50; % grid frequency
%Vr/Vtri
% changing the M causes the change of the output main voltage
M=1.8 %M= Modulation index.
fs=1050 %switching frequency
T= 1/fs
Mf=fs/f
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [Va,i1] = fcn(i,idot,Iref,DI,Vdc)
% This block supports an embeddable subset of the MATLAB language.
% See the help menu for details.
% this file is written to regulate phase current
%it needs idot, i, Vdc and gives Q as the output
Qa=1;
if Qa==1;
ilower=Iref-DI;
iupper=Iref+DI;
```

```
if (i<=ilower);
Va = Vdc;
elseif (i>ilower)&& (i<iupper) && (idot>=0);
   Va=Vdc;
   elseif (i>ilower)&& (i<iupper) && (idot<0);
      Va=0;%-Vdc;
elseif (i>=iupper);
   Va=0;%-Vdc;
else;
   Va=Vdc;
end
elseif Qa==-1;;% do it for negative phase current here
ilower=Iref-DI;
iupper=Iref+DI;
i=-i;
idot=-idot;
if (i<=ilower);
Va=0;%-Vdc;
elseif (i>ilower)&& (i<iupper) && (idot>=0);
   Va=0;%-Vdc;
   elseif (i>ilower)&& (i<iupper) && (idot<0);
      Va=Vdc;
elseif (i>=iupper);
   Va=Vdc;
else;
   Va=0;%-Vdc;
end
elseif Qa==0;% do it for negative phase current here
      %if current is not zero it should go to zero
      %first write algorithm on the paper' the finish it
if i==0;
   Va=0;
      elseif i>0;
         Va=0;%-Vdc;
      elseif i<0;
         Va=Vdc;
      else;
         Va=Vdc;
      end
else;% not excited, break without doing anything
   Va=Vdc;
end
if Va==0;
   i1=0;
else;
   i1=i;
end
```