Dissertation

Design and fabrication of various MEMS-based structures for investigating thermo-mechanical and fatigue behavior of thin metal films and metal barriers

Montanuniversität Leoben
Department of Materials Physics

Fahimeh Saghaeian

August 2019

Copyright © 2018 by Fahimeh Saghaeian. All rights reserved.

Infineon Technologies Austria AG

Siemensstrasse 2

9500 Villach

Austria

https://www.Infineon.at

Affidavit

I declare in lieu of oath that I wrote this thesis and performed the associated research myself, using only literature cited in this volume.

August 2019, Fahimeh Saghaeian

Acknowledgements

This work would not have been possible without support of colleagues at Infineon Technologies and material physics department of Leoben University. Years of my PhD was a great challenge, which led to improve my scientific knowledge and growth of my personality. For that, I would like to express my gratitude to the following people.

First of all, I express my sincere gratitude towards Prof. Jozef Keckes for his professional support and guidance throughout entire duration of my studies. I whole-heartedly thank him for his supervision and moral behavior, which has widened my horizon and made this thesis a success.

Secondly, I would like to thank Mr. Manfred Frank. Only with his support and perfect management, I was able to overcome many difficulties during these years of my studies. Additionally, I thank Dr. Wolfgang Diewald for offering me a PhD position and Dr. Elmar Aschauer for giving me a chance to be part of his group. I thank Dr. Kai Schreiber for his supervision to overcome challenges in this work.

I am indebted to Prof. Golta Khatibi from TU Wien for sharing her knowledge, experience and giving me a chance to collaborate with her group as well as using lab facilities at TU Wien.

I would like to thank many colleagues at Infineon Technologies Austria and Germany for their constant help. Few of those are Dr. Andreas Behrendt, Dr. Stefan Woehlert, Dr. Petra Fischer, Dr. Johannes Zechner, Mr. Heimo Hofer, Dr. Juergen Walter and many more.

I would like to express my deepest thankfulness and feelings to my mom and dad, without their teachings, encouragement and sacrification, I could never be the person whom I am now. I owe my success and my personality to them. It is also worth to mention name of Sara, my beloved sister, for her long lasting sentimental support.

Finally, I would like to thank profoundly to my soul mate Ravi who walked side by side in every step of my PhD life like a real companion. His kindness, moral help and pure love is strength of my life.

به دانش فزای و به یزدان گرای	که او باد جان ترا رهنمای
بپرسیدم از مرد نیکو سخن	کسی کو بسال و خرد بد کهن
که از ما به یزدان که نزدیکتر	که را نزد او راه باریکتر
چنین داد پاسخ که دانش گزین	چو خواهی ز پروردگار آفرین

"فردوسی، شاعر ایرانی (۳۲۹ ه ق-۴۱۶ ه ق)"

Increase your knowledge and walk towards divinity that it is guidance for your soul

I asked from a wise man, who was the idol and his knowledge was old,

That who is closer to divinity than us, who has most narrow path to it

He replied me, increase your knowledge, that even divinity will accolade you.

"Ferdowsi, Persian poet (940-1020)"

Abstract

The multidisciplinary semiconductor industry utilizes various thin films of metal, oxides or nitrides etc. to improve performance of MOSFET devices. Especially, metal thin films are predominantly used to create a network of integrated circuit on a chip, as well as supplying a path for heat dissipation. For this particular case, a stack of power metal and diffusion barrier is employed which is required to cope with a repetitive thermo-mechanical loading. It is thus important to investigate the material properties of metals and barriers in detail to evaluate the extent of deformation under a thermo-mechanical load, the interfacial adhesive strength or endurance against cyclic fatigue load. This demands a proper methodology to study thin films, and determine the impact of processing conditions on their material properties. The present work focuses on developing a variety of MEMS based test structures to enable characterization of thin metal films.

Using a semiconductor on insulator technology, a fabrication process was developed to manufacture different MEMS structures such as; beams, cantilevers, curved cantilevers, theta and plus shaped structures with varying aspect ratios. A metal film was deposited on these structures, either including the sidewall, or else it was structured in such a way as to give MEMS structures with metal-free sidewalls. The process offers the possibility to change dimensions of structures, the stack and thickness of metal films, or the interface with substrate.

Following this, thermo-mechanical behavior of thin copper films was investigated using curved cantilever and plus shaped structures. Using data obtained during in-situ high temperature cycling, the deflection of structure was plotted against the temperature, revealing the typical hysteresis curve depicted by copper. The amount of deflection and therefore area of hysteresis curve was found to increasing either with the increasing thickness of copper, or with the dimensions of the structure.

Secondly, by using nano-indentation technique, mechanical properties of Cu-TiW stack were evaluated. The composite cantilever of Si-TiW-Cu was subjected to different annealing temperatures prior to testing under fracture load. Annealed copper films showed significant reduction in load to fracture in comparison to a deposited film. Grain growth and reorientation of copper grains during annealing are the major reasons for reduction in the fracture strength of Cu films.

In a subsequent study, plus shaped structures were used to evaluate the fatigue behavior of thin copper films. Using a piezo electric shaker, a thin copper film deposited on plus shaped

structures was subjected to cyclic fatigue load at the resonant frequency of structure. The fatigue deformation was concentrated at either ends of beams revealing typical signatures such as slip lines, extrusions, grain growth and grain reorientation. The plus structure was found to be an excellent tool for the characterization of fatigue behavior of thin films.

Finally, morphology of TiW film was investigated to understand functionality of TiW as a diffusion barrier. TiW films of two different stoichiometries and residual stress levels have been analyzed to illustrate differences in their microstructures. The thickness dependent stress gradient was determined in tensile films, while the same in compressive films was relatively constant. The stress level was influenced by the energy of plasma during deposition, confirming the Thornton model.

The present study pave a platform for characterization of thin metal films using MEMS based structures. In this work, a process to fabricate these structures was developed and selected structures were characterized under various loading conditions. This approach opens the possibility of studying properties of bilayers and thin film interfaces as well as investigating the impact of various process steps on the microstructure, residual stresses and thereby on device characteristics.

Zusammenfassung

Die Halbleiterindustrie verwendet verschiedene Dünnschichten aus Metallen, Oxiden oder Nitriden usw., um die Leistung von MOSFET-Bauteilen zu verbessern. Insbesondere Metallschichten werden oft verwendet, um Netzwerke integrierter Schaltkreise auf einem Chip zu erzeugen und um Wärmeableitung sicherzustellen. Es werden Schichtstapel, bestehend aus Leistungsmetall und einer Diffusionsbarriere angewandt, die wiederholte thermomechanische Belastung aushalten müssen. Es ist daher wichtig, die Materialeigenschaften des Metalls und der Barriere zu untersuchen, um das Verformungsausmaß unter solcher Belastung, die Grenzflächenhaftung, oder die Ermüdungsfestigkeit zu bewerten. Dafür wird eine geeignete Methode benötigt, um verschiedene Schichten und die Auswirkungen von Prozessbedingungen auf ihre Materialeigenschaften zu untersuchen. Die vorliegende Arbeit beschäftigt sich mit der Entwicklung von MEMS Teststrukturen zur Charakterisierung dünner Metallfilme.

Basierend auf der „silicon on insulator“ Technologie wurde ein Verfahren etabliert, um verschiedene MEMS Strukturen wie Balken, Kragbalken, gekrümmte Kragbalken, theta- sowie plusförmige Strukturen mit verschiedenen Formfaktoren herzustellen. Metallschichten wurde auf den Strukturen einschließlich ihrer Seitenwände abgeschieden. Für metallfreie Seitenwände wurden diese danach weiter strukturiert. Das Verfahren bietet die Möglichkeit zur Einstellung der Strukturabmessungen, der Dicke und Schichtfolge der Metallfilme und deren Grenzfläche zum Substrat.

Zunächst wurde das thermomechanische Verhalten eines dünnen Cu-Films mittels plusförmiger Strukturen und gekrümmter Kragbalken untersucht. In einem in-situ Hochtemperaturzyklus wurde die Durchbiegung der Struktur mit der Temperatur gemessen, welche die für Cu typische Hysterese zeigt. Es wurde festgestellt, dass die Auslenkung bzw. die Fläche der Hysteresekurve mit zunehmender Dicke des Kupfers sowie der Größe der Struktur zunimmt.

Als nächstes wurden die mechanischen Eigenschaften eines Cu-TiW-Stapels mithilfe von Nanoindentation ausgewertet. Vor einem Bruchtest wurden die aus dem Schichtstapel und Substrat bestehenden Kragbalken thermisch belastet. Der unbehandelte Cu-Film zeigt im Vergleich zu wärmebehandelten Cu-Filmen eine höhere Bruchlast. Kornwachstum und Neuorientierung der Cu-Körner während der Wärmebehandlung sind Hauptgründe für diese Festigkeitsverringerung.

In einer weiteren Studie wurde das Ermüdungsverhalten dünner Cu-Filme untersucht. Mit einem piezoelektrischen Rüttler wurden die Filme auf plusförmigen Strukturen bei deren jeweiligen Resonanzfrequenzen einer zyklischen Belastung auszusetzen. Ermüdungserscheinungen waren an den Enden der Trägerarme lokalisiert und bestanden aus Gleitlinien, Extrusionen, Kornwachstum sowie Kornrotation in den Cu-Filmen. Plusförmige Strukturen erwiesen sich als hervorragend geeignet zur Charakterisierung des Ermüdungsverhaltens von Dünnschichten.

Um schließlich die Funktionalität von TiW als Diffusionsbarriere zu verstehen, wurde die Filmmorphologie untersucht. TiW-Filme mit zwei verschiedenen Stöchiometrien und Eigenspannungsniveaus wurden analysiert, um die Unterschiede zwischen ihren Gefügen zu bestimmen. Ein dickenabhängiger Eigenspannungsverlauf wurde in der Schicht mit Zugspannung beobachtet. Andererseits blieb in der Schicht mit Druckspannung diese ziemlich konstant. Das Eigenspannungsniveau war stark durch die Plasmaenergie des Abscheideprozesses bestimmt. Das bestätigt das Thornton-Modell.

Die vorliegende Arbeit dient als Grundlage zur Charakterisierung von Dünnschichten mithilfe von MEMS-basierten Strukturen. Es wurde ein Verfahren zur Herstellung dieser Strukturen etabliert und ausgewählte Strukturen wurden unter verschiedenen Belastungen untersucht. Das Verfahren ermöglicht die Untersuchung der Eigenschaften von Schichtaufbauten und Grenzflächen, sowie des Einflusses verschiedener Prozessparameter auf das Gefüge, Eigenspannungen und in weiterer Folge auf funktionale Eigenschaften.

Contents

Affidavit i

Acknowledgements iii

Abstract vii

Zusammenfassung ix

1. **Introduction** 1

2. **Semiconductor devices : MOSFET** 5

   2.1 General structure of MOSFET 5

   2.2 Operation of MOSFET device 6

   2.3 Power dissipation in power MOSFET device 8

3. **Application of metals in MOSFET** 11

   3.1 Ohmic / Schottky contact metals 11

   3.2 Metal barrier 12

      3.2.1 Metal nitride based barriers 14

      3.2.2 Self-forming barrier 17

      3.2.3 TiW barrier 18

4. **Interconnect metal** 21

   4.1 Choice of interconnect metal : Copper 21

   4.2 Deposition technique for copper metal 24

      4.2.1 Physical vapor deposition (PVD) 24

      4.2.2 Plating of thin copper films 27

   4.3 Properties of copper 30

      4.3.1 Film growth and crystal orientation 30

      4.3.2 Electro migration of copper 32

4.3.3 Thermo-mechanical behavior ... 33

5. **Micro electro mechanical systems (MEMS)** ... 36

5.1 Introduction to MEMS ... 36

5.2 MEMS fabrication techniques ... 38

5.2.1 Surface micromachining ... 38

5.2.2 Bulk micromachining ... 39

5.2.3 Focused ion beam milling (FIB) ... 40

5.2.4 Silicon on insulator (SOI) technology ... 41

5.3 Application of MEMS structure for material characterization ... 41

6. **Summary and conclusion** ... 45

7. **List of appended publications** ... 55

7.1 Contribution of the author to the papers ... 56

Paper A: Design and development of MEMS-based structures for in-situ characterization of thermo-mechanical behaviour of thin metal films ... 57

Paper B: Fabrication of MEMS based structures for characterization of thin metal films by nanoindentation technique ... 71

Paper C: Investigation of high cyclic fatigue behaviour of thin copper films using MEMS structure ... 81

Paper D: Microstructure and Stress Gradients in TiW Thin Films Characterized by 40nm X-ray Diffraction and Transmission Electron Microscopy ... 103

1. Introduction

Metals have prominent applications in almost every field of science and technology. Choice of metal for a particular application is mainly driven by its requirement such as high mechanical strength, high ductility, high fracture toughness, or resistance to oxidation etc. Among all of its properties, metals are known to be excellent conductor of heat and electricity. In last decades, advances in microelectronic industry kept demand for metals for various applications quite high to serve only purpose of transporting electric charge from one end to another end of the device [1]. Various metals are frequently used in semiconductor devices for countless applications such as, forming an ohmic contact to semiconductor material, interconnect joints, vias, diffusion barriers, heat storage etc. [2,3]. Usage of proper metal has not only helped to improve the performance and reliability of semiconductor devices but also has enabled miniaturization of transistor devices [3]. Although by shrinking the device dimensions, transistors have improved their switching performance, it had two major impacts on metals used. First, the current density, a metal thin film needs to withstand, has been increased and second, thermal management of device has become essential [3,4]. Furthermore, application field of semiconductor devices has broadened from simple logic devices to automotive applications where high reliability is demanded [5]. It makes choice of metal for such applications more critical. In order to fulfill this requirement, it is very important to understand various aspects of transistors operation, which induce different kinds of load on thin metal films. In addition to it, a dedicated platform is needed to be developed for testing thin metal films in similar conditions.

Metal oxide semiconductor field effect transistor (MOSFET) is an electrical device which means resistance of the device leads to losses and those are ultimately converted into thermal energy or heat [6,7]. During operation of the MOSFET device, there are situations such as turn on/off, rate of switching, short-circuit conditions etc. which results into heat generation in the device and the rate of this heat generation is different in every situation [5,7]. In short, before investigating thin metal films for its performance in MOSFET device, it is needed to get a basic understanding about operation of MOSFET device. Chapter 2 gives a brief introduction on basic elements of MOSFETs, functionality of the device, different working conditions and a short summary on power losses during its operation.

On a similar path, it is needed to understand precise requirements; the field of semiconductor world has from metals. Among many, metals are used for two major applications in MOSFET devices namely; diffusion barriers and metallization. Diffusion

barrier is a layer of thin metal film sandwiched between device elements and metallization to hinder the reaction between them without having a noticeable influence on the electrical performance of device [3,8]. Furthermore, it also serves the purpose of good adhesion promoter between device elements and top metal layer. On the other hand, aluminum or copper are most commonly used metals for metallization purposes in semiconductor field. As copper supersedes aluminum in various material properties, it is currently a favorite candidate for the metallization [1,3]. However, various parameters such as deposition processes, pre-cleaning, application requirements and influence of forthcoming processes etc. effect the microstructure of thin films, their interfaces or adhesion strength. Therefore, prior to investigation of metals, a concise overview elaborating their material properties, various deposition methods and intrinsic properties of metals and barrier are summarized in third chapter.

Moreover, properties of thin films differ from their bulk properties [1,9]. In addition to it, varying interfaces or different loading conditions makes it cumbersome to investigate metal properties in micron regime. This demands a dedicated methodology with which one can precisely evaluate the impact of different influences on performance of thin metal film. Here, micro-electro mechanical systems (MEMS) based structures are quite useful. Many studies have already proven the potential of this approach for characterization of thin films [10-12]. For this purpose, structures such as beams, cantilevers and membranes are commonly used to study the material properties of thin metal films. However, these traditional structures such as beams or cantilevers are not sufficient enough to quantify the impact of various parameters listed above on the performance of thin metal films for semiconductor applications. This is because, not only the material interface plays a role in functionality of thin metal films but also loading conditions in MOSFET applications are very different than standard measurement techniques such as nano-indentation. It means there is a need to design dedicated structures on which operating conditions of MOSFET can be simulated and thereby performance of thin metal film can be evaluated for those specific conditions. Prior to do that, a broad review, highlighting major aspects of MEMS and its application potential in field of thin film characterization, is summarized in the last chapter of the introduction.

The current work represents a consolidated approach to design, develop and fabricate MEMS based structures and utilize them for in-situ characterization of thin metal films. In first research study, using silicon on insulator (SOI) technology, various structures such as beams, cantilevers, curved cantilevers, theta shaped structures and plus shaped structures of

varying dimensions or aspect ratios have been fabricated. Thereafter based on two structures namely, plus structure and curved cantilever, thermo-mechanical behavior of thin copper film was investigated in an in-situ mode using optical profilometer. In the second article, cantilever structures are used to study the mechanical properties of thin copper films and variation of fracture load in correlation with its grain size. In the third publication, by using plus shaped structures, fatigue behavior of thin copper film was studied. Experimental investigation on different thicknesses of copper thin film together with finite elemental simulation revealed that plus shaped structure is an excellent design to locally induce high stress in thin metal film under cyclic load. Finally, in the fourth publication, most commonly used TiW diffusion barrier was investigated using high-energy X-ray nanodiffraction at Grenoble synchrotron facility to correlate its morphology with the intrinsic stress gradients. This provides vital information about functionality of TiW barrier. In summary, various MEMS structures fabricated here offer a broad platform for in-situ investigation of thin metal films.

References

1. Gupta, T., *Copper Interconnect Technology*2008: McGraw-Hill Professional Publishing.
2. Murarka, S.P., *Multilevel interconnections for ULSI and GSI era.* Materials Science and Engineering: R: Reports, 1997. **19**(3): p. 87-151.
3. Shacham-Diamand, Y., et al., *Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications*2009: Springer-Verlag New York.
4. Rosenberg, R., et al., *Copper Metallization for High Performance Silicon Technology.* Annual Review of Materials Science, 2000. **30**(1): p. 229-262.
5. Nelhiebel, M., et al., *Effective and reliable heat management for power devices exposed to cyclic short overload pulses.* Microelectronics Reliability, 2013. **53**(9): p. 1745-1749.
6. Hoffmann, K., *System Integration: From Transistor Design to Large Scale Integrated Circuits*2006: Wiley
7. Ytterdal, T., Y. Cheng, and T.A. Fjeldly, *Device Modeling for Analog and RF CMOS Circuit Design*2003: Wiley.
8. Kaloyeros, A.E. and E. Eisenbraun, *Ultrathin Diffusion Barriers/Liners for Gigascale Copper Metallization.* Annual Review of Materials Science, 2000. **30**(1): p. 363-385.
9. Arzt, E., *Size effects in materials due to microstructural and dimensional constraints: a comparative review.* Acta Materialia, 1998. **46**(16): p. 5611-5626.
10. Nazeer, H., et al., *Determination of the Young's modulus of pulsed laser deposited epitaxial PZT thin films.* Journal of Micromechanics and Microengineering, 2011. **21**(7): p. 074008.
11. Lalinský, T., et al., *Thermo-mechanical analysis of uncooled La0.67Sr0.33MnO3 microbolometer made on circular SOI membrane.* Sensors and Actuators A: Physical, 2017. **265**: p. 321-328.
12. Nazeer, H., et al., *Residual stress and Young's modulus of pulsed laser deposited PZT thin films: Effect of thin film composition and crystal direction of Si cantilevers.* Microelectronic Engineering, 2016. **161**: p. 56-62.

2. Semiconductor devices : MOSFET

2.1 General structure of MOSFET

Metal-Oxide-Semiconductor field effect transistor (MOSFET) is basically a highly efficient switch made out of semiconductor material. The device consists of three major constituents namely, source, drain and gate. Metals are often used to contact these three major elements to outer world. Gate is commonly made up of silicon dioxide, while source and drain are made up of highly doped semiconductor material. The basic structure of the MOSFET is as shown in figure 1. The name field effect transistor is derived from a fact that, by applying electric field on the gate oxide, a conductive channel can be formed between source and drain. Through this channel, electrons can flow and device is in on state. By changing

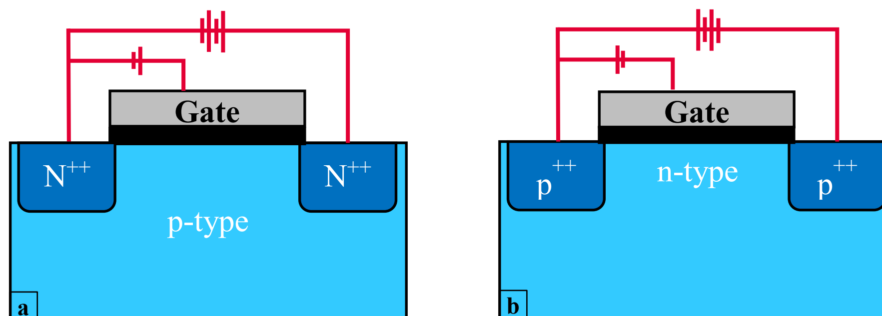

Figure 1. Schematics showing basic elements of (a) N-MOSFET and (b) P-MOSFET. Dark blue areas mark source and drain structures made by high doped regions.

applied electric field on the gate oxide, conductivity of formed channel can be manipulated. Device state can be changed from fully on condition to off state simply by turning off the applied gate voltage. Basically by change of applied field, transistor conductivity can be tuned and thus named as Field effect transistor. In most of the modern MOSFETs, silicon and silicon dioxide are widely used as semiconductor and gate oxide material respectively. However, various other semiconductor materials such as gallium nitride (GaN), gallium arsenide (GaAs), silicon carbide (SiC), etc. are also intensively studied for MOSFET applications [1].

MOSFETs are further classified into two types (1) N-MOSFET and (2) P-MOSFET. From structural point of view, these two types are complementary to each other. It means, in N-MOSFET, source and drain are made up of highly n doped silicon, while the body region in which conductive channel forms is of p type. On the other hand, in P-MOSFET

source and drains are made out of p doped island and the body is made up of n type semiconductor material. This means, electrons in N-MOSFET and holes in P-MOSFET are charge carriers. By combining N and P MOSFET together, complementary MOS (CMOS) transistors can be built up for logic applications.

2.2 Operation of MOSFET device

MOSFET device can be turned on and off by controlling the applied gate voltage. However, based on gate voltage applied, the state of MOS structure can be classified into three different conditions, namely accumulation, depletion and inversion (see figure 2). The explanation given here is for N-MOSFET, which would be same for P-MOSFET with opposite value of gate voltage. In N-MOSFET device, accumulation is a state where negative gate voltage ($V_{gs} < 0$) attracts holes in semiconductor towards the interface of the gate oxide and semiconductor. By increasing the negative voltage, more and more holes are accumulated at gate increasing hole density. If voltage is reversed ($V_{gs} > 0$), positive gate voltage repels positively charged holes from surface into the bulk, creating holes depleted region. Thus, this state is called “Depletion”. As a matter of fact, in this depleted region electrons are accumulated along the gate oxide. By increasing the gate voltage, more and more electrons are accumulated and depletion region keep on increasing. Upon having sufficient positive gate voltage, a conductive channel of electrons is formed between source and drain region. Through this channel, under the influence of applied drain voltage, electrons starts flowing from source to drain. The gate voltage at which conductive channel is formed and current starts to flow is called as threshold voltage. It is represented by symbol V_{th}. At gate voltage higher than threshold voltage the MOSFET is in the third state called “inversion”. The value of threshold voltage depends on numerous parameters, but mainly decided by the thickness of gate oxide and dopant concentration of the body region. The equation for threshold voltage is given in equation 1.

$$\boldsymbol{V_{Th} = V_{FB} + 2\emptyset_F + \frac{\sqrt{2qN_a 2\varepsilon_s 2\emptyset_B}}{C_{ox}}} \qquad (1)$$

Where V_{FB} = flat band voltage, $2\varphi_F$ = Fermi voltage, q = N_a = dopant concentration, C_{ox} = capacitance of gate oxide

MOSFET device consists of gate electrode, gate oxide and semiconductor material and they act together as a parallel plate capacitor that can be charged or discharged. If capacitance of the device is plotted against applied gate voltage, it depicts all three states of

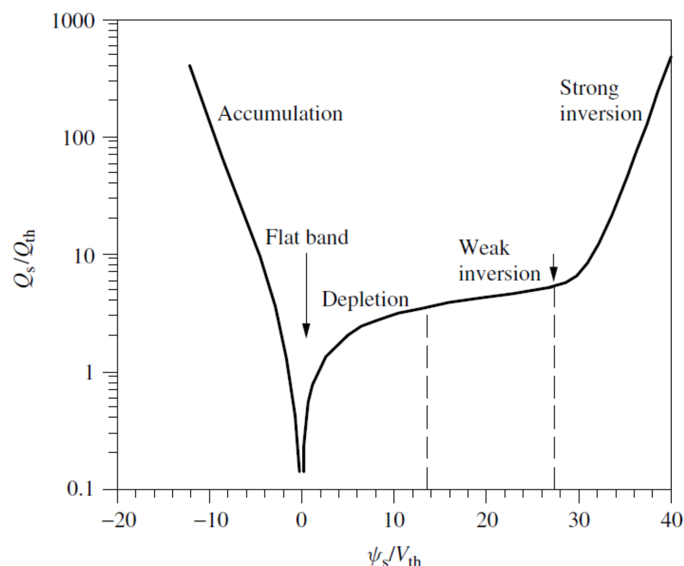

Figure 2. A plot showing normalized semiconductor charge per unit area against surface potential. Plot shows different states of MOSFET as a function of applied gate voltage. [3]

the MOSFET [2]. The voltage that separates the accumulation and depletion region is called flat band voltage. This is the voltage where, there is no charge in the capacitor or no electric field on the oxide. Depletion and inversion regions are demarcated by threshold voltage. With the further increase of gate voltage, the MOS transistor can be driven into deep depletion zone.

During normal operation of MOSFET device, when gate voltage is more than threshold voltage, under the influence of source-drain (V_{SD}) voltage, current starts to flow between source and drain. By altering the gate voltage, this electron density between source and drain can be tuned and by doing so one can control the conductance of channel or current through the device. However, at given gate voltage ($V_{gs} > V_{th}$), initially device current tends to increase with increasing drain voltage (V_{DS}), but at the same time, reduction in gate-channel bias especially close to drain takes place. With further increase of drain voltage, a state called "pinch off" is reached. After this point, further increase in V_{DS} voltage will not result into any increase in the device current. A plot showing device current for various values of source-drain voltage is as shown in figure 3 [3]. For given gate voltage, the voltage at which device current reaches the saturation value is called saturation voltage (V_{DSsat}). The equation for saturation voltage is stated in equation 2. From the equation, it is clear that, in order to drive higher current through the device, higher gate voltage is needed to be applied.

$$V_{DSsat} = V_{GS} - V_{Th} \qquad (2)$$

Where V_{GS} = Gate source voltage and V_{Th} = Threshold voltage

MOSFET devices are basically designed for logical or power applications. In logical devices, N and P-MOSFETs are designed complementary to each other and thus called

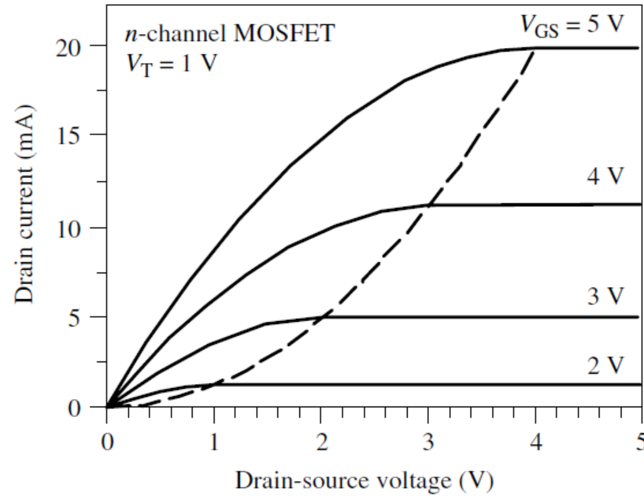

Figure 3. A plot showing current-voltage characteristics of N-MOSFET for varying gate voltages. [3]

complementary MOS (CMOS) devices. The application demands fast turning on and off the device while voltage supported by device or current flowing through the device is relatively small. On the other hand, power devices are designed for supporting very high voltage and high current densities. The typical applications for such MOSFETs are in motor drivers, invertors, power supply units etc. It is a general trend to decrease the dimensions of the MOSFET device to increase its performance, thus MOSFETs are being designed for higher and higher power densities. Although it makes the device efficient in performance, the electric field across every element of the MOSFET such as gate oxide, semiconductor, source, drain etc. is increasing which lead to higher thermal budget; the system has to deal with. This demands a very efficient cooling system by using thin metal films. (In paper A, thermomechanical behavior of thin metal film is studied under sudden heating-cooling condition.)

2.3 Power dissipation in power MOSFET device

During operation of the MOSFET device, various situations result into power dissipation or energy loss. The dissipated electrical energy is directly converted into the thermal energy,

resulting into increase in device temperature [3]. Such a temperature shootout would be detrimental for the device performance as well as for lifetime of the device. In numerous cases, the increase in temperature is so high and local, that it can lead to meltdown of certain device parts. The current chapter highlights few of those scenarios that can lead to the increase in device temperature and thereby affect its performance.

Power MOSFET device is designed for certain maximum operating current in “turn on” mode. Resistance of the device in this mode is responsible for losses in electrical energy [4]. Furthermore, when device is turned off or operated in reverse direction, additional energy loss takes place due to voltage drop across PN junction. Not needed to mention, that the losses will be higher with continuous fast switching between operational modes. Thus all these parameters increase temperature of the device or in other words, the maximum current that can be allowed through device will determine by maximum permissible channel temperature.

Performance of MOSFET device is improved by simply scaling down the device dimensions as per Moore’s law. The disadvantage of this miniaturization is the increase in power densities across the device elements such as source, drain or gate electrodes [5]. It means higher current density will increase temperature of the device. Under such conditions, if the device is not cooled down properly, temperature can shoot up to several hundreds of degrees locally, resulting into the device malfunctioning.

Thermal breakdown of the device in avalanche operation is also a common mode of device failure [1,2]. If voltage applied across source and drain is higher than the permissible value, charge carriers are created by breaking the covalent bonds between silicon atoms in a semiconductor material. This leads to flow of current or energy loss resulting in temperature shoot up. If the applied field is very high, increase in undesirable current flow is high enough to shoot up the channel temperature above permissible value and as consequence, device destruction occurs.

The MOSFET is required to withstand certain number of short circuit events during its lifetime. Short circuit in MOSFET device means a sudden increase in output current in event of lack of designed output load. This makes MOSFET device to handle enormous amount of current and very sudden increase in device temperature [4,6]. Depending on application of device, short circuit time can be in a range of few microseconds. The sudden increase in device current heats up the device and duration of event is too short to transport the heat from MOSFET to outer world. In addition to it, due to sudden and enormous increase in temperature, leakage current is generated, affecting electrical performance of

device. Likewise, high thermal budget has impact on the material properties of various elements of MOSFET device. This can lead to degradation of ohmic contact, delamination between metal and semiconductor, or even a strong local melting of the device elements [1,3,6].

In summary, energy losses in MOSFET device due to various aspects cause increase in device temperature, which is detrimental due to various reasons. Therefore, an active heat management in the MOSFET device is a pertinent factor to its high performance and guaranteed operation over its life time [4,6,7]. In order to cool the device and drive away the heat generated in the semiconductor elements, thin metal films are deployed. Thin metal films acts as a heat sink. It means, during temperature shoot up, metal films absorb this heat limiting the temperature shoot up in device well below permissible limit. It is thus evident that metals, those having higher thermal conductivity, higher thermal heat storage capacity and can be possibly be deposited to higher thicknesses in a cost effective way, are ranked high for such applications. In past years aluminum in form of AlSiCu or AlCu alloys have been chosen, while currently the trend is to use thicker copper thin films [4,5,7]. Upcoming chapters will give more insight into this topic. Further, on in paper A, such an effect of high temperature on the metals in devices has been studied. The study also shows extent of deformation silicon has to undergo under the influence of copper.

3. Application of metals in MOSFET

Metals are integral part of MOSFET device and in current state of art different metals find numerous applications in current MOSFET devices [5,8]. Large number of metals like aluminum, copper, gold, titanium, tantalum, tungsten, molybdenum, nickel, cobalt and many others are used for various applications such as forming ohmic or schottky contacts, forming interconnects, metal barriers, diffusion barriers, via filling metals etc. [5,8,9]. Right after the birth of MOSFET technology, highly doped poly silicon was used as a gate electrode. However, as technology started getting complex, conductivity of poly silicon was not sufficient. The low electrical resistance of metals make them quite useful for creating circuitry on the chip level to carry the current or electrical signal from one place to another. Over the generations, MOSFET efficiency has been improved following the Moore's law, leading to miniaturization of the device or device elements. This made the need of utilizing metals even more prominent for different applications such as heat sink, interconnects, new generation of ohmic contacts and superior diffusion barrier to withstand high temperature applications etc. [5,8-10].

The thickness of these deposited thin films can be in range from few tens of nanometers to micrometer. The thickness, deposition process, structuring, pre-processing cleaning etc. are predetermined by the intended application. The current chapter focuses on giving a short summary about application of various metals into MOSFET devices, their deposition or structuring techniques, applications and problems associated with them. Thereafter, a detailed information on the application of copper in power MOSFET devices and problems associated with copper as power metal are explained. Below, metals those are used frequently in MOSFET are categorized into three groups.

3.1 Ohmic / schottky contact metals

Every semiconductor material has a definite band gap. By varying the doping concentration, band gap can be tuned but still it exists. If metal is deposited on semiconductor material, electrons from conduction band of metal were passed into conduction band of semiconductor which creates a thermal equilibrium. This results into a certain potential barrier that is created between metal and semiconductor, which is called as a Schottky barrier or barrier height [9]. It is named after German scientist Walter Schottky. The

Schottky barrier height is defined as potential difference between work function of metal and electron affinity of semiconductor material [9]. The equation for the Schottky barrier height (φ_{bn0}) for n-type semiconductor is given in equation 3.

$$q\emptyset_{bn0} = q(\emptyset_m - \chi) \qquad (3)$$

Where, φ_m = metal work function and χ = electron affinity of semiconductor material

The value of Schottky barrier height depends on type or doping concentration of semiconductor material as well as type of metal used. When applied voltage across metal-semiconductor is more than the formed barrier height, current starts flowing in forward direction.

Apart from certain applications, such a barrier height between metal and semiconductor is not ideal as in MOSFET applications current should be transferred in and out of semiconductor without any major losses. In other words, ohmic contact between semiconductor-metal interface is desired. Ohmic contact is the one where current driven out of metal-semiconductor junction depicts a linear relationship with voltage applied across the junction. It means the resistance of this contact should be minimum possible to avoid the losses during operation [11,12]. Most of the cases, metal silicides are used for this purpose as they form stable interface. The choice of the metal depends on various factors such as, work function of metal, doping concentration of the semiconductor, silicide conductivity and stability etc. [9,11,12].Various metal silicides, which are used for ohmic contact with semiconductor materials, are silicides of titanium, cobalt, nickel, tungsten, tantalum, platinum, molybdenum and many more [9,11,12]. For semiconductor materials with large band gap, choice of metal become critical as one with low work function does not exist. Thus heavy implant dose is used at contact surface of semiconductor to get low ohmic contact with metal. Currently, metal silicide is formed by deposition of metal followed by anneal at appropriate temperature to get good ohmic contact [9].

3.2 Metal barriers

In previous chapters, it has been stated that the MOSFET devices under normal operating conditions have certain losses, which generate thermal energy in the device. Based on operating conditions, device temperature can shoot to a temperature as high as 400°C [4,7]. Under such a substantial thermal budget if metal is deposited on silicon directly, it ends up

reacting with silicon. If metal reacts with silicon, electrical properties of device elements such as gate, source or drain will be altered. This can lead to malfunctioning of the device, increasing leakage current or even causes short circuit between two areas [6]. In order to restrain the reaction of silicon substrate with the metal films, metal barriers are used. Metal barriers are thin layer of specially designed metals, metal nitrides, carbides or metal alloys which have high thermal stability for long duration of time and does not or react moderately with semiconductor substrates [5,6,8,10]. Various kinds of metals such as tungsten, molybdenum, tantalum or their nitride layers viz. titanium nitride, tungsten nitride, tantalum nitride, or alloys viz. TiW, Cu-Mn, Al-Cu, Ti-Cu or Cu-Rh etc. have been used as a metal barrier [5,8,10,13,14]. It is a matter of extreme importance that these metal barriers have low resistance, high thermal stability; show resistance to phase change or crystal change and forbid inter-diffusion of metal through its grains or grain boundaries.

The functionality of thin metal films as metal barrier is strongly depends on several factors [8,10,13-15]. The performance of diffusion barrier is nothing but its ability to resist the atomic migration between silicon and power metal such as Al or Cu. This is influenced by concentration differences, applied electrical field, thermal energy or strain in the system [8,15,16]. The inter-diffusion can take place through defects or vacancies in the barrier, or along the grain boundaries of barrier grains, due to metallurgical or chemical reactions of

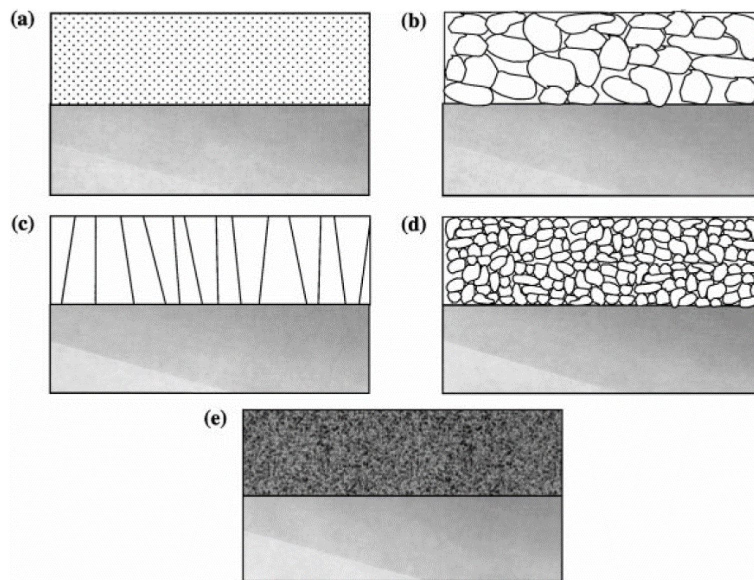

Figure 4. Schematics of various possible microstructures for the barrier (a) single crystalline (b) poly crystalline (c) bamboo like (d) nano-crystalline (e) amorphous. [16]

barrier with substrate or metal [14-16]. This leads to the conclusion that, microstructure of barrier has predominant role in its performance against the metal diffusion (In paper D it is discussed how morphology of the film is dependent on deposition process and thus its performance). Thus, it's quite logical that metals such as tungsten, tantalum, molybdenum etc. will be chosen for barrier application as their melting point is high which means the change in microstructure of the film or tendency to form intermetallic alloys at operating temperature of the MOSFET device will be marginal [5,8,15-16]. In addition to it, properties of thin films of these metals or their alloys or nitride layers can be tuned easily by tuning the process parameters [10,15,16]. This leads to easier tuning of the microstructure of the films and thus functionality of barrier can be enhanced (cf. Paper D). Kaloyeros et. al. stated that fine nano-crystalline or amorphous material with stable crystalline state is desirable candidate for barrier application compared to single, poly or bamboo shaped crystalline microstructure (see figure 4) [16]. Another important aspect of the barrier is its adhesive properties. It should have sufficient adhesion to the substrate as well as to power metal. Any kind of delamination or voids formation leads to the loss of effective contact area between the two layers having the interface under consideration, which means loss of electrical conductivity. This can be detrimental as loss of conductive path leads to failure of the device [8,15,16].

Here, a summary on various types of barriers is given below. Among others, metal nitrides, self-forming barriers and TiW are one of most commonly used metal barriers. Various studies elaborating their deposition techniques, properties and high temperature stability from application point of view are explained below in nut shell.

3.2.1 Metal nitride based barriers

In the field of MOSEFT devices, metal nitrides have gained immense importance as they put forth excellent performance in area of metal barrier applications. The nitrides of tungsten, titanium, tantalum etc. fulfill requirements of this field in many ways. These nitrides have low electrical resistance, high thermal stability, chemical inertness and offer good adhesion to silicon, silicon dioxide or metals such as copper [14,16-20]. These films are also quite stable under the electric field and phenomenon such as phase change or grain growth is seldom witnessed. Titanium nitride is used as a barrier for low temperature applications and restricted to aluminum, as copper readily reacts with titanium nitride [16,21]. On the other hand, tantalum nitride and tungsten nitride have wide spread application as a diffusion barrier in semiconductor world.

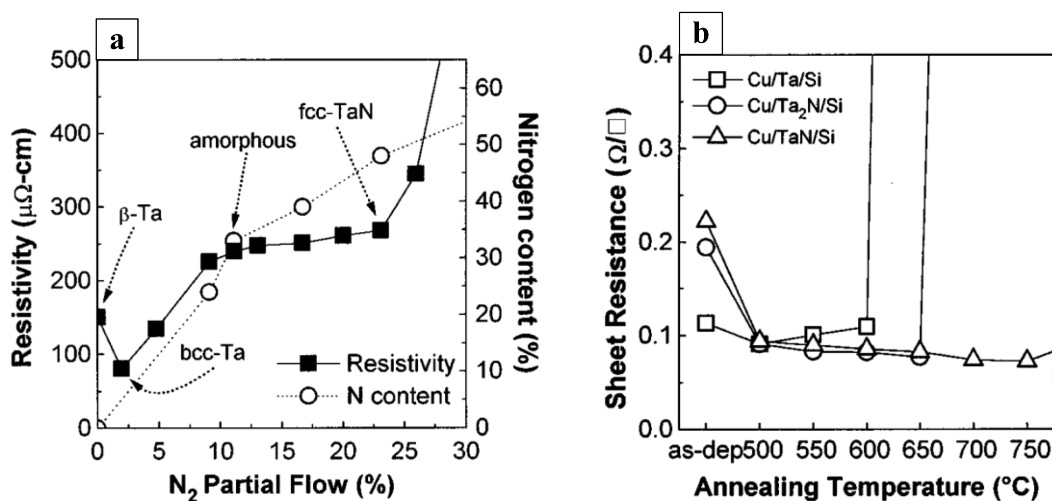

Figure 5. (a) A plot showing change in resistivity of tantalum and tantalum nitride barriers against change in nitrogen partial pressure (b) annealing experiment showing stability of various tantalum based barriers [23].

Tantalum is refractory metal having very high melting point (~3000°C) and it can be deposited using PVD process or its nitride by using a reactive (mixture of nitrogen and argon) plasma sputtering technique [16,18,22]. Alternative process for deposition of tantalum nitride is MOCVD technique, which is however seldom in use [16]. Tantalum nitride exhibits numerous different phases and tantalum or its nitride can be used as a diffusion barrier for copper [16,18]. The resistivity of tantalum nitride can be tuned by merely incorporating more nitrogen in the film [14,23,24]. The sheet resistance of tantalum nitride film can be tuned in the range of 150-1000 μΩ.cm depending on the extent of nitrogen gas added to the plasma. By incorporating more nitrogen in plasma, phase change was observed in deposited tantalum nitride films as shown in figure 5a. At beginning by small increase in flow of nitrogen, initially deposited tetragonal β-Ta film changes its crystal structure to bcc, which is α-Ta. The resistance of this newly deposited α-Ta is 15-30μΩ.cm, which is much lower compared to that of β-Ta which is around 150 μΩ.cm. With further increase in the nitrogen flow, tantalum nitride is deposited (fcc-Ta (N) film). Tantalum itself is good barrier up to a moderate temperature of ~ 450-500°C [14,25]. At higher temperature, it reacts with silicon forming tantalum silicide and diffusion of copper into the tantalum film is also been reported. On the other hand, Ta_2N is stable up to 600°C and at higher temperature, it tends to crystallize from its previously amorphous phase. Tantalum nitride deposited at higher nitrogen partial flow has TaN phase and it is known to be a stable copper barrier for temperature as high as 750°C [18,23,24]. A plot showing barrier stability as a

function of annealing temperature for three different barriers is as shown in figure 5b. Several studies have been carried out depicting same results while the degradation temperature for barrier film was varying and it was accounted to the fluctuation of nitrogen content in the reactive plasma. Nonetheless, nitrogen incorporation enhances the diffusion barrier properties of tantalum and tantalum nitride. The fcc-tantalum nitride film (TaN) is amorphous in nature and same is a most stable Ta-based diffusion barrier for copper on silicon at a temperature as high as 700°C [18,23,24].

Barrier	Unit Cell Type	Sheet resistance (μΩ.cm)	Method of deposition	Stable barrier up to [ref]
Ta	bcc	25	PVD	500°C [23]
Ta_2N	fcc	Varies sensitively with nitrogen content (150 to 1000)	PVD	600°C [23]
TaN	fcc		PVD	700°C [23,24]
W	bcc	50	MOCVD, PVD	600°C [17]
W_2N	fcc	200		800°C [17,27]
WN	fcc	600		600°C [17,27]

Table 1. Showing comparison of various tantalum and tungsten based barriers.

Similar to tantalum nitride, tungsten nitride exhibits numerous polytypes [14,26]. If nitrogen content in a phase is higher than that of tungsten, the sheet resistance of the same phase was found to be higher to stoichiometric tungsten nitride [17,27,28]. A detailed investigation on tungsten nitride as diffusion barrier revealed that, the W_2N is better barrier compared to WN [17,27]. At a temperature as high as 800°C, W_2N barrier prevents diffusion of copper into silicon [17,27]. Unlike to it, failure of WN barrier film happens much earlier at around 600°C. This is because W_2N is thermodynamically favorable phase while WN undergoes degradation showing loss of nitrogen content at elevated temperature [17,27]. Furthermore, W_2N film can be deposited in an amorphous phase and its recrystallization temperature is higher compared to that of WN and thus reduces chances of grain boundary diffusion of copper [17,29]. Irrespective of which phase, tungsten nitride can be deposited using Metal-CVD technique as well as PVD technique [16,17,27,29]. Metal CVD utilizes the tungsten hexafluoride precursor and deposition can be very conformal; even for high aspect ratio topographies [16]. Alternative methods would be to have metal organic (MO)

CVD technique. In PVD method, by using reactive plasma of argon and nitrogen gas, tungsten nitride is deposited. Uekubo et.al. have reported that, at lower nitrogen flow at around 20%, deposition of W_2N phase take place while at around 50% of nitrogen or above WN film is synthesized [17]. Table 1 gives a comparative summary for various metal barriers, their deposition methods, stable operating temperatures, sheet resistances etc.

3.2.2 Self-forming barrier

As name indicates, it is a kind of metal barrier that forms by itself upon a supply of first thermal budget. Typically, an alloy of copper and particular elements such as aluminum, magnesium, manganese or titanium etc. was used for this purpose and deposited instead of barrier layer on the dielectric film [13, 30-34]. The choice of solute element is based on its large negative heat of oxide formation as well as on its limited solubility in power metal such as copper [13]. After the deposition of thick Cu metal, the complete stack will be annealed to certain elevated temperature. Under the influence of thermal budget, solute element diffuses out of the thin film towards the interface to silicon dioxide [30-32]. The metal thus forms oxide layer between dielectric and metal, preventing diffusion of it into silicon dioxide and thus acts as a barrier. A schematic of three process steps; namely deposition of barrier, Cu deposition and annealing are as shown in figure 6 a-c respectively. Murarka et. al. introduced this concept of forming a self-forming barrier [5,15]. The segregation of solute atoms at the interface of silicon dioxide or silicon leads to insulation of Cu metal from these layers. If the low solubility atom has high tendency to form oxide, it creates oxide layer. In case of low probability of oxide formation, a thin amorphous layer of metal diffused out of the thin film, is sufficient enough to form a barrier. The deposited layer of such an alloy is purposefully kept thin enough that out diffusion can take place quite fast and at relatively lower annealing temperature. The newly formed layer also enhances

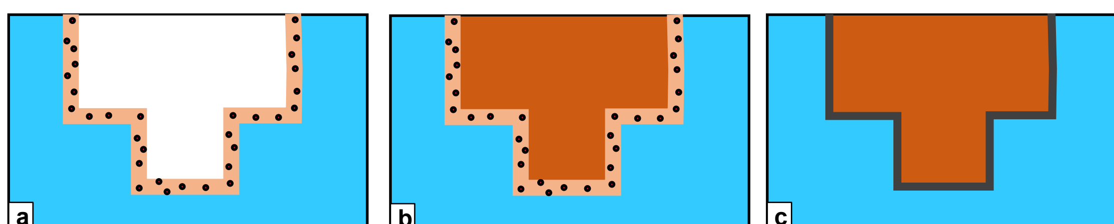

Figure 6. Schematic representation of self-forming barrier process. (a) Deposition of alloy for self-forming barrier (b) deposition of copper (c) subsequent annealing to out diffuse solute atoms to form a barrier.

the adhesion of metal to substrate as well as increases the electro-migration resistance [13,34,35]. The out diffusion is mainly dependent on the solute concentration and supplied thermal budget.

There are certain considerations in using solute element for self-forming barrier. The solute atom should not increase the resistivity of copper film drastically or at least it should be reduced after annealing at suitable temperature [13,15]. By annealing, certain amount of solute element can diffuse into the power metal as well, reducing the net resistance of deposited barrier film. On the other hand, rate of diffusion of solute in the Cu metal should be sufficiently high. This offers a faster diffusivity of solute atom out of the system and better probability of forming good barrier at lower annealing temperature.

3.2.3 TiW barrier

A metastable phase of titanium-tungsten metals (TiW) has proven to be excellent metal diffusion barrier in the interconnect world [14,36-38]. A thin film of TiW barrier is deposited by sputtering process from a target made up of titanium and tungsten. Titanium is often around 10% by wt. and rest 90% is tungsten. The phase diagram of titanium and tungsten system is as shown in figure 7. It is clear, at room temperature there is no stable phase that exists between two metals [14,39]. Interestingly, as atomic radius of these two elements is almost the same, it results in a substitutional solid solution of two atoms. Titanium takes a substitutional position in the crystal structure of tungsten [40]. The presence of titanium increases the adhesion of TiW film on the underlying substrate or oxide layer drastically [36,41]. The barrier properties of TiW film can be tuned drastically by changing deposition conditions. In paper D by tuning deposition parameters two different TiW films have been deposited and studied for their microstructural properties. Furthermore, by using cross-sectional X-ray nanodiffraction, the residual stress gradient in the films was mapped. It is seen that metallurgical dense grain boundaries result in compressive stress in the film while porous grain boundaries offer tensile film stress. There are numerous studies stating mechanism for the performance of TiW as a diffusion barrier. Oparowski et. al. stated that the diffusion properties of TiW film can be improved drastically by sputtering the film under reactive sputtering conditions [38]. By incorporation of nitrogen or oxygen during sputtering process, barrier performance was improved and the same is correlated to the loss of β-W phase and growth of nitride or oxide of titanium and tungsten phases. Different studies concluded that the presence of oxygen or nitrogen atoms between TiW and Al layer due to vacuum break enhances life time of the barrier [37,38]. The

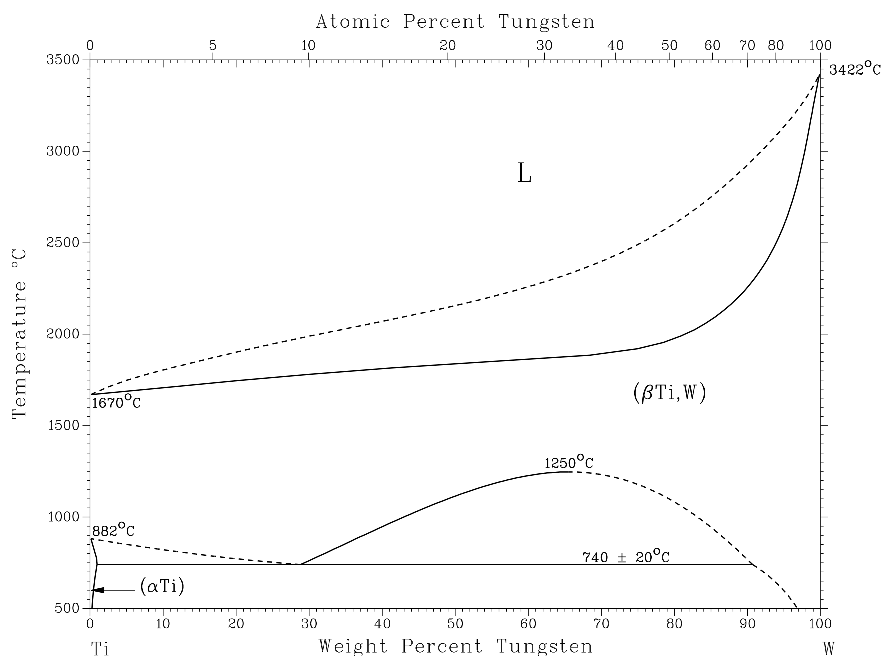

Figure 7. Phase diagram of titanium and tungsten metals [45].

application of D.C. Bias voltage during sputtering alters titanium content of the deposited film [42,43]. The titanium content of the film shows linear dependency to the applied D.C. bias and same decreases with increasing the D.C bias. The author stated that, the decrease in titanium content of the film might be detrimental to the adhesive properties of TiW film [43]. However, in a recent study, Voelker et. al. demonstrated that, the presence of titanium in TiW film, rather than its amount, is responsible for the good adhesive properties [44]. In this study, using four point bending method, interface release energy of barrier and silicon oxide was calculated. The interface energy of TiW film was higher than pure tungsten film and is in same range of pure titanium film. Bergstrom studied two different stoichiometries of TiW films as a diffusion barrier for aluminum metallization and calculated the activation energy for the formation of WAl_4 intermetallic layer for both TiW films [46]. The failure of the barrier is mainly designated to the W-Al intermetallic formation while titanium was found to be diffused into the Al layer. It proved that films having lower titanium content perform better as a metal barrier. Another study reported same mode of failure of TiW barrier where upon annealing titanium diffuses into aluminum layer eventually leading to malfunction of barrier [47]. The activation energy of 2.28eV was also calculated for such out-diffusion of titanium into AlCu metal system. However, as stated before, the microstructure (grain size, grain boundaries etc.) of the barrier has vital role to play in its

performance [15,16]. Presence of titanium influences adhesive properties of TiW barrier but not proven to have any influence on its diffusion properties [44-46]. Thus, it is matter of extreme importance to investigate the microstructure of TiW film for its excellent barrier properties. The current work will address this issue. (cf. Paper D)

4. Interconnect metal

4.1 Choice of interconnect metal : Copper

The candidature of metal for this category is based on two important properties, its electrical and thermal conductivity. Since the evolution of semiconductor era around 1960 and onwards, aluminum or aluminum based alloys (such as AlSiCu) fulfilled the requirements of IC metallization [8,10]. The major advantage of aluminum is that, it does not react with silicon dioxide or dielectric material and by incorporating proper amount of silicon into its alloy, it can be made inert against silicon itself. However, in order to boost performance of MOSFET devices and avail high speed applications, device miniaturization has taken place which leads to increase in power densities [8,15]. Thus, recent trend is to replace aluminum or aluminum based metallization with a metal that has lower resistivity. Therefore, choice of metal is then shrunk down to copper, silver and gold. The table 2 listed below gives a comparison of these four metals [5]. The choice is obvious to use copper to replace aluminum in silicon based IC devices. Copper offers various advantages over aluminum

Property	Metal				
	Cu	Ag	Au	Al	W
Resistivity ($\mu\Omega$ cm)	1.67	1.59	2.35	2.66	5.65
Young's modulus ($\times 10^{-11}$ dyn cm^{-2})	12.98	8.27	7.85	7.06	41.1
TCR$\times 10^3$ (K^{-1})	4.3	4.1	4	4.3	4.8
Thermal conductivity (W cm^{-1})	3.98	4.25	3.15	2.38	1.74
CTE$\times 10^6$ (°C^{-1})	17	19.1	14.2	23.5	4.5
M.p. (°C)	1085	962	1064	660	3387
Specific heat capacity (J kg^{-1} K^{-1})	386	234	132	917	138
Corrosion in air	Poor	Poor	Excellent	Good	Good
Adhesion to SiO_2	Poor	Poor	Poor	Good	Poor
Deposition					
Sputtering	✓	✓	✓	✓	✓
Evaporation	✓	✓	✓	✓	✓
CVD	✓	?	?	✓(?)	✓
Etching					
Dry	?	?	?	✓	✓
Wet	✓	✓	✓	✓	✓
Delay (ps mm^{-1}) [a]	2.3	2.2	3.2	3.7	7.8
Thermal stress per degree for films on Si ($\times 10^7$ dyn cm^{-2} °C^{-1})	2.5	1.9	1.2	2.1	0.8
Self-diffusion					
Q (eV)	2.19	1.97	1.81	1.48	5.47
D_o (cm^2 s^{-1})	0.78	0.67	0.091	1.71	0.04
Free-energy (ΔG) of formation oxide	CuO	Ag_2O	Au	Al_2O_3	WO_3
ΔG (298 °C) (kcal per oxygen atom)	30.7	~16	– [b]	126	60.8
Mean free path of electrons (Å)	390	520	380	150	50 (+6) [c] 81 (+3)

Table 2. A table summarizing various properties of commonly used metals in semiconductor applications [5].

metal [5,8,10,15]. First and foremost importance is electrical conductivity. As seen in the table 2, the resistivity of copper is much lower compared to that of aluminum. The study revealed that for a film thickness higher than 100nm, copper has almost 35% lower bulk resistivity compared to aluminum [8]. It means copper interconnect that has same length, width and thickness as that of aluminum interconnect, shows 35% smaller resistivity. At the same time, its thermal conductivity is high but its coefficient of thermal expansion is low [5,8]. Thus, copper not only can conduct the electricity with lower losses, but also can absorbs more heat compared to aluminum and it induces lesser mechanical stress on the system due to its thermal expansion.

Another advantage of copper based metal system is that, it is more resistant to electro migration compared to aluminum based metallization because of its high melting point [10,48]. Higher current densities across smaller line widths create sufficient momentum in electrons, which is then transferred to atoms. As copper melts at much higher temperature compared to aluminum, it tends to sustain such a momentum applied by electrons making it robust against electro-migration effect. Furthermore, the mechanical strength of copper is much higher than that of aluminum. It means for a given force, copper metal undergoes less deformation in comparison to aluminum [10,15]. This results in much lower interfacial stress between copper and its surrounding material such as dielectric. This decreases the risk of delamination between two materials.

The other two metals namely, silver and gold have certain disadvantages over copper metal and thus are not a proper choice to replace aluminum in metallization. Although silver has marginally better electrical conductivity than copper, corrosion resistance of silver is much poor compared to copper [5,49]. Furthermore, it reacts with silicon dioxide much faster and performs worse in electro-migration. On the other hand, gold offers only a better corrosion resistance than copper, while two important factors; its electrical and thermal conductivity is lesser [5]. Therefore, it doesn't offer a great advantage over the copper. In addition to it, after considering cost effectiveness of copper over gold or silver, copper comes out to be a suitable choice in this case.

There are also few disadvantages that copper possess over aluminum. Copper unlike to aluminum fails to protect itself by creating a protective oxide layer over its surface [5,8]. Aluminum forms dense aluminum oxide layer, which protects rest of the metal from corrosion. Copper oxide on the other hand, has two types of oxide CuO and Cu_2O, which are readily formed above 100°C [5]. However, both of them are not dense enough against further oxidation of metal into the depth [48]. Thus, copper metal needs a good protective

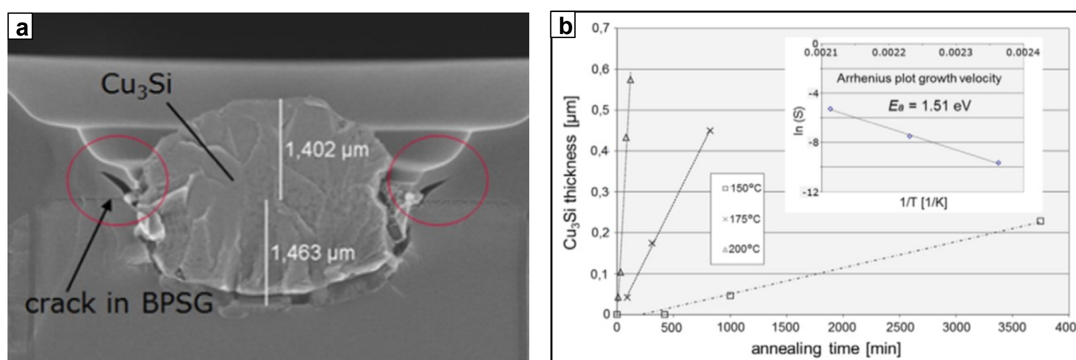

Figure 8. (a) SEM micrograph showing copper silicide formed. Copper was deposited without any barrier and (b) plot showing rate of copper silicide formation for different temperature and time. [6]

layer to cover its surface from oxidation. Moreover, copper reacts and diffuses into silicon dioxide layer mainly in form of Cu^{+} ions [15,49]. The ionization of copper mainly takes place in presence of humidity or impurity atoms. The rate of diffusion is mainly depend on type and quality of this oxide, applied bias value as well as the temperature of operation. The presence of Cu^{+} ions increases leakage current and it results into malfunctioning of the device and thus not acceptable.

On a similar path, direct contact of copper with silicon is contra productive for two major reasons. First, copper is expected to have three acceptor levels in a band gap of silicon [15]. If copper occupies those three levels, it can generate the leakage current in reverse bias condition [5,15]. Second reason is that, copper reacts with silicon, i.e. semiconductor material at relatively lower temperature [6,8,15]. The reaction product is copper silicide (Cu_3Si) (see figure 8a). At given temperature, copper has very high solubility in silicon and is considered to be fastest diffusing transition metal in silicon [15]. The solubility is not only affected by the temperature but also influenced by type and doping concentration of semiconductor material. Hille et. al. have shown that copper silicide formation can start at temperature as low as 150°C at moderate annealing time (see figure 8b) [6]. The growth of copper silicide was accompanied by volume expansion. In range of 150-200°C, initial growth of copper silicide showed a linear behavior while it shifted to parabolic behavior after a growth to a thickness of 600nm. The activation energy calculated for the same was 1.5 eV. For a temperature above 200°C, growth of copper silicide tends to follow a parabolic law. Various reports have shown that the calculated activation energy for silicide growth may vary from 0.95 eV to 1.34 eV [50,51]. Ward et al. have explained that, activation energy

depends on the type of diffusion of copper namely; grain boundary diffusion or bulk diffusion. At lower temperature grain boundary diffusion is faster than bulk diffusion, thus it decreases the activation energy. Nevertheless, in every case, there is strong volume expansion during silicide formation and silicon is consumed at steep rate. Thus, it is matter of extreme importance to protect silicon from copper diffusion and usage of proper barrier is mandatory. In conclusion, copper needs to be separated from silicon dioxide as well as from silicon itself by using a properly chosen diffusion barrier [6,52]. Various barriers for this purpose are listed above with proper description.

Another drawback of copper metallization is the lack of its adhesion to any kind of dielectric layer. Copper does not reduce dielectric namely silicon dioxide as aluminum does, thus adhesion between dielectric and copper is poor [52]. Therefore, a proper adhesion promoter is needed. Above mentioned diffusion barriers can serve dual function of a barrier as well as adhesion promoter [10,15,52]. Lastly, unlike to aluminum which can be etched with wet or dry techniques, copper structuring is not possible by dry etching and can be structured either wet chemically or by using techniques such as damascene [8,10,48]. The microstructure of copper is strongly influenced by deposition processes and thereby, its material properties. Below, a summery on various aspects of deposition techniques is given to get a better overview on properties of copper. In paper B, a special deposition process led to nano-crystalline grain growth in copper film. Upon annealing, grains have grown to micron size. The fracture load of the same film before and after annealing was significantly reduced.

4.2 Deposition techniques for copper metal

Copper offers numerous benefits compared to other metals in various manners, one among those is its ease of deposition. The thickness of copper film can be easily tuned from few microns till few tens of microns by means of adopting proper deposition process [8]. This gives copper additional plus point to be a superior choice compared to other metals such as aluminum whose thickness is hard to tune without increase in cost and process complications. In this chapter, various deposition processes for copper metallization are illustrated.

4.2.1 Physical vapor deposition (PVD)

PVD or sputtering is one of the simple techniques for deposition of metal films. In this process, highly energized particles knock out atoms from the target material and same being

deposited on the substrate (see figure 9 left). Highly energized particles are basically ionized atoms of noble gases such as helium or argon which are accelerated through the plasma against the cathode electrode [8,53]. The cathode electrode is nothing but a target metal while anode is substrate on which deposition takes place. The deposition is carried out at relatively low pressure and offers a good control over uniformity, composition and microstructure of deposited film and it is an efficient and reliable process. In this process, kinetic energy of ion is transferred to target atoms and by that, material or metals of very high melting point such as tungsten or tantalum, can also be sputter deposited using this process.

As deposition process is considerably low angle deposition (from top to down), the conformity of the deposition process is not quite good [53]. As shown in figure 9 right, during deposition the top edge of contact hole or via is adequately deposited while at a same

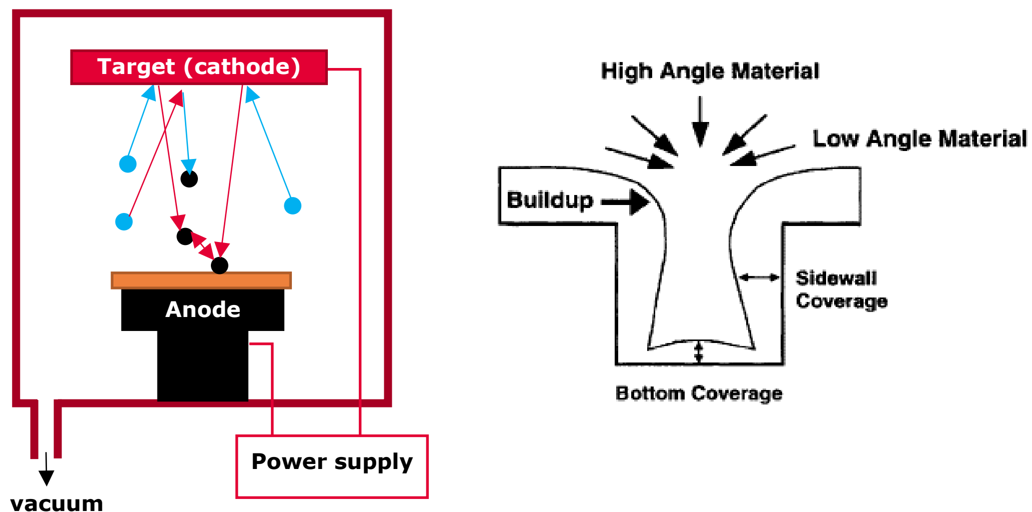

Figure 9. Schematic representation of (left) DC sputtering process. Blue circles represent sputtering gas while black circles stand for target atoms. (right) Non-conformal filling behavior of sputtering process in a contact hole or trench [53].

time, due to shadowing effect, deposition on the sidewall or at bottom of via is less. The ratio of thickness of film deposited on sidewall to that of one deposited at bottom of via is called step coverage. In order to maximize such step coverage, sputtering process is assisted with additional bias power. By application of RF bias, plasma density increases as electrons are trapped in the plasma due to rapid change of additional potential [8,53]. This creates additional acceleration of ions and transports them to the substrate bottom or sidewall. Furthermore, magnetic field is applied to confine secondary electron to ease them reaching

the target. This can increase the deposition rate and offer ease of tuning the deposition uniformity.

Various gases can be used for the sputtering application. Commonly argon gas is used as sputtering gas but gases such as neon, xenon, and krypton can also be used [53]. Figure 10 shows a plot on impact of changing sputter gas on sputter yield for varying ion energy. At low sputter energy, mass of knocking particle has no significant effect and only at relatively very high energy regime, it carries an influence. Furthermore, sputtering is nothing but a transfer of momentum or energy of particle and it happens most efficiently, if mass of two particles is approximately same. There are few other factors such as, incident angle of knocking particle, target to substrate distance, operating pressure etc. which have certain influence on the sputtering yield of the system [8,53]. In addition to it, the energy of the system has definite impact on the morphology of the deposited film [54,55]. Thornton has put forth a model explaining the correlation between these sputter parameters and morphology of crystal growth in a deposited film [54]. Thornton divided model into three different regimes based on sputtering process pressure and ratio of substrate temperature (T) to the melting temperature of target metal (Tm) i.e. T/Tm. In paper D, based on this model, different morphological aspects of TiW films were discussed and correlation to Thornton's growth model has been shown.

At low deposition temperature (T/Tm < 0.3), zone I exists and it has columnar grains consisting of tapered units. The grains have voids along the grain boundaries. Zone II (0.3 < T/Tm < 0.5) consists of columnar grains but have metallurgical grain boundaries which

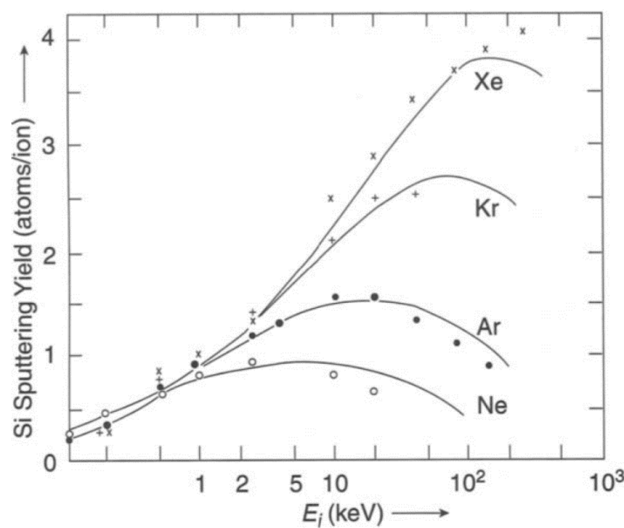

Figure 10. A plot showing sputtering yield (for Si) for varying ion energies and different noble gases. [53]

are densely packed. In this zone, due to higher temperature, energy of system is higher, enabling high rate of surface diffusion. This leads to better grain growth and film development. The high temperature zone III ($T/Tm > 0.5$) structure have equiaxed grains with large grain size. In this zone, activation energy is sufficient for a bulk diffusion process. There is also a zone called “zone T”, which is a transition zone between zone I and II. The grains of this zone have less porosity compared to zone I and surface roughness is lesser compared to the two adjacent zones (as seen in the figure 11a).

Based on this theory, Craig and Harding have carried out an extensive study of sputter depositing copper thin films covering experimental conditions for all four zones [55]. In that experiment, the substrate temperature was varied between 20-450 °C while sputter gas pressure was meddled between 0.5-100 Pa. The deposited films were then classified as per their microstructure and surface topography. The grain growth or surface morphology show clear correlation to the deposition conditions giving experimental evidence of Thornton model. Based on collected data, a structural zone model for substrate temperature and sputter pressure was created by them. The same is displayed in the figure 11b. The model is a basic platform to understand the morphology of sputter deposited copper film and use the same as per need to fine tune the morphological properties of deposited film.

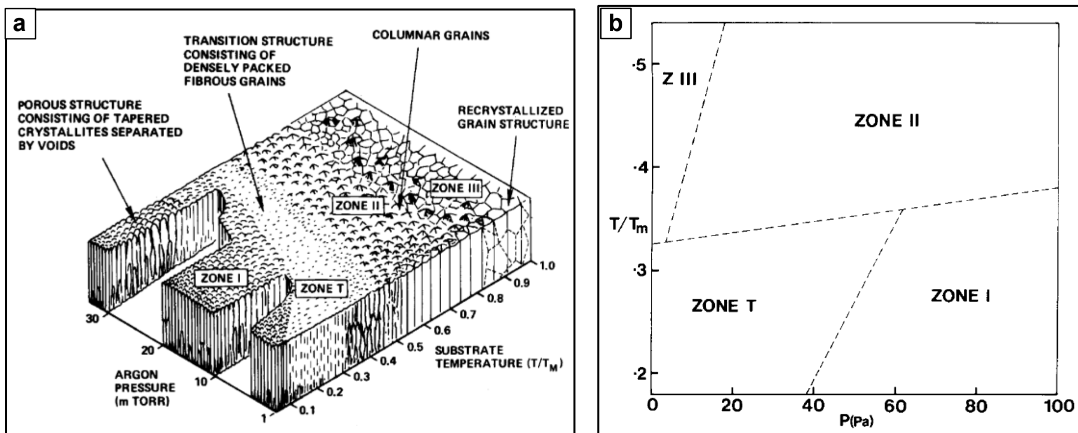

Figure 11. (a) Microstructural zone diagram for metal film deposited by sputtering process representing Thornton’s model [54]. (b) Based on same, a diagram summarizing dependence of morphological features of sputter deposited copper film on temperature of deposition and process pressure [55].

4.2.2 Plating of thin copper films

Plating is a process where thin metal film is deposited from a chemical bath. It is classified into two major categories; electro-plating and electro-less plating [8]. Electro-plating

process utilizes applied electric current between two electrodes for deposition of metal film. Thus, it is also called as electro-chemical deposition (ECD) technique. In second method of electro less plating, no electric field is necessary for the deposition of metal thin film. Using both methods, copper films can be deposited efficiently on substrate or in trenches or vias [48,52]. Copper cannot be structured easily compared to other traditional metals such as aluminum or tungsten, thus modern semiconductor fabrication processes has moved from traditional “deposition + structuring concept” to a dual damascene technique for copper metallization [8,48,52].

Damascene is a technique originally got its name from Damascus city, famous for its steel. This technique is used basically to deposit copper in trenches or contact vias, structured in dielectric layer. It is called single damascene if trench or contact hole is fabricated and filled with copper one at a time. On the other hand, if both are fabricated one behind another and then filled with copper by single metallization step, the process is named as dual damascene. It is thus relatively cost effective as one metallization step is eliminated and thus with fewer process steps it is preferred over single damascene [8]. A schematic depicted in figure 12 shows the difference between two processes.

After trench or via is etched in the oxide, copper is filled with plating method. In order to do that, first a thin seed layer is deposited. Seed layer consists of metal barrier and copper thin film deposited often using PVD technique [8,10,56]. The barrier layer in most of the cases is TaN/Ta layer while copper film is 150-300nm thick. On this film, copper layer is grown by plating method in a chemical bath. For electro plating, chemical bath consists of cupric solution of copper sulfate and sulfuric acid [8,56]. Copper is deposited at cathode electrode by consuming copper ions from bath and amount deposited is directly proportional to the magnitude and duration of current flow. In order to achieve deposition of void free copper in trench or via geometries better flow of chemical and concentration control over the wafer is required. For this purpose, a dedicated flow system using pumps or rotating electrodes is used. In addition, various additives are added to the chemical bath to further control the current flow locally, reduce or enhance and ensure uniform deposition of copper [8]. The copper film deposited on seed layer is very fine crystalline in nature. The as deposited film consists of various impurities which were eventually driven out of the film by a proper annealing step afterwards [8,48]. In addition, resistance of the deposited film is higher than the bulk copper value due to various crystal dislocation, impurity atoms, too many grain boundaries etc. The film undergoes change in resistivity, grain size, microstructural changes during this annealing step [8,10,48,52]. Self-annealing

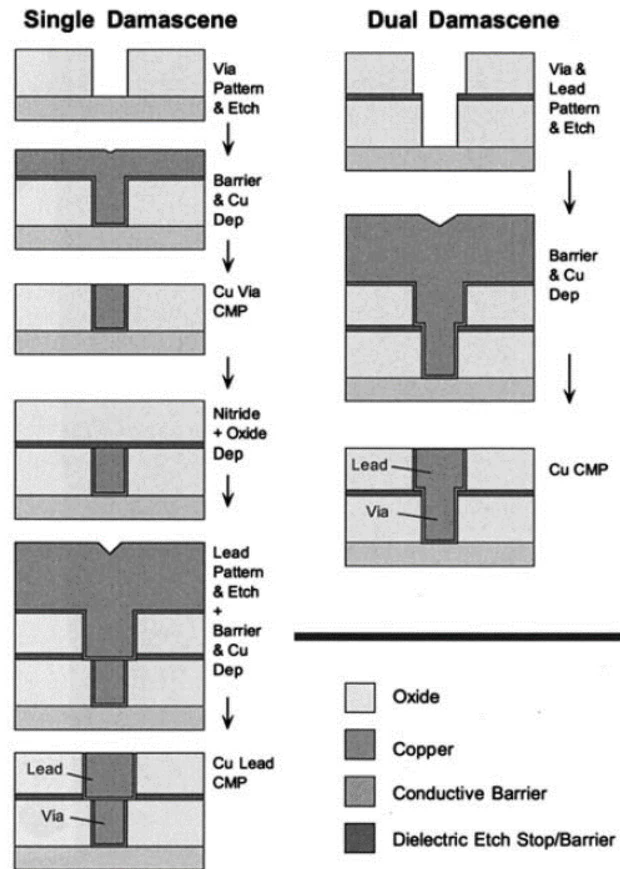

Figure 12. A schematic representing single and dual damascene processes. [8]

crystallization at room temperature reduces the grain growth and resistance of the film [8]. The film has often (111) texture inherited from seed layer and trench geometry has twofold influence; first (111) fiber texture decreases with line width and second short distance lines has bamboo-like structure with grain boundaries perpendicular to trench edges [8,10]. The (111) texture minimize the presence of high angle grain boundaries making material robust against the electro-migration [10,48].

The trench filling follow three kinds of filling form in plating process; conformal filling, sub-conformal filling and super-conformal filling (see figure 13) [8,10]. The sub-conformal filling process leads to creation of voids while in case of conformal filling there is a risk of seam line generation in a filled copper film. The super conformal filling is the most optimal method and this can be achieved by using proper inhibitor in the bath. Adding inhibitors suppresses the copper deposition on top of the trench and enables filling of trench from bottom side and thus a preferred option among three.

Copper thin film can also be deposited using an electro-less plating method [5,8]. In this method, the metal salt is reduced in presence of reducing agent and is deposited on the materials, which are conductive or non-conductive in nature. Once the process starts, it continues, and generally over-potential is large enough to avoid reaction in opposite direction. The bath generally consists of copper sulfate, potassium-sodium tartarate, sodium hydroxide and formaldehyde [8]. The bath size is generally small and not thermodynamically not very stable. Recent advances in electro-plating of copper have limited the application fields for e-less plating.

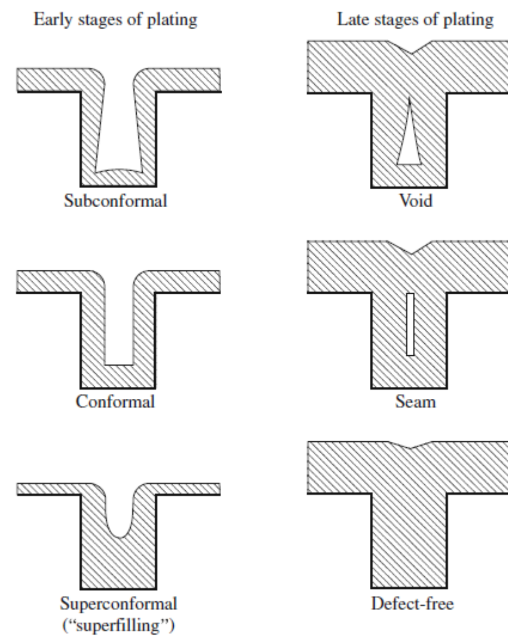

Figure 13. Shows types of filling profiles generated during electroplating of copper [8].

4.3 Properties of Copper

4.3.1 Film growth and crystal orientation

In microelectronics industry, copper thin films are deposited by various deposition techniques and every technique leaves behind its footprint on the microstructure and thus on material properties of deposited Cu film [8,10,48-52]. It is thus essential to understand material properties of copper that one can investigate behavior of copper thin film for its mechanical and thermo-mechanical applications in integrated circuits (cf. Paper A and D). In most of the applications, thin film is grown either by PVD technique or grown electrochemically over a seed layer which is deposited again by sputtering technique [8]. The sputter deposited films tend to grow in direction of (111) giving a preferred orientation to crystal structure of copper film [5,10,55]. This is because, activation energy for the surface diffusion is lesser compared to bulk diffusion energy during sputtering. This makes ad-atoms to adopt the crystal structure of minimum surface energy, which is (111) orientation. The same phenomenon is valid during electro-chemical deposition of the copper, giving a thin film with (111) as major orientation. Thereafter, it is most common to anneal the deposited film to gain a uniform microstructure across the film (see figure 14a)

[55,56]. There are numerous other parameters, which contribute to grain size of the deposited film. The copper which is investigated in following publications is nano crystalline copper which is deposited by low energy process (cf. Paper A, B, C). The grain size of copper is strongly under influence of wafer topography, pre-deposition cleaning processes, deposition atmosphere, impurity atoms etc. [8,10,55,56]. Rosenberg et. al. have elaborated the effect of substrate orientation on the forthcoming copper film [10]. Two seed layers of different grain orientations were deposited and ECD copper was grown on these films. The ECD films have opted to retain the same orientation as that of seed layer on which film was grown. Figure 14b & 15c show respectively, fiber texture plot of two different seed layers and ECD film grown on it showing unique same orientation.

Copper depicts another interesting phenomenon of self-annealing at room temperature [8,10,48,56]. After deposition of copper mainly by ECD, its grain size is very fine and defective. The grains re-crystallize showing noticeable grain growth without any supply of thermal budget. Lingk et al, have recorded the re-crystallization of copper for 24 hours after the deposition (see figure 15) [56]. Various FIB images show clear grain growth of ECD copper. It is also reported that CMP of Cu film before its re-crystallization, reduces the crystallization tendency of remain copper filled in a trench. The process is basically driven by residual stress in the system. Same phenomenon of stress relaxation can also be witnessed in sputter deposited films. The stress in the film changes, if the film relaxes over 24 hours [57]. In present study, copper film was grown in nano-crystalline size but no such a self-annealing effect was observed. However, upon supply of mechanical stress, Cu grains have grown their grain size showing similar effect. This self-annealing induces 25-30%

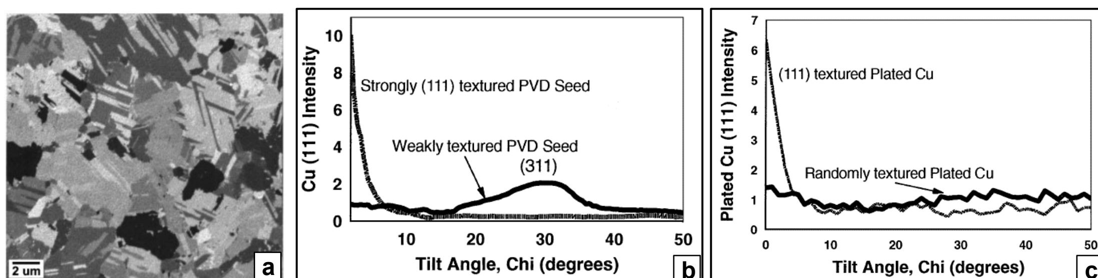

Figure 14. (a) SEM micrograph revealing microstructure of electro-plated copper, (b & c) are texture plots of copper seed layer and electro plated copper respectively. Plots show electroplated copper inherits its orientation from Cu seed layer [10].

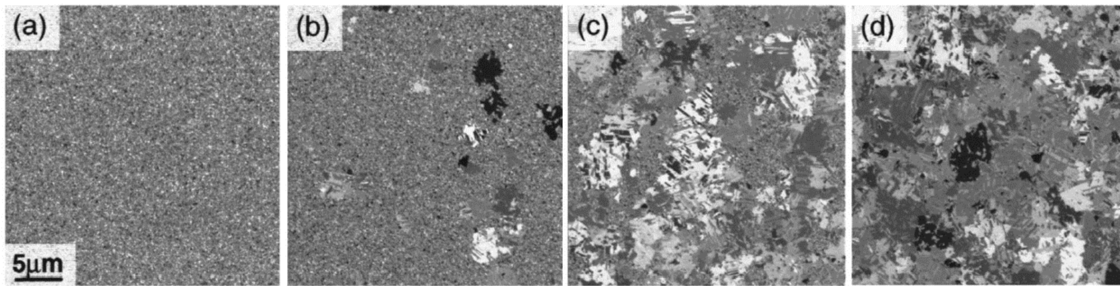

Figure 15. SEM micrographs showing self-recrystallization of copper at room temperature after cooled down to -78°C (a) after warming to room temperature (b) t = 5 hrs (c) t = 13 hrs and (d) t = 25 hrs. [56]

reduction in resistivity, change in stress of the film and strong growth in (111) orientation of the film [8]. Nevertheless, in order to get homogenous grain distribution in the film, post-processing annealing is recommended.

The grain size, spread of grain size and grain orientation have major influence on the material properties of thin copper films. This decides the stress of the film, electro migration resistance and its thermo-mechanical behavior. [5,10]. The grain orientation has major influence on stress of the film, as elastic modulus of copper vary with varying orientation. (111) orientation has 2.9 times higher elastic modulus than (100) direction [58]. As often, copper films tend to grow along (111) orientation due to sputtering process, relatively higher stress is imposed on the substrate by the copper film. The high temperature anneal assists to reduce total stress induced on substrate by increasing the grain size and developing a uniform microstructure over the film thickness [10,55,56] (In paper A, initial stress of copper film was reduced after first heating cycle and second cycles onwards no change in stress was observed). In addition to all these factors, the effect of reduced dimensions or simply geometrical constraints carry certain impact on microstructure of the copper thin film [10,56].

4.3.2 Electro migration of copper

The electro migration depends mainly on the type of metal but also influenced by its microstructure, various operating conditions such as current density, temperature etc. Copper outperforms aluminum in electro migration because of having superior intrinsic properties such as high melting point and ability to handle higher current density, [8,10]. The experimental study has revealed that, in electro migration, copper is more than 100 times more robust compared to aluminum metallization (see figure 16). The electro migration in copper is mainly a surface diffusion process unlike to Al metallization where

grain boundary diffusion is predominant [48]. As surface diffusion is key reason for electro migration, it is very important to have good adhesion between copper interconnect and barrier to avoid the surface diffusion. In addition to it, in dual damascene process, CMP process is used for planarization of copper surface after deposition, which leads to low adhesion of copper with upcoming dielectric film. This enhances electro migration of copper by offering path for atomic migration [48]. Furthermore, similar to copper in aluminum metallization, adding solute atoms in copper increases its resistance to the electro migration. For this purpose, metal tin is found to increase the electro migration resistance of copper drastically. However, increase in resistivity of copper is a side effect, making ad-atoms

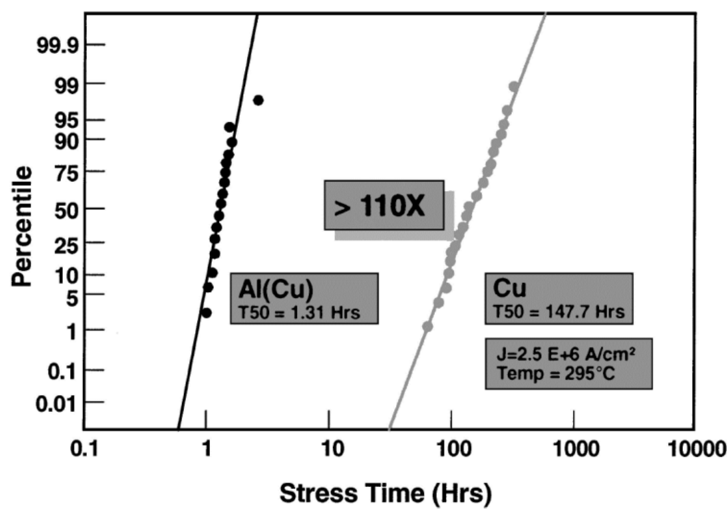

Figure 16. A plot showing electro migration lifetime of copper and aluminum (AlCu) metallization for 0.3 μm line. Copper lines have stronger resistance to electro migration [10].

uninteresting for increase in the electro migration resistance [48]. Line width of copper interconnect is also an important factor to be taken into consideration. For same current density, it is found that, decrease in line width has decreased the lifetime of copper in electro migration [10].

4.3.3 Thermo-mechanical behavior

The microstructure of copper film has a determining role to play in behavior of the film under temperature variations. Copper has higher modulus of elasticity as well as higher tensile strength compared to aluminum [8,10,15]. It means, for given strain the force induced by copper on silicon is much higher than that of aluminum metal. Although, the coefficient of thermal expansion of copper is lower than that of aluminum, due to its higher

stress, the net force induced by copper during thermal cycling is much higher [8,15]. Toomey et. al. have experimentally recorded thermo-mechanical stress behavior of copper [59]. The plot is reproduced in figure 17. As one can see, upon heating, the intrinsic stress of copper film decreases linearly with increase in temperature and it changes from tensile to compressive at around 200°C. With further increase in temperature, no recognizable change in film stress is observed till 400°C. Upon cooling, the film regains its original stress value. The plot is called hysteresis curve and many have reported same behavior for different types of copper films and thicknesses. The initial behavior where copper shows loss of film stress is called elastic part, while later part is called plastic deformation of copper film (cf. Paper A). The shape of hysteresis plot is controlled by various parameters such as initial microstructure of the copper, annealing temperature, type of passivation of copper film,

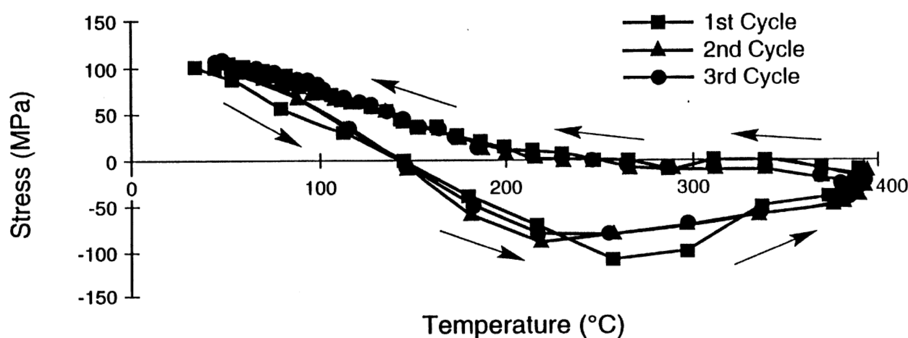

Figure 17. A plot showing film stress of 600 nm thick copper as a function of temperature for three heating cycles [59].

annealing atmosphere and impurity in copper film etc. [8,60-61]. The curve tends to follow same nature if experiment is repeated numerous times. However, with every cycle, energy supplied to the copper film is utilized to initiate deformation in copper film and eventually after certain number of cycles, copper ends up showing cracks, delamination, and slip lines generation [61]. This kind of cyclic load subject copper to fatigue loading resulting into failure of copper film. Bigl et al. have studies various copper thickness in range of 5 to 20µm deposited using sputtering or electro-chemical deposition technique [61]. After 1000 thermal cycles, irrespective of thickness of the film, crack formation or slip line formation together with increased surface roughness was recorded. In paper C, thin copper film was studied for its fatigue behavior using plus shaped MEMs structure and together with type of deformation stated above, it was observed that thickness has strong influence on endurance of the film under cyclic load.

In summary, mechanical stress induced by copper on the substrate at elevated temperature acts against adhesive force between copper film and silicon substrate. With every thermal cycle, the interface is repeatedly subjected to high stress and thus it is matter of immense importance to form a reliable interface between copper film and the substrate. Here, surface cleaning techniques play a vital role.

5. Micro electro mechanical systems (MEMS)

5.1 Introduction to MEMS

The invention and development of MOSFET and integrated circuit (IC) technology in mid-twentieth century has revolutionized the computer industry. Following the Moore's law, there was a trend to increase total number of transistors on a chip to boost the performance of chip. This helped microelectronics world in two ways; there was continuous improvement in techniques for silicon processing to facilitate the miniaturization of MOSFET devices and also various sensors as well as actuators have been incorporated in the system [62-65]. The both factors have offered a favorable platform for the development of micro-electro-mechanical systems (MEMS). MEMS is nothing but a system consisting of at least one sensor, actuator and processing unit inbuilt in it (see figure 18) [62]. The sensing unit read the input signal and feed the data to the processing unit. Based on this data, the processing unit commands the actuator unit to deliver an output signal. Essentially all these three systems can be fabricated from a single crystal silicon. In order to do so, the well-developed process blocks for the fabrication of MOSFETs and ICs such as deposition, etching, lithography etc. can be readily used for micromachining MEMS parts out of silicon [62,64,65]. These MEMS devices have miniaturized in sizes and thus can be mass produced identical to ICs [62]. Their small sizes also offer great range of sensitivity, accuracy and reliability in operation. This opens wide range of applications for MEMS devices and can be fabricated similar to ICs or MOSFET chips. Currently MEMS applications are in fields such as sensors, power generators, biological research, tele-communications, displays etc. [66-69] In addition to these applications; one prominent field of application for MEMS structure is for investigating material properties of thin films [70-75]. (cf. Paper A, B, C)

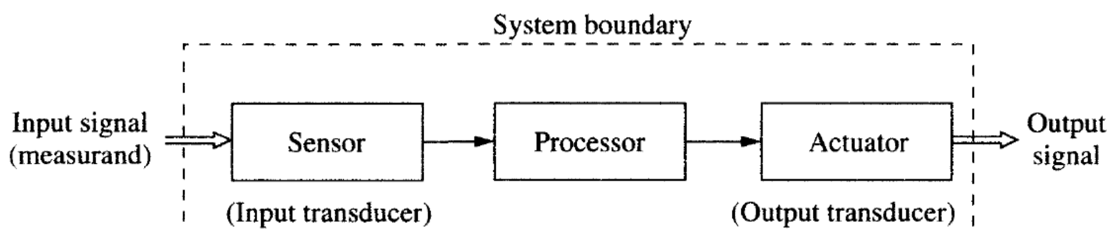

Figure 18. A pictorial representation of various basic elements of MEMS device; namely sensor, processing unit and actuator [62].

The field of material science is following the path of advances in micro-electronics industry where device dimensions are shrinking [66,68,71]. In order to accommodate these demands, dimensions of various films used in MOSFET technologies are also shrinking from macro, to micro to even nanoscale. Such a rigorous change in dimensions not only alter material properties of these films but also might offer completely new properties to thin metal films [76,77]. This requires an extensive study of thin films of various existing materials such as oxides, nitride, and metals from reliability point of view. In addition to it, there is constant search for new generation of materials to fulfill demands of new insulating materials, thin metals for low resistivity interconnects, advanced metal barriers, new contact metals etc. [8,10,15]. There is considerable knowledge available for many materials in bulk state, which might not be the same when dimensions are reduced to micro or even nanoscale [8,76,77]. Conclusively, there is a need of a dedicated test bench for the substantial study of thin films to evaluate their material properties, such as residual stress, Young's modulus, fracture strength, yield strength etc. (cf. Paper B). MEMS structures are coming up on this front as a reliable solution for investigating various material properties of thin films from their application point of view [64,78,79].

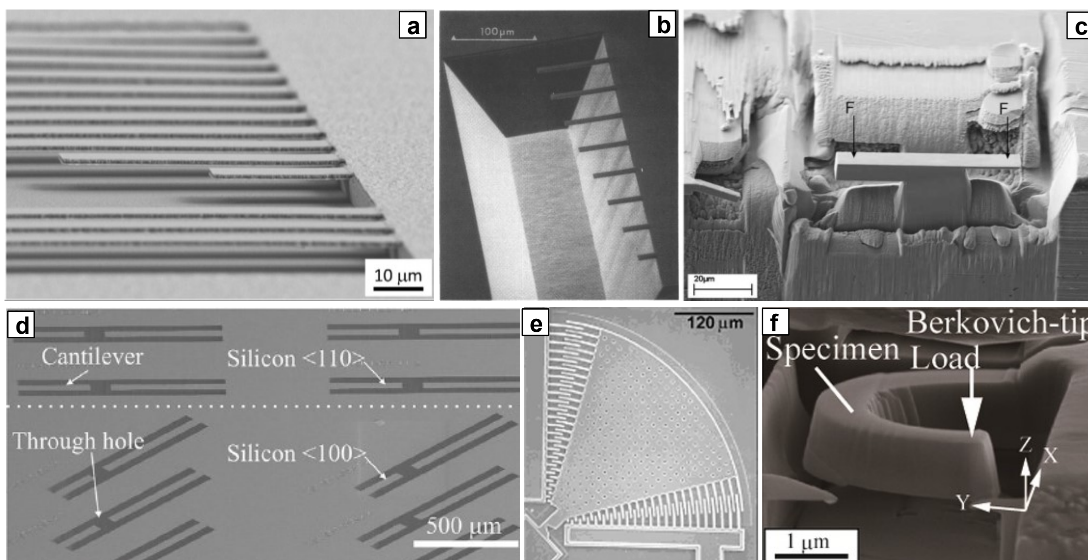

Figure 19. SEM micrographs of MEMS cantilevers for thin film characterization. (a, b, c & d) are different cantilever structures fabricated using surface micromachining, bulk micromachining , FIB milling and SOI technology respectively. (e) Poly silicon resonant cantilever for fatigue testing of thin film and (f) curved cantilever of single crystalline copper [72, 77, 79, 83, 89, 92].

There are various kinds of MEMS structures that have been fabricated for the evaluating material properties of thin film. In simpler form, structures such as cantilevers, beams, silicon membranes and pillars are most commonly used [64,71-73]. Most of the studies are carried out by using versatile platform of nano-indentation [77,78,80]. MEMS structure will be carefully loaded with external load using nano indenter tool and amount of displacement or load to fracture is recorded. Based on it, material properties of thin film can be calculated [74,81-83]. (Similarly, in paper B micro cantilevers are used to study properties of thin copper film). Nano-indentation is thus a common approach for characterization of mechanical properties of thin films in a reliable manner; especially when material properties tend to vary under influence of process conditions or film dimensions [8,64,81,83]. Few exemplary images of standard MEMS structures such as beams or cantilevers together with numerous other designs, which are being used for extracting material properties of thin films, are shown in figure 19.

One important criterion for MEMS application in thin film characterization is their reliable fabrication. As stated before, MEMS field is extremely benefitted by progress in the field of silicon fabrication techniques due to advancement in semiconductor industry. Many of those fabrication processes are favorably adapted for the fabrication of MEMS structures. Few of those important techniques are elaborated in nutshell below.

5.2 MEMS Fabrication Techniques

5.2.1 Surface micromachining

Surface micromachining is most simple technique for producing MEMS structures and it consists of sequential process steps of deposition and etching of different thin films [64,65]. The typical thickness of thin film, which is used in this case, is 1 to 100µm. In this method, material is deposited on the substrate and sequentially patterned. Thus, structures are created on the substrate and substrate doesn't become part or element of the device. A simple example stated in figure 20a illustrates the concept of surface micromachining. At beginning, a sacrificial layer was deposited and structured on the substrate. This can be typically silicon dioxide layer. Further on, poly silicon of desired thickness was deposited and structured. Finally, the sacrificial layer was etched away to get freestanding cantilevers

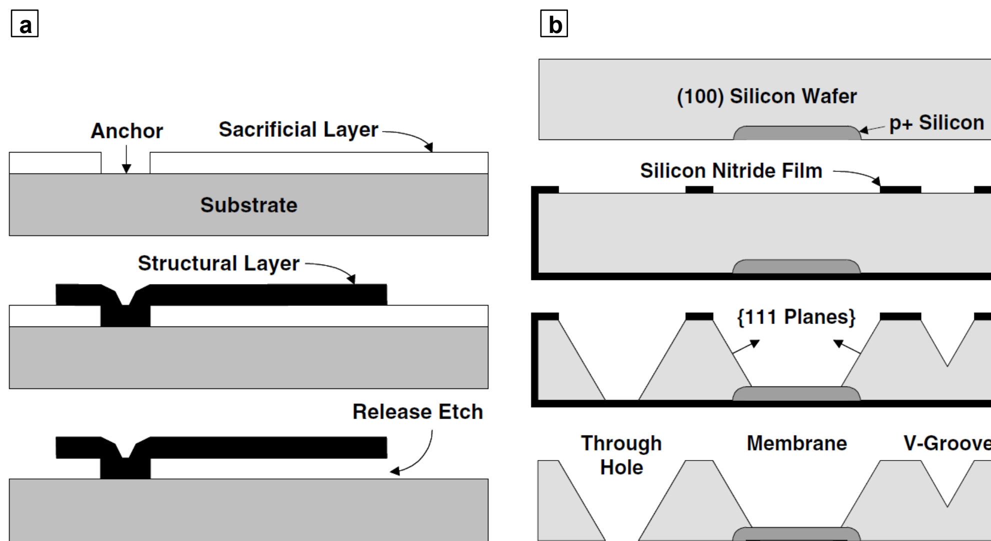

Figure 20. A schematic representation of two basic micromachining techniques. (a) Surface micromachining technique to create poly silicon cantilever structure. (b) Bulk micromachining method to create silicon membrane [64].

of chosen dimensions. Howe et. al. have successfully demonstrated usefulness of this fabrication process way back in 1983 by creating cantilevers of poly-silicon material [26]. The method can also be used to form far more complicated structures such as resonant cantilever structure for fatigue testing of metal [66,79].

5.2.2 Bulk micromachining

Bulk micromachining utilizes the substrate itself for fabricating MEMS devices [64,66,79,85]. For this purpose, properties of single crystal silicon as well as various fabrication processes are utilized effectively to generate different shapes and sizes of functional components of MEMS devices. In order to do so, one can use deep reactive ion etching, wet chemical etching, selective implants to form shapes such as v-grooves, pyramidal membranes, etc. in silicon [64,85]. However, during etching processes, critical areas are protected by either using photoresist or silicon dioxide. The etchant should have reasonable selectivity between protective layers and silicon to ensure good etching without attacking critical areas. Figure 20b shows classical example of making a membrane from a silicon substrate. The silicon substrate was selectively implanted by p type dopant, followed by oxidation of the substrate. The oxide was then structured to create opening of defined dimensions. Finally, the silicon substrate was wet chemically etched to generate the

membrane, hole as well as V-groove. A concise overview on bulk micromachining methods, processes and exemplary devices fabricated by using this technique are available [64,79,85].

5.2.3 Focused ion beam milling (FIB)

Focused ion beam milling is an alternative way to micro machine the MEMS structure out of thin film of desired material [80,86,87]. Advantages of this method over electron beam lithography are many. Few among them to list are high current density, capability of very fine focusing, choice of wide variety of ion masses, large energy density, short penetration depth in solids etc. [86,87] The process of device fabrication has four major steps; namely milling, deposition, implantation and imaging. The milling is process of material removal where solid surface is bombarded with a beam of ions (see figure 21 left) [86]. The surface atoms of thin film receive energy. If energy is higher than the binding energy, atoms will be sputtered away. Physical sputtering is major mechanism of material removal. On the other hand, if energy received by surface atoms is lower than binding energy, they remain excited but will be not sputtered away. Such atoms can relax by giving their energy to adsorbed gas molecules supplied by injection nozzle. These gas molecules will be dissociated to form a thin film on the substrate. This concludes second step of FIB termed as "deposition". By means of sequential milling and deposition steps, one can form a desired structures using

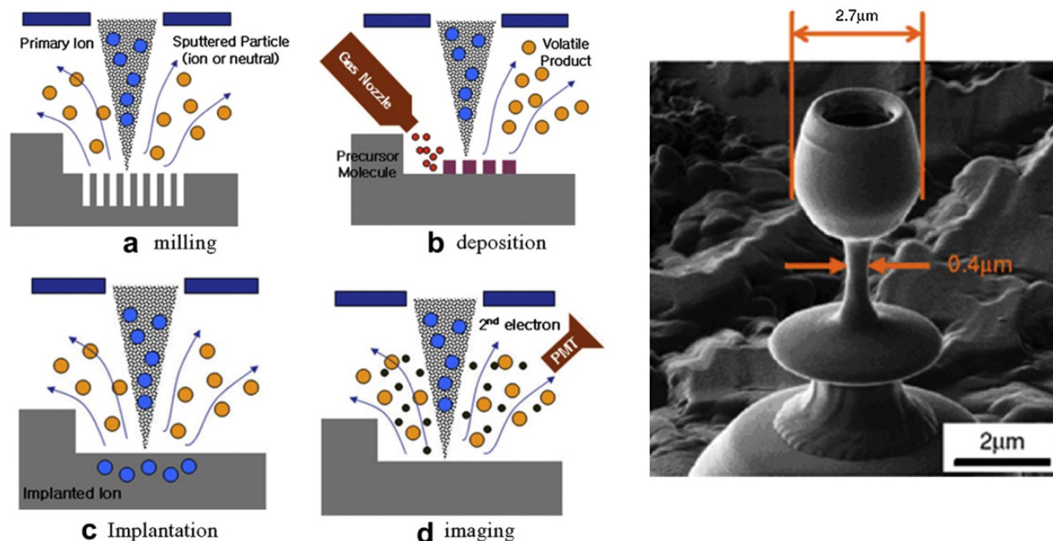

Figure 21. (left) show four major components of focused ion beam machining technique. (right) Few micrometer sized wine glass milled using focus ion beam technique. It represents the ability of FIB method to fabricate complex 3D structures [86].

FIB technique. Implantation as third step can modify the material surface, while forth step called imaging is a technique to provide micro scale analysis for material characterization.

This technique is quite useful to carve out various complicated structures, which can be used for investigating and testing different material properties. Figure 21 right, shows a micron sized wine glass machined by using FIB-CVD technique to demonstrate resourcefulness of this method. [86] By using four different steps of FIB mentioned above, MEMs structures of different shapes can be milled out of various materials and same technique has been used in several studies [77,88,89]. A broad overview stating important aspects of FIB is summarized here [86,87].

5.2.4 Silicon on insulator (SOI) technology

SOI is a special kind of substrate where thin oxide layer is sandwiched between the two silicon substrates. The buried oxide layer acts as a selective stop layer, facilitating the structuring of top and bottom silicon independent to each other and thus provides a great freedom for device fabrication [70-72,74]. The top layer is mainly used for fabricating active parts of MEMS device while bottom part is etched to form cavity underneath. The cavity provides formation of free standing device after etching away the buried oxide. Structures can be made by using standard lithography and direct reactive ion etching (DRIE) technique for silicon etching. Another advantage of this method is that thickness of structure can be tuned simply by choosing appropriate thickness of top silicon. The process can be used for manufacturing simple structures such as cantilever till complicated structures such as membrane using same methodology [70,71].

Various kinds of methods can be used to fabricate different MEMS structures. In spite of that, still most commonly used structures for the micro/nano scale analysis of material are cantilevers and beams. Within this work, a process flow based on SOI technology was developed to fabricate systematically designed structures for characterization of thin film. (cf. Paper A, B). Furthermore, a summary on various structures and their application for investigating material properties of various thin films is explained.

5.3 Application of MEMS structures for material characterization

Over past years, several studies have been published on investigation of material properties of thin film using MEMS structures. The simplest and most commonly used structures are cantilevers and beams. Cantilevers can be fabricated using several fabrication techniques

including all four methods listed above [70,74,77,83]. They can be prepared by using bulk micromachining technique. For example, cantilever can be simply made up of silicon dioxide. As dimension of cantilever is decided over photolithography, a wide range of cantilever length can be chosen. Weih et. al has calculated yield strength and young modulus of silicon oxide and gold film [83]. Using nano indenter tool, oxide cantilevers were indented at room temperature. Based on their deflection curves, young's modulus was calculated for the thermal oxide to be 64 GPa±10% while same for the low temperature oxide (LTO) was 44 GPa±5% . The gold film deposited on same cantilever was found to have E-modulus of value 57 GPa±11%. Sasangka et. al. employed same kinds of silicon dioxide cantilever for measuring the young modulus, residual stress and fracture strength of copper-tin-indium (Cu-Sn-In) thin film for broad range of their alloying composition [90]. The cantilevers were fabricated using wet chemical structuring of oxide followed by anisotropic wet etch of silicon in tetra methyl ammonium hydroxide (TMAH) solution. The film of three metals was deposited using combinatorial sputter deposition and elemental concentration decided using EDX analysis. The calculation of young's modulus for different phases were in good agreement with literature values. The technique of using arrays of cantilever together with combinatorial sputtering process allows characterization of alloys of different composition.

Similar to silicon dioxide cantilever, silicon cantilever can also be fabricated by bulk micromachining technique for investigating material properties of thin film. Grochla and his team developed sensor arrays of silicon cantilevers with the help of direct reactive ion etching from wafer front side and KOH wet etching from wafer backside to form free standing arrays [73]. The measurement technique was based on the stress induced by bending of the sensor and arrays are sensible to measure film thickness change in few nanometer range. The author has claimed to have application of these sensor arrays to measure the residual stress, film thickness inhomogeneity, determining coefficient of thermal expansion (CTE) etc. Two kinds of silicon cantilevers were manufactured using SOI technology to determine elastic-plastic and stress-strain relations of thin metal films [74]. The micro-beams were fabricated using standard semiconductor processing techniques followed by wet chemical etch of substrate using tetra methyl ammonium hydroxide (TMAH) solution. The front and backside etching was aligned over the lithography. On them, copper thin film was deposited with either oxide or tantalum as separating layer. The residual stress of the film was calculated by beam bending experiments in indenter. Results showed yield stress of copper increases with decreasing grain size and decreasing the film thickness. They also showed strain hardening rate is dependent on the texture of the film.

Silicon cantilevers are also used to measure Young's modulus of lead zirconate titanate (PZT) thin film [72]. PZT film itself is one of the interesting materials for the MEMS application due to its piezoelectric properties. The silicon cantilevers were fabricated using SOI technology and DRIE silicon etch for front and backside of the wafer. Cantilevers of different crystal orientation (100) and (110) were fabricated to ease the measurement of residual stress in the PZT film (see figure 22). The residual stress of PZT film was always tensile in nature but its value was dependent on its composition as well as on substrate orientation.

There are also several studies in which cantilevers were fabricated from the material of interest itself. A thin film of pure silicon dioxide or stack of silicon dioxide-silicon nitride were micro-machined to form a cantilever without any support of foreign material [82,91]. The material of desired thickness was deposited on silicon substrate, followed by structuring of the film in form of a preferred cantilever shape using photolithography. Finally, the substrate underneath the structure was etched away using wet chemical etching to get free standing cantilever. These cantilevers were subjected to the fracture at previously induced crack with the help of FIB. The material properties of silicon dioxide, silicon nitride and silicon oxynitride were calculated and it also demonstrated that strength of multilayer cantilever is determined by surface defects rather than defects at interface. Ghidelli and co-workers had followed same approach to fabricate composite beam of TiW and gold thin film [92]. The two thin films were sputter deposited, structured using lithography and finally the substrate was etched away underneath the structure to obtain freestanding cantilevers and beams. Using these beams and cantilevers, an analytical approach is demonstrated to calculate the residual stress and E-modulus of TiW and gold film by suing nano-indentation approach. Author has also demonstrated the typical parabolic behavior of stiffness as a function of distance of indenter point from the clamped end. In another untraditional approach, properties of $Ti_{1-x}Al_xN$ thin film cantilever were investigated in transmission electron microscopy (TEM) [88]. The film of $Ti_{1-x}Al_xN$ was deposited by tuning the sputter power to gain a defined gradient of aluminum and titanium content

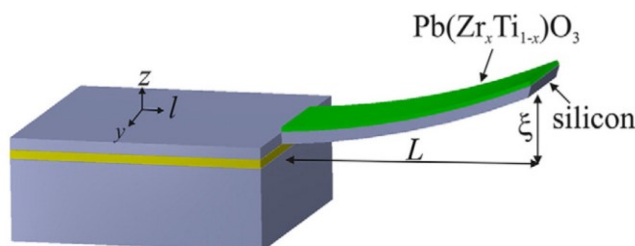

Figure 22. Simple cantilever structure fabricated using SOI technology for characterizing thin films [72].

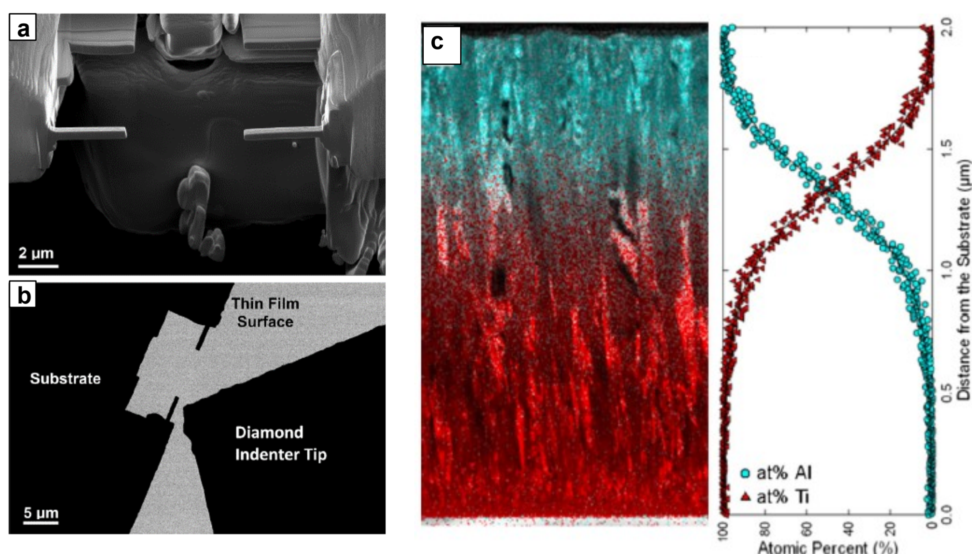

Figure 23. (a) Cantilever beam fibbed out of sputter deposited TiAlN film. (b) TEM image showing indentation of cantilever using diamond tip and (c) shows Ti and Al compositional gradient measured using EDS-STEM analysis [88].

over the film thickness (see figure 23). Out of this film, cantilevers were milled out from various areas across the cross-section to obtain cantilevers of different compositions. These cantilevers were subjected to bending experiments in the TEM and based on the displacement values, young modulus and fracture toughness for $Ti_{1-x}Al_xN$ film of varying value of x were calculated. Values recorded for above mentioned properties, were found to be higher for higher titanium content in the film compared to the one with aluminum. Koiwa et. al. have fabricated curved cantilever out of single crystal copper by using FIB technique to load the single crystal copper with torsional force [89]. The purpose of this experiment is to develop understanding about deformation behavior of micro scale crystal structure.

6. Summary and conclusion

Investigation of thin films demands a reliable platform to evaluate impact of various factors such as dimensions, morphology or crystal structure on their material properties. MEMS based structures have proven to be useful in this matter. Till this date, one or another type of cantilever based structures are used for this purpose. This is because, the study was concentrated on investigating different mechanical properties such as young's modulus, fracture toughness, yield strength etc. of thin films and less attention was given towards evaluation of material properties in combination with substrate, various deposition processes and post processing conditions etc. Thus present study comprises of a methodology including a fabrication technique to generate kinds of MEMS structures and characterization of thin metal films for its properties.

Various MEMS structures such as straight or curved cantilevers, beams, plus shaped structures and theta shaped structures were fabricated using state of the art SOI technology. A pragmatic approach involved fabrication of structures, deposition and structuring of thin film and offers an ability to tune interface properties between structure and thin film. In spite of the fact that these structures have dimensions in range of hundreds of micron and thickness in range of couple of microns, they are quite stable and can be used to load thin metal films in varying operating conditions.

The second major part of this work dealt with characterization of thin films of copper and diffusion barrier used in semiconductor world. By using fabricated structures, properties of thin copper film such as thermo-mechanical behavior, fatigue behavior under vibration load and fracture toughness were investigated. The thermo-mechanical investigation of copper depicts hysteresis curve over the temperature regime and thus are ideal design for studying interface between thin film and substrate. Moreover, plus structure found to be a perfect MEMS based structure, in simulation as well as experimentally, for loading thin films to study their fatigue behavior. Under cyclic vibrational loading, nano-crystalline copper revealed fatigue deformation in concentrated areas. Therefore, plus structure is found to offer a platform for studying thin metal films. In addition to it, micro cantilevers are found to be suitable structures to evaluate stiffness or fracture mechanism of thin film using nano-indentation technique. It was found that fracture load of thin copper film was reduced with increasing grain size of copper. Furthermore, morphological aspects of TiW diffusion barrier were studied and analogy between deposition conditions and intrinsic properties of TiW film was drawn based on Thornton's model for sputter deposited thin film.

The current work is a comprehensive approach to investigate properties of thin films using MEMS based structure. It comprises fabrication method for MEMS based structures, design and development of new structures and most importantly introducing a new platform for investigation of thin metal films for their material properties in broader aspects.

References

1. Hu, C., *Modern Semiconductor Devices for Integrated Circuits*2010: Prentice Hall.
2. Hoffmann, K., *System Integration: From Transistor Design to Large Scale Integrated Circuits*2006: Wiley.
3. Ytterdal, T., Y. Cheng, and T.A. Fjeldly, *Device Modeling for Analog and RF CMOS Circuit Design*2003: Wiley.
4. Nelhiebel, M., et al., *A reliable technology concept for active power cycling to extreme temperatures.* Microelectronics Reliability, 2011. **51**(9): p. 1927-1932.
5. Murarka, S.P., *Multilevel interconnections for ULSI and GSI era.* Materials Science and Engineering: R: Reports, 1997. **19**(3): p. 87-151.
6. Hille, F., et al., *Reliability aspects of copper metallization and interconnect technology for power devices.* Microelectronics Reliability, 2016. **64**: p. 393-402.
7. Nelhiebel, M., et al., *Effective and reliable heat management for power devices exposed to cyclic short overload pulses.* Microelectronics Reliability, 2013. **53**(9): p. 1745-1749.
8. Gupta, T., *Copper Interconnect Technology*2008: McGraw-Hill Professional Publishing.
9. Sze, S.M. and K.K. Ng, *Physics of Semiconductor Devices*2006: Wiley.
10. Rosenberg, R., et al., *Copper Metallization for High Performance Silicon Technology.* Annual Review of Materials Science, 2000. **30**(1): p. 229-262.
11. Maex, K., et al., *Stability of As and B doped Si with respect to overlaying CoSi2 and TiSi2 thin films.* Journal of Materials Research, 1989. **4**(5): p. 1209-1217.
12. Yamada, K., K. Tomita, and T. Ohmi, *Formation of metal silicide‐silicon contact with ultralow contact resistance by silicon‐capping silicidation technique.* Applied Physics Letters, 1994. **64**(25): p. 3449-3451.
13. He, M. and T.M. Lu, *Metal-Dielectric Interfaces in Gigascale Electronics: Thermal and Electrical Stability*2012: Springer New York.
14. Nicolet, M.A., *Diffusion barriers in thin films.* Thin Solid Films, 1978. **52**(3): p. 415-443.

15. Shacham-Diamand, Y., et al., *Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications*2009: Springer-Verlag New York.

16. Kaloyeros, A.E. and E. Eisenbraun, *Ultrathin Diffusion Barriers/Liners for Gigascale Copper Metallization.* Annual Review of Materials Science, 2000. **30**(1): p. 363-385.

17. Uekubo, M., et al., *WNx diffusion barriers between Si and Cu.* Thin Solid Films, 1996. **286**(1): p. 170-175.

18. Chen, G.S., et al., *Evaluation of single- and multilayered amorphous tantalum nitride thin films as diffusion barriers in copper metallization.* Journal of Vacuum Science & Technology A, 2000. **18**(2): p. 720-723.

19. Shih, K.K. and D.B. Dove, *Ti/Ti-N Hf/Hf-N and W/W-N multilayer films with high mechanical hardness.* Applied Physics Letters, 1992. **61**(6): p. 654-656.

20. Shen, Y.G. and Y.W. Mai, *Effect of oxygen on residual stress and structural properties of tungsten nitride films grown by reactive magnetron sputtering.* Materials Science and Engineering: B, 2000. **76**(2): p. 107-115.

21. Chang, T.S., et al., *Thermal stability study of TiN/TiSi2 diffusion barrier between Cu and n+Si.* Journal of Applied Physics, 1994. **75**(12): p. 7847-7851.

22. Holloway, K., et al., *Tantalum as a diffusion barrier between copper and silicon: Failure mechanism and effect of nitrogen additions.* Journal of Applied Physics, 1992. **71**(11): p. 5433-5444.

23. Min, K.H., K.C. Chun, and K.B. Kim, *Comparative study of tantalum and tantalum nitrides (Ta2N and TaN) as a diffusion barrier for Cu metallization.* Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 1996. **14**(5): p. 3263-3269.

24. Wang, H., et al., *Copper diffusion characteristics in single-crystal and polycrystalline TaN.* Applied Physics Letters, 2002. **81**(8): p. 1453-1455.

25. Kolawa, E., et al., *Tantalum-based diffusion barriers in Si/Cu VLSI metallizations.* Journal of Applied Physics, 1991. **70**(3): p. 1369-1373.

26. Soto, G., et al., *Tungsten nitride films grown via pulsed laser deposition studied in situ by electron spectroscopies.* Applied Surface Science, 2003. **214**(1): p. 58-67.

27. Pokela, P.J., et al., *Performance of W100−xNx diffusion barriers between 〈Si〉 and Cu.* Applied Surface Science, 1991. **53**: p. 364-372.

28. Migita, T., et al., *Effect of dc bias on the compositional ratio of WNX thin films prepared by rf-dc coupled magnetron sputtering.* Applied Surface Science, 2001. **169-170**: p. 362-365.

29. Chiu, H.-T. and S.-H. Chuang, *Tungsten nitride thin films prepared by MOCVD.* Journal of Materials Research, 1993. **8**(6): p. 1353-1360.

30. Ding, P.J., et al., *Oxidation resistant high conductivity copper films.* Applied Physics Letters, 1994. **64**(21): p. 2897-2899.

31. Frederick, M.J., R. Goswami, and G. Ramanath, *Sequence of Mg segregation, grain growth, and interfacial MgO formation in Cu–Mg alloy films on SiO2 during vacuum annealing.* Journal of Applied Physics, 2003. **93**(10): p. 5966-5972.

32. Koike, J. and M. Wada, *Self-forming diffusion barrier layer in Cu–Mn alloy metallization.* Applied Physics Letters, 2005. **87**(4): p. 041911.

33. Liu, C.J. and J.S. Chen, *Low leakage current Cu(Ti)/SiO2 interconnection scheme with a self-formed TiOx diffusion barrier.* Applied Physics Letters, 2002. **80**(15): p. 2678-2680.

34. Usui, T., et al. *High Performance Ultra Low-k (k=2.0/keff=2.4)/Cu Dual-Damascene Interconnect Technology with Self-Formed MnSixOy Barrier Layer for 32 nm-node*. in *2006 International Interconnect Technology Conference*. 2006.

35. Ding, P.J., et al., *Effects of the addition of small amounts of Al to copper: Corrosion, resistivity, adhesion, morphology, and diffusion.* Journal of Applied Physics, 1994. **75**(7): p. 3627-3631.

36. Canali, C., et al., *Interdiffusion and compound formation in the c□Si/PtSi/(Ti□W)/Al system.* Thin Solid Films, 1982. **88**(1): p. 9-23.

37. Nowicki, R.S., et al., *Studies of the Ti-W/Au metallization on aluminum.* Thin Solid Films, 1978. **53**(2): p. 195-205.

38. Oparowski, J.M., R.D. Sisson, and R.R. Biederman, *The effects of processing parameters on the microstructure and properties of sputter-deposited TiW thin film diffusion barriers.* Thin Solid Films, 1987. **153**(1): p. 313-328.

39. Ghate, P.B., et al., *Application of Ti: W barrier metallization for integrated circuits.* Thin Solid Films, 1978. **53**(2): p. 117-128.

40. Evans, D.R. and D.M. Leet, *3% Ti-Tungsten Diffusion Barriers: I . A Discussion of the Role of the A15 Structure.* Journal of The Electrochemical Society, 1994. **141**(7): p. 1867-1871.

41. Matoy, K., et al., *Interface fracture properties of thin films studied by using the micro-cantilever deflection technique.* Surface and Coatings Technology, 2009. **204**(6): p. 878-881.

42. Ramarotafika, H. and G. Lemperiere, *Influence of a d.c. substrate bias on the resistivity, composition, crystallite size and microstrain of WTi and WTi-N films.* Thin Solid Films, 1995. **266**(2): p. 267-273.

43. Hartsough, L.D., *Resistivity of bias-sputtered TiW films.* Thin Solid Films, 1979. **64**(1): p. 17-23.

44. Völker, B., et al., *Mechanical and chemical investigation of the interface between tungsten-based metallizations and annealed borophosphosilicate glass.* Thin Solid Films, 2015. **583**: p. 170-176.

45. Okamoto, H., Schlesinger, M., and Mueller, E., ASM Handbook : Alloy Phase Diagram 1993: ASM International.

46. Bergstrom, D.B., I. Petrov, and J.E. Greene, *Al/TixW1−x metal/diffusion-barrier bilayers: Interfacial reaction pathways and kinetics during annealing.* Journal of Applied Physics, 1997. **82**(5): p. 2312-2322.

47. Plappert, M., et al., *Characterization of Ti diffusion in PVD deposited WTi/AlCu metallization on monocrystalline Si by means of secondary ion mass spectroscopy.* Microelectronics Reliability, 2012. **52**(9): p. 1993-1997.

48. Tu, K.N., *Recent advances on electromigration in very-large-scale-integration of interconnects.* Journal of Applied Physics, 2003. **94**(9): p. 5451-5473.

49. Wong, H.Y., N.F. Mohd Shukor, and N. Amin, *Prospective development in diffusion barrier layers for copper metallization in LSI.* Microelectronics Journal, 2007. **38**(6): p. 777-782.

50. Chromik, R.R., W.K. Neils, and E.J. Cotts, *Thermodynamic and kinetic study of solid state reactions in the Cu–Si system.* Journal of Applied Physics, 1999. **86**(8): p. 4273-4281.

51. Ward, W.J. and K.M. Carroll, *Diffusion of Copper in the Copper-Silicon System.* Journal of The Electrochemical Society, 1982. **129**(1): p. 227-229.

52. Li, B., et al., *Reliability challenges for copper interconnects.* Microelectronics Reliability, 2004. **44**(3): p. 365-380.

53. Rossnagel, S.M., R. Powell, and A. Ulman, *PVD for Microelectronics: Sputter Desposition to Semiconductor Manufacturing*1998: Elsevier Science.

54. Thornton, J.A., *The microstructure of sputter-deposited coatings.* Journal of Vacuum Science & Technology A, 1986. **4**(6): p. 3059-3065.

55. Craig, S. and G.L. Harding, *Effects of argon pressure and substrate temperature on the structure and properties of sputtered copper films.* Journal of Vacuum Science and Technology, 1981. **19**(2): p. 205-215.

56. Lingk, C. and M.E. Gross, *Recrystallization kinetics of electroplated Cu in damascene trenches at room temperature.* Journal of Applied Physics, 1998. **84**(10): p. 5547-5553.

57. Patten, J.W., E.D. McClanahan, and J.W. Johnston, *Room-Temperature Recrystallization in Thick Bias-Sputtered Copper Deposits.* Journal of Applied Physics, 1971. **42**(11): p. 4371-4377.

58. Hertzberg, R.W., P.R. Vinci, and J.L. Hertzberg, *Deformation and fracture mechanics of engineering materials*1996: J. Wiley & Sons.

59. Toomey, J.J., S. Hymes, and S.P. Murarka, *Stress effects in thermal cycling of copper (magnesium) thin films.* Applied Physics Letters, 1995. **66**(16): p. 2074-2076.

60. Keller, R.M., S.P. Baker, and E. Arzt, *Quantitative analysis of strengthening mechanisms in thin Cu films: Effects of film thickness, grain size, and passivation.* Journal of Materials Research, 1998. **13**(5): p. 1307-1317.

61. Bigl, S., et al., *Film thickness dependent microstructural changes of thick copper metallizations upon thermal fatigue.* Journal of Materials Research, 2017. **32**(11): p. 2022-2034.

62. Gardner, J.W., V.K. Varadan, and O.O. Awadelkarim, *Microsensors, MEMS, and Smart Devices*2010: Springer Berlin Heidelberg.

63. Jiang, L. and R. Cheung, *A review of silicon carbide development in MEMS applications.* International Journal of Computational Materials Science and Surface Engineering, 2009. **2**(3-4): p. 227-242.

64. Judy, J.W., *Microelectromechanical systems (MEMS): fabrication, design and applications.* Smart Materials and Structures, 2001. **10**(6): p. 1115-1134.

65. Bustillo, J.M., R.T. Howe, and R.S. Muller, *Surface micromachining for microelectromechanical systems.* Proceedings of the IEEE, 1998. **86**(8): p. 1552-1574.

66. Korvink, J. and O. Paul, *MEMS: A Practical Guide of Design, Analysis, and Applications*2010: Springer Berlin Heidelberg.

67. Moore, D.F. and R.R.A. Syms *Recent developments in micromachined silicon*. Electronics & Communication Engineering Journal, 1999. **11**, 261-270.

68. Osterberg, P.M. and S.D. Senturia, *M-TEST: A test chip for MEMS material property measurement using electrostatically actuated test structures.* Journal of Microelectromechanical Systems, 1997. **6**(2): p. 107-118.

69. Yao, J.J., *RF MEMS from a device perspective.* Journal of Micromechanics and Microengineering, 2000. **10**(4): p. R9-R38.

70. Nazeer, H., et al., *Determination of the Young's modulus of pulsed laser deposited epitaxial PZT thin films.* Journal of Micromechanics and Microengineering, 2011. **21**(7): p. 074008.

71. Lalinský, T., et al., *Thermo-mechanical analysis of uncooled La0.67Sr0.33MnO3 microbolometer made on circular SOI membrane.* Sensors and Actuators A: Physical, 2017. **265**: p. 321-328.

72. Nazeer, H., et al., *Residual stress and Young's modulus of pulsed laser deposited PZT thin films: Effect of thin film composition and crystal direction of Si cantilevers.* Microelectronic Engineering, 2016. **161**: p. 56-62.

73. Grochla, D., et al., *Si micro-cantilever sensor chips for space-resolved stress measurements in physical and plasma-enhanced chemical vapour deposition.* Sensors and Actuators A: Physical, 2018. **270**: p. 271-277.

74. Florando, J.N. and W.D. Nix, *A microbeam bending method for studying stress–strain relations for metal thin films on silicon substrates.* Journal of the Mechanics and Physics of Solids, 2005. **53**(3): p. 619-638.

75. Haque, M.A. and M.T.A. Saif, *Application of MEMS force sensors for in situ mechanical characterization of nano-scale thin films in SEM and TEM.* Sensors and Actuators A: Physical, 2002. **97-98**: p. 239-245.

76. Arzt, E., *Size effects in materials due to microstructural and dimensional constraints: a comparative review.* Acta Materialia, 1998. **46**(16): p. 5611-5626.

77. Motz, C., T. Schöberl, and R. Pippan, *Mechanical properties of micro-sized copper bending beams machined by the focused ion beam technique.* Acta Materialia, 2005. **53**(15): p. 4269-4279.

78. Sebastiani, M., et al., *Measurement of fracture toughness by nanoindentation methods: Recent advances and future challenges.* Current Opinion in Solid State and Materials Science, 2015. **19**(6): p. 324-333.

79. Spearing, S.M., *Materials issues in microelectromechanical systems (MEMS).* Acta Materialia, 2000. **48**(1): p. 179-196.

80. Sebastiani, M., T. Sui, and A.M. Korsunsky, *Residual stress evaluation at the micro- and nano-scale: Recent advancements of measurement techniques, validation through modelling, and future challenges.* Materials & Design, 2017. **118**: p. 204-206.

81. Koumoulos, E.P., et al., *Metrology and nano-mechanical tests for nano-manufacturing and nano-bio interface: Challenges & future perspectives.* Materials & Design, 2018. **137**: p. 446-462.

82. Matoy, K., et al., *A comparative micro-cantilever study of the mechanical behavior of silicon based passivation films.* Thin Solid Films, 2009. **518**(1): p. 247-256.

83. Weihs, T.P., et al., *Mechanical deflection of cantilever microbeams: A new technique for testing the mechanical properties of thin films.* Journal of Materials Research, 1988. **3**(5): p. 931-942.

84. Howe, R.T. and R.S. Muller, *Polycrystalline Silicon Micromechanical Beams.* Journal of The Electrochemical Society, 1983. **130**(6): p. 1420-1423.

85. Adams, T.M. and R.A. Layton, *Introductory MEMS: Fabrication and Applications*2009: Springer-Verlag US.

86. Kim, C.-S., S.-H. Ahn, and D.-Y. Jang, *Review: Developments in micro/nanoscale fabrication by focused ion beams.* Vacuum, 2012. **86**(8): p. 1014-1035.

87. Tseng, A.A., *Recent Developments in Nanofabrication Using Focused Ion Beams.* Small, 2005. **1**(10): p. 924-939.

88. Zalesak, J., et al., *Cross-sectional structure-property relationship in a graded nanocrystalline Ti1−xAlxN thin film.* Acta Materialia, 2016. **102**: p. 212-219.

89. Koiwa, K., et al., *Investigation of continuous deformation behavior around initial yield point of single crystal copper by using micro scale torsion test.* Scripta Materialia, 2016. **111**: p. 94-97.

90. Sasangka, W.A., et al., *Characterization of the Young's modulus, residual stress and fracture strength of Cu–Sn–In thin films using combinatorial deposition and micro-cantilevers.* Journal of Micromechanics and Microengineering, 2015. **25**(3): p. 035023.

91. Matoy, K., et al., *Micron-sized fracture experiments on amorphous SiOx films and SiOx/SiNx multi-layers.* Thin Solid Films, 2010. **518**(20): p. 5796-5801.

92. Ghidelli, M., et al., *Determination of the elastic moduli and residual stresses of freestanding Au-TiW bilayer thin films by nanoindentation.* Materials & Design, 2016. **106**: p. 436-445.

7. List of appended publications

Paper A

Design and development of MEMS-based structures for in-situ characterization of thermo-mechanical behaviour of thin metal films

F. Saghaeian[a,b,*] , J. Keckes[b] , K.A. Schreiber[a] , T. Mittereder[c]

Published in Microelectronics Reliability, Volumes 88–90, 2018, Pages 829-834

https://doi.org/10.1016/j.microrel.2018.07.005

Paper B

Fabrication of MEMS based structures for characterization of thin metal films by nanoindentation technique

F. Saghaeian[a,b,*], J. Keckes[b], J. Zechner[c], S. Woehlert[a], K.A. Schreiber[a], H. Pfaff[d], J. Walter[d]

Published in IEEE xplore (March 2019)

DOI: 10.1109/EMAP.2018.8660918

Paper C

Investigation of high cyclic fatigue behaviour of thin copper films using MEMS structure

F. Saghaeian[a,b,*], M. Lederer[c], A. Hofer[a], J. Todt[b], J. Keckes[b], G. Khatibi[c]

Published in International Journal of Fatigue, Volumes 128, 2019, 105179

https://doi.org/10.1016/j.ijfatigue.2019.06.039

Paper D

Microstructure and Stress Gradients in TiW Thin Films Characterized by 40nm X-ray Diffraction and Transmission Electron Microscopy

F. Saghaeian[a,b,*] , J. Keckes[b], S. Woehlert[a], M. Rosenthal[c], M. Reisinger[d], J. Todt[e]

Submitted manuscript to Thin Solid Films (Jan 2019)

7.1 Contribution of the author to the papers

	Conception and planning	Experiments	Analysis and interpretation	Manuscript preparation
Paper A	100	90	90	95
Paper B	100	90	100	90
Paper C	100	100	80	90
Paper D	100	60	60	80

Table 1. Contribution of the Author to the appended publications in percent.

Paper A

Design and development of MEMS-based structures for in-situ characterization of thermo-mechanical behaviour of thin metal films

F. Saghaeian[a,b,*] , J. Keckes[b] , K.A. Schreiber[a] , T. Mittereder[c]

a Infineon Technologies Austia AG, 9500 Villach Austria

b Department of Materials Physics, Montanuniversitaet Leoben and Erich Schmid Institute for Materials Science, Austrian Academy of Sciences, Leoben, Austria

c Infineon Technologies AG, 85579 Neubiberg Germany

Microelectronics Reliability, Volumes 88–90, 2018, Pages 829-834

https://doi.org/10.1016/j.microrel.2018.07.005

Abstract

The reliability as well as performance of micro electronic devices strongly depends on the resistance to their thermal degradation induced during operation. In present work, a process flow is developed to fabricate Micro-Electro-Mechanical systems (MEMS) structures, which provide a reliable platform to study thermo-mechanical aspects of silicon-thin metal interface at different temperatures. Here different submicron structures such as cantilever, beams, plus sign, theta and curved cantilevers of varying dimensions are fabricated. The process demonstrates flexibility to manufacture different structures, where the thickness of silicon and of copper can be varied independent to each other. Features based on Si with thickness of 4 or 11µm coated with Cu of 0.5-3µm in thickness are manufactured and used as plus signs and curved cantilevers to study deformation over the temperature range of -50 to 400°C. Deflections from 3µm tensile to -8µm compressive are observed. This study gives an experimental evidence of behaviour of copper over thermal cycling using MEMS structure. Moreover, Si-Cu based structures are subjected to high temperature cycling to induce degradation and microstructure of their interface is studied. This methodology offers flexibility to characterize different kinds of thin films of various dimensions under individual process conditions.

1 Introduction

As semiconductor industry following along the Moore law, chips are getting smaller and smaller. This lead to increase in a current density within the chip and thereby, leading to increase in the thermal budget one chip has to deal with. This demands thicker metallization stack (power metal) with better thermal and electrical conductivity which copper can easily fulfill [1, 2]. However, apart from large mismatch in coefficient of thermal expansion between silicon and copper, behavior of copper as power metal is strongly influenced by its thickness, method of copper deposition as well as by loading conditions [3-5]. The last one is more important as every power MOSFET is designed for unique application and thus the thermal load on the power metal is different in every case. Moreover, in order to increase the performance of transistor, final thickness of silicon is decreasing leading to a situation thick metal on thin silicon. In addition, there is a need of diffusion barrier between the silicon and power metal which makes system complex to study [6, 7]. After considering all these parameters stated above, detailed study of power metal; copper in this case, is extremely convoluted. Therefore, in order to have systematic approach a platform based on novel structures of Micro-electro-mechanical systems (MEMS) is chosen for this current study.

MEMS have proven to be an ideal platform to study thin films for their mechanical properties and to do so numerous different structures are being used; among them cantilever and bridges are most famous ones [8-13]. However, in most of the cases, MEMS structures are micro-machined out of previously deposited bulk film [10, 11, 13, 14] or made up of silicon dioxide cantilevers [12, 16] or on silicon structures [8, 17] with smaller cavity space underneath. Such structures are reasonably good for measuring the material properties of the thin film such as modulus of elasticity or fracture strength under static mechanical loading. However as explained above, the performance of thin metal film depends on numerous factors and thus altogether it is a matter of extreme importance to design and fabricate appropriate structures offering defined silicon-thin power metal interface that can be subjected to thermo-mechanical loading under dynamic conditions [1]. However, simple beams or cantilevers are useful for unidirectional loading but in-appropriate for studying behavior of power metal, in semiconductor field. This is because the topography of the chip is strongly influenced by the MOSFET structures underneath leading to different loading conditions in x and y directions [1,2]. Thus, in this work fabrication of two novel structures, plus and curved cantilever together with different other structures such as beams, cantilevers, theta structures of varying dimensions based on silicon on insulator (SOI)

technology is demonstrated [17]. The process offers ease of tuning thickness of silicon and copper independent to each other together with the interface between the same. Finally, thermo-mechanical behavior of copper on these structures at high temperature is shown.

2 Experimental

Silicon on insulator (SOI) wafers of 200 mm diameter, (100) orientation and a phosphorus doped, are used for fabrication. Wafers have 1µm thick thermal oxide buried between a 5.2 µm top active layer and 725 µm base Si. For all cleaning steps standard RCA cleaning solutions were used. With the help of optical lithography and deep reactive-ion plasma (BOSCH) etching, structures were etched on front side and cavities on backside of wafer. A 6µm thick TEOS based filler oxide was deposited by plasma assisted (PECVD) technique to strengthen the wafer before backside cavity etch. This deposition was carried out at rate of 500nm/min. Chemical mechanical polishing (CMP) was carried out to remove additional oxide from surface of wafer at a rate of 6nm/sec. TiW and Cu were sputter deposited in-situ mode without any vacuum break. The chamber pressure for TiW deposition was maintained between 2 to 6x10-6 mbar[18] while the same for copper was between 2 to 4x10-6 mbar[18]. Argon flow was held constant in order to retain chamber pressure within the range. Copper was structured using phosphoric acid based chemistry at room temperature while TiW was etched using hydrogen peroxide at 25°C. In order to release the structure, oxide was wet etched in standard buffered oxide etch solution at room temperature.

A CT100 optical profilometer from Cyber Technologies Company was used to measure the membrane deflection during temperature cycling. Tool is equipped with confocal chromatic white light sensor. The nominal z-resolution of the sensor is 0.014µm with a spot size of 4µm [19]. Furthermore it was used in combination with an INSTEC heating/cooling chamber. The sample was heated and cooled in the chamber at 50°C/ min and held for about 4-5 minutes at every measurement point. The measurement was carried out under nitrogen atmosphere and chamber was purged sufficiently with nitrogen before heating the stage. The subzero temperatures were achieved circulation of liquid nitrogen.

3 Results and discussion

3.1 Fabrication of MEMS structures

The fabrication was carried out using a SOI wafer [17]. To produce alignment marks for lithography, 1µm of top silicon was consumed and thus top layer thickness was reduced to 4µm for device fabrication. A summary of process flow for device fabrication is as depicted in figure 1. After generation of alignment marks, using patterned photo-resist structures were plasma etched in top silicon with selective stop on box oxide. Thereafter, resist was removed and oxide was deposited to fill the cavities formed by etching. The same was then chemical-mechanically polished to remove additional oxide deposited on the structure and thereby minimizing the topography on wafer front side. In a subsequent step, wafer was thinned down to 400µm final thickness and cavities were etched on backside of wafer perfectly aligned to structures on wafer front side. At this stage, the process flow is divided into two subsets. The first subset offers structures with metal deposited on side wall while in another case; structures have no metal on side wall.

In subset 1 (see fig. 1), filler oxide and box oxide both were etched away using buffered oxide etch chemistry to obtain free standing structures. The oxide etch time was precisely controlled to avoid excessive under etch of oxide. This is particularly important as this defines the overhang of structures. After this, metal was sputter deposited. The

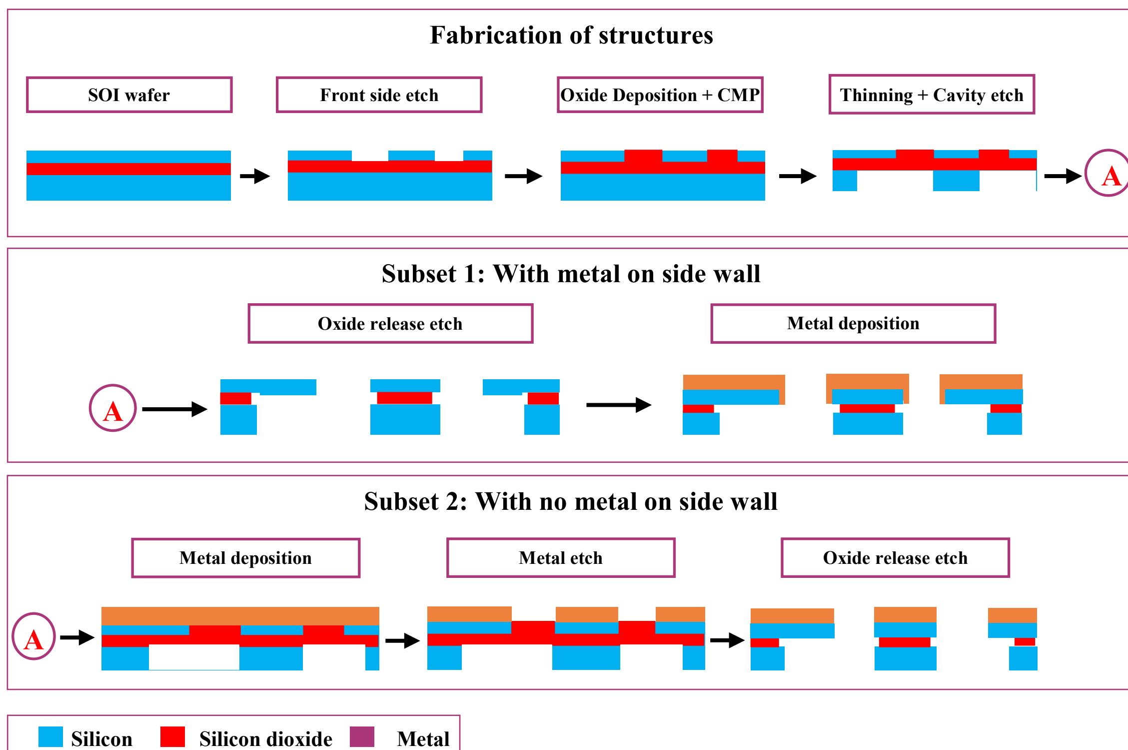

Fig. 1. Process flow for manufacturing different free standing silicon based structures of different dimensions

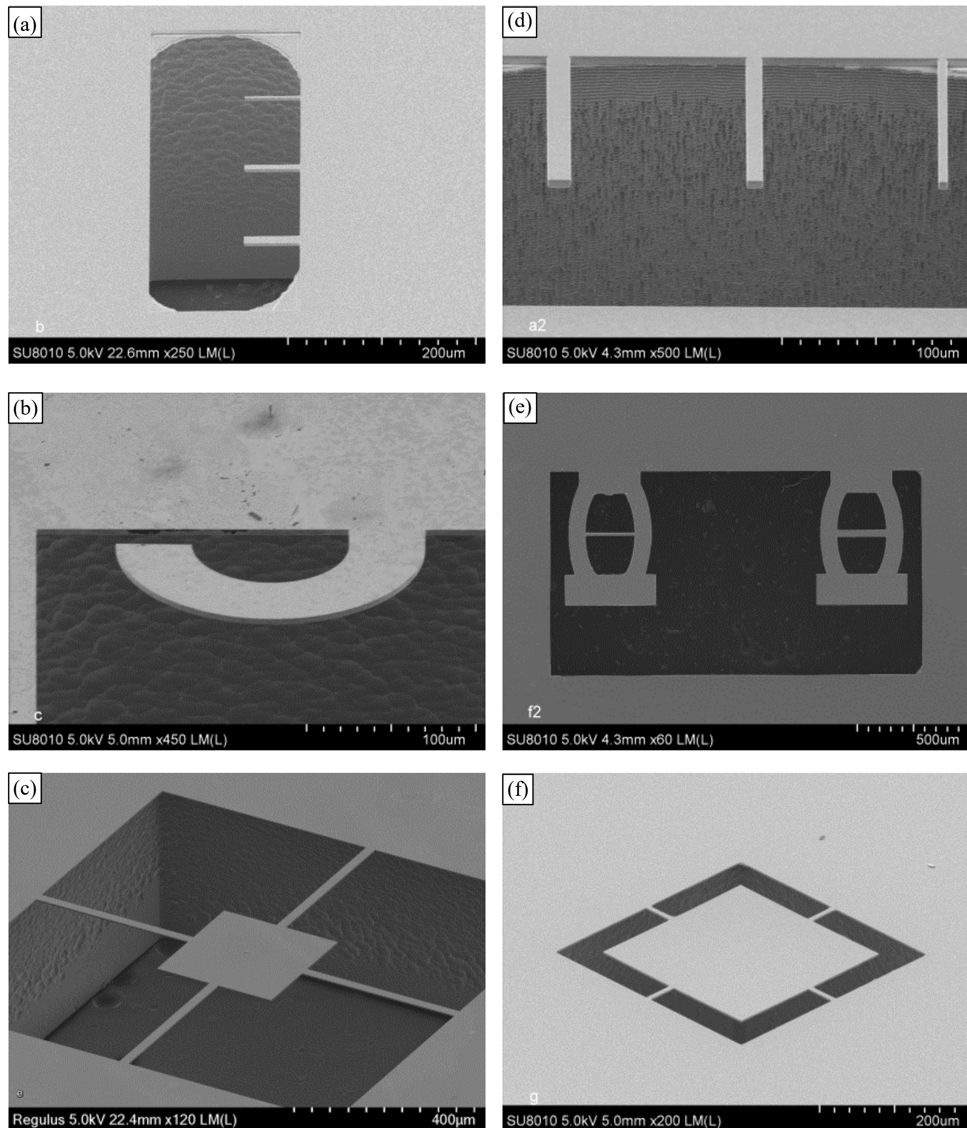

Fig. 2. SEM micrographs showing different free standing structures fabricated with copper on side wall. (a & d) cantilever (b) curved cantilever (c & f) plus structure

deposition was carried out with least energy to avoid any kind of mechanical damage to the structures. As structures were released before, the metal tends to deposit on side walls of structures. Few SEM micrographs of different structures deposited with 50nm TiW together with 2000nm Copper are depicted in figure 2.

As one can see, special effort is taken not only to choose different structures but also to fabricate same in different dimensions. This process flow offers a great degree of freedom to fabricate structures of any kind of complicated shape. By varying a top silicon thickness in SOI wafer, one can easily vary the thickness of final structure. Furthermore, as energy of metal sputtering process was less; copper film tends to grow with nano crystalline columnar

grains on top of structures while forming an inhomogeneous film of small agglomerates on their side wall (see fig. 3a &3b). In addition, thickness of film on side wall is lesser than thickness deposited. Thus, thick continuous film of copper on top of silicon structure induces major force during thermo- mechanical loading of structure in compare to one on side wall. This holds true as long as thickness of metal deposited on side wall is not too high which would otherwise influence deflection during temperature cycling.

In another process flow (subset 2), after the cavity-etch, metal was directly deposited on wafer front side. As oxide was filled in the cavities, no metal was deposited on the side wall of structures. The metal was then wet chemically structured with the help of resist mask. Finally the oxide was etched away as explained before. Selected SEM micrographs of such structures are as shown in figure 3. Subset1 is simplified version of subset 2, in which structuring of deposited metal is not required. It makes diffusion study of metals and alloys, where structuring is cumbersome, possible. Apart from this, structures fabricated from both process flows can be used for studying thermo-mechanical behavior of metal thin films.

3.2 Characterizations of fabricated structures

For the present study, a stack of TiW barrier and copper metal was chosen. A barrier constitutes of 50nm of TiW film while thin copper film of either 500 or 2000nm was deposited on it. Thickness of TiW film was intentionally limited to 50nm as otherwise influence of copper film will be hard to evaluate. For present study, plus structure of two different dimensions and a curved cantilever structure with copper deposited on side wall were chosen. These two structures were carefully chosen for this study due to its unique shape. The central square plate in plus structure offers a defined interface of silicon-power metal and the same can be loaded under different thermo-mechanical loading conditions. The stress generated here is either tensile or compressive in nature. However, curved cantilever generates torsional stress on interface during thermal cycling. After deposition of TiW/Cu Metal stack, it is observed that these two structures bend in opposite direction to each other. The plus structure bends in concave shape under the influence of tensile stress imposed by copper on silicon while under the same stress tip of the curved cantilever bends upwards. The initial bending of these structures under the influence of residual stress of the copper is measured using optical profilometer for different copper thicknesses. Two such images are shown in figure 4. Clearly the increase in thickness of copper led to higher deflection of the structure in pristine state.

These structures were studied under thermal load by using CT100 tool [19]. The structures were studied over a temperature range starting from room temperature to 400°C and then cooled down to -50°C in subsequent steps. The bending of the structure at every temperature interval of 100°C was documented using an optical interferometer (see figure 5). As reported in literature, over this temperature range, copper depicts initially elastic and then followed by plastic deformation giving rise to a hysteresis curve [20]. At room temperature, Plus2 structure with 2000nm Cu thickness, after deposition forms concave shape with total deflection of 2.45µm measured from edge to edge. Upon heating to higher temperature, the structure starts to bend in an opposite direction to form a convex shape.

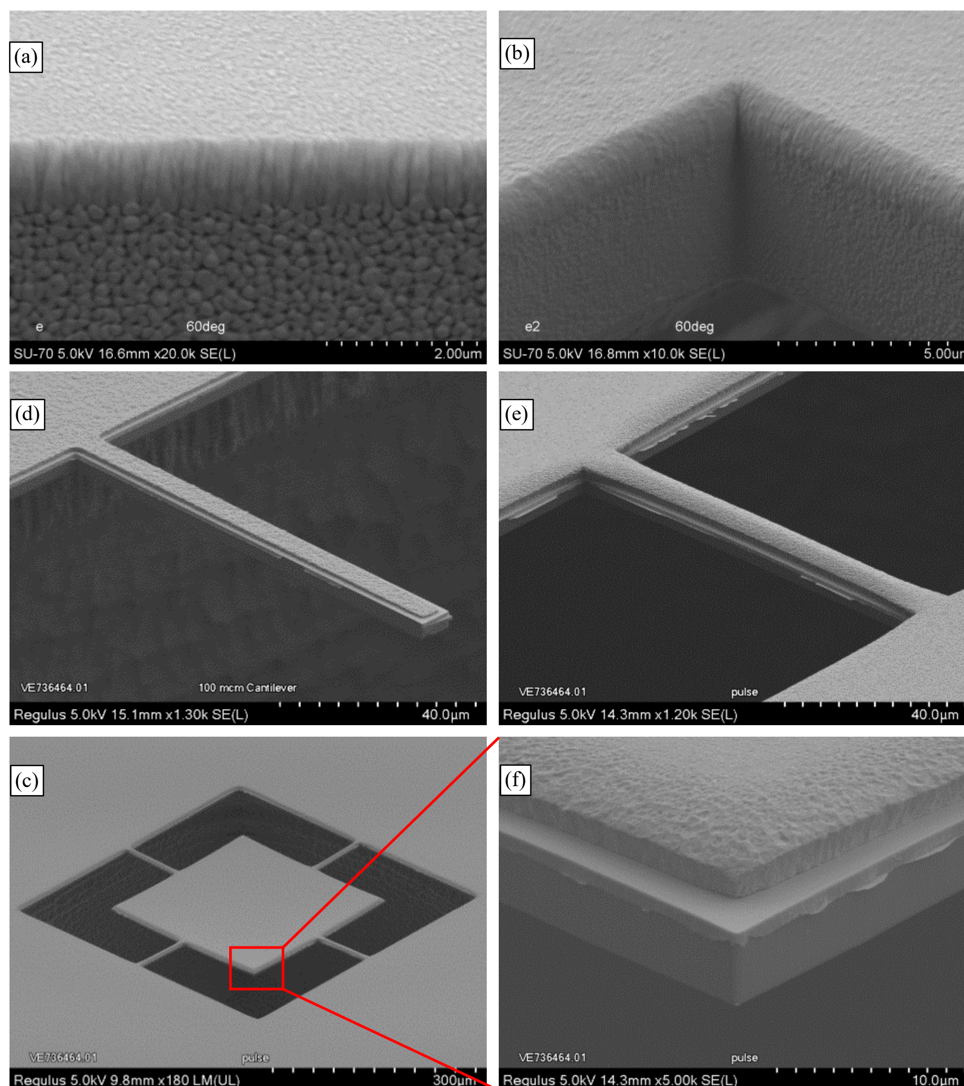

Fig. 3. SEM micrographs showing (a,& b) grain size and morphology of copper deposited on structures from subset 1 and (c,d,e & f) different structures fabricated using process flow “without copper on side wall” (Subset 2)

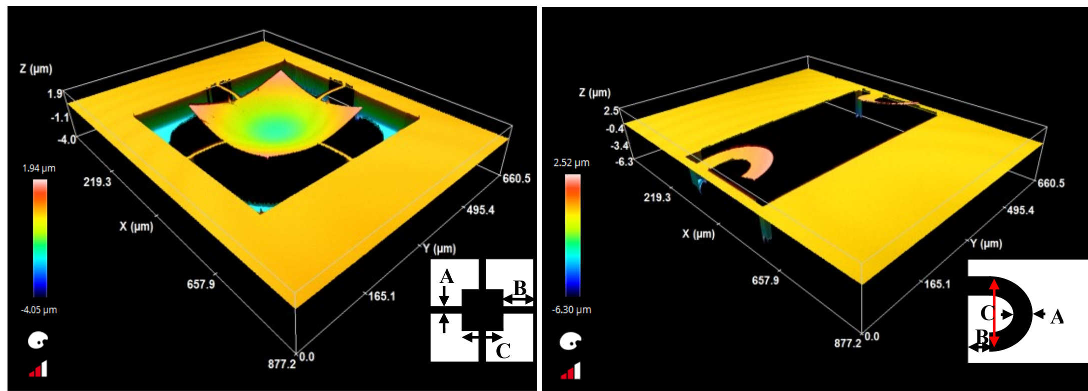

Fig. 4. 3D optical profilometer image of plus structure (left) and curved cantilever (right) showing deflection after metal deposition. Insets show schematics of same structure and their dimensions are listed in table 1.

The total deflection increases with increase in the temperature. Initial bending of 2.45µm at room temperature was changed to -7.8µm convex shape, resulting into total bending of 10.25µm over a temperature range of 25 to 400°C. Such a large deflection is primarily due to thick copper film for two reasons. First, thermal expansion coefficient of copper is ~6 times higher than that of silicon and second bare silicon structure without copper did not show any deflection (data not shown) [20, 21]. Upon cooling down, deflection decreases in a reverse order and finally at room temperature, the structure regains its original concave shape. However, it is worth to mention that, the degree of curvature of concave shape is now higher than that of pristine sample. This drift in deflection at room temperature is outcome

Structure	**Dimension (µm)**			
	A	B	Aspect ratio	C
Plus 1	10	50	5	300
Plus 2	10	100	10	300
Curved Cantilever	50	20	2.5	200

Table 1. Dimensions of different structures are listed as marked in inset of figure 4. (Aspect ratio = B/A).

of reorientation of copper grains due to thermal budget [21]. The same plus2 structure was subjected to the repetitive loading for 20 heating-cooling cycles. The hysteresis plot didn't

show any major change after thermal loading of 20 cycles. The delta in deflection which was observed at room temperature before and after first thermal cycle was not seen

after second cycle onwards. On the other hand, if the structure was cooled down to subzero temperature of -50°C, as shown in figure5j, the deflection was found to be higher (7.5µm) in comparison with room temperature value of 7µm. The curved cantilever replicated same behavior under thermal loading except for its deflection in opposite direction. The tip of curved cantilever which was bent initially in upward direction, during temperature cycling, it started bending downward with increasing temperature till 400°C and regained its original form upon cooling down.

The plot of deflection vs. temperature for different structures for first heating-cooling cycle is as shown in figure 6. The resulting plot reproduces the typical hysteresis profile

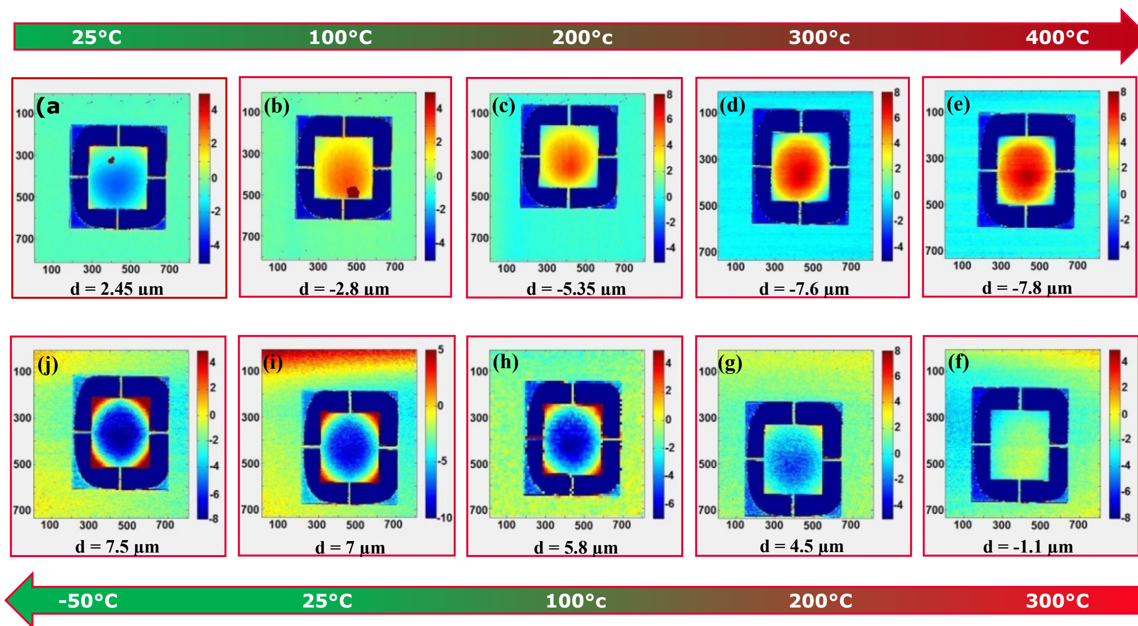

Fig. 5. Optical interferometer micrographs of plus structure with 2µm copper at different temperature. Micrographs show deflection of microstructure changes at given temperature. (d=deflection)

described for copper in the literature. As deflection of curved cantilever is in opposite direction, the hysteresis plot for curved cantilever is in inverted manner in comparison to plus structure. At a fixed end of curved cantilever, due to its special shape, one can induce torsional load instead of tensile or compressive load as in case of plus structure. The area of

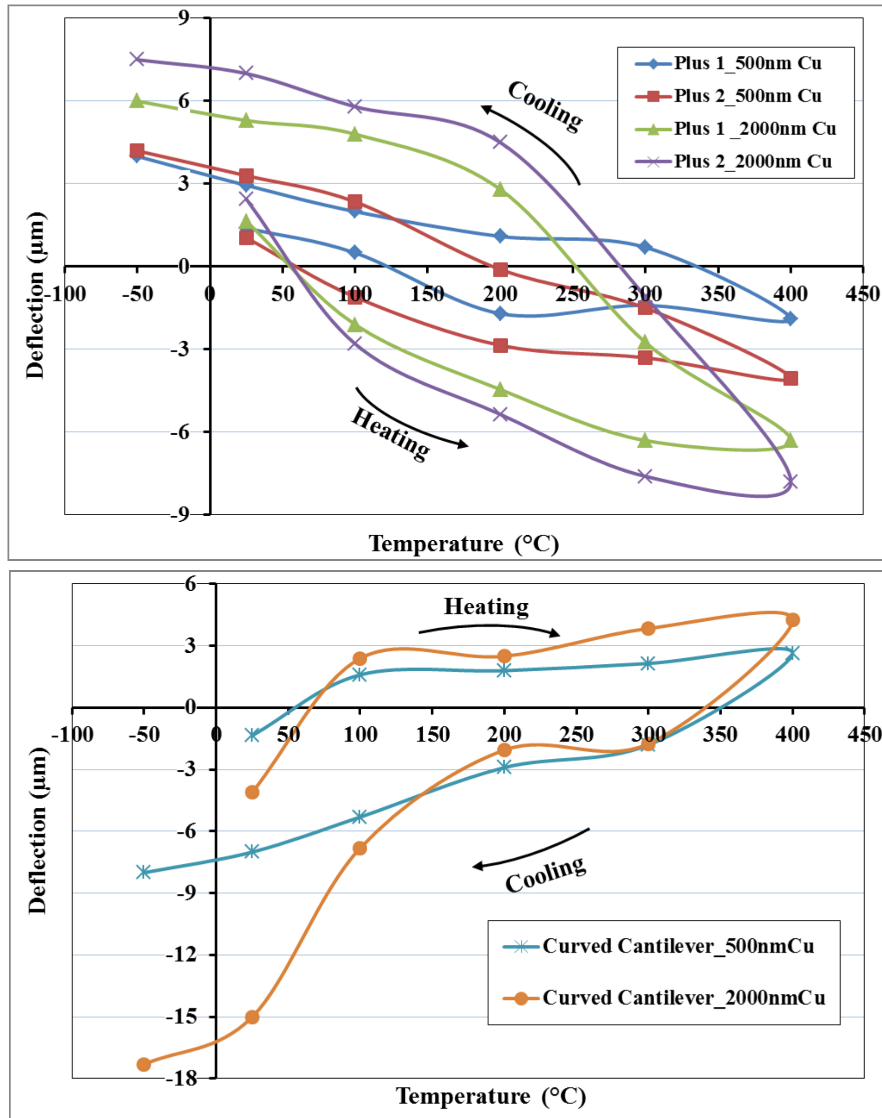

Fig. 6. Hysteresis plot shown for different plus (left) and curved cantilever (right) structures with different copper thicknesses.

hysteresis curve increases with copper thickness as well as with dimensions of the structure. Higher the copper thickness, higher will be the energy loss (energy given to copper to reorient its grains) during the heating-cooling cycle. On a same path, as the plus 2 has higher aspect ratio of four arms supporting the central plate than plus1 structure (see table 1), the deflection will be higher due to higher tensile or compressive force. This again increases the energy loss and thus area of hysteresis curve.

4 Conclusion and future work

A novel method to fabricate different silicon based structures on large scale to analysis thin metal film is demonstrated. With this process, numerous different structures such as theta

structure, plus sign, curved cantilever together beams and cantilevers of different dimensions of different silicon thickness can be fabricated. The process offers ease of deposition and structuring the thin film directly on structures and by this one can analyze various thin films of metal at micron scale. Also, the method offers a high degree of freedom to analyze and understand the behavior of thin metal films under the influence of different environment conditions such as temperature, atmosphere, humidity, mechanical load etc. Using the fabricated structures, behavior of thin copper film is investigated. The investigation gives experimental proof by depicting hysteresis curve of copper using these MEMS structures under thermo-cyclic loading. The study will be continued further to understand the behavior of copper in greater detail and will focus on the degradation of copper under thermal load.

References

1. Nelhiebel, M., et al., *Effective and reliable heat management for power devices exposed to cyclic short overload pulses.* Microelectronics Reliability, 2013. **53**(9): p. 1745-1749.

2. Hille, F., et al., *Reliability aspects of copper metallization and interconnect technology for power devices.* Microelectronics Reliability, 2016. **64**: p. 393-402.

3. Gupta, T., *Copper Interconnect Technology*2008: McGraw-Hill Professional Publishing.

4. Wong, H.Y., N.F. Mohd Shukor, and N. Amin, *Prospective development in diffusion barrier layers for copper metallization in LSI.* Microelectronics Journal, 2007. **38**(6): p. 777-782.

5. Heinz, W., W. Robl, and G. Dehm, *Influence of initial microstructure on thermomechanical fatigue behavior of Cu films on substrates.* Microelectronic Engineering, 2015. **137**: p. 5-10.

6. Mönig, R., R.R. Keller, and C.A. Volkert, *Thermal fatigue testing of thin metal films.* Review of Scientific Instruments, 2004. **75**(11): p. 4997-5004.

7. Lederer, M., et al., *Thermomechanical Stresses in Copper Films at Elevated Temperature.* Journal of Microelectronics and Electronic Packaging, 2010. **7**(2): p. 99-104.

8. Ghidelli, M., et al., *Determination of the elastic moduli and residual stresses of freestanding Au-TiW bilayer thin films by nanoindentation.* Materials & Design, 2016. **106**: p. 436-445.

9. Haque, M.A. and M.T.A. Saif, *Application of MEMS force sensors for in situ mechanical characterization of nano-scale thin films in SEM and TEM.* Sensors and Actuators A: Physical, 2002. **97-98**: p. 239-245.

10. Matoy, K., et al., *A comparative micro-cantilever study of the mechanical behavior of silicon based passivation films.* Thin Solid Films, 2009. **518**(1): p. 247-256.

11. Matoy, K., et al., *Micron-sized fracture experiments on amorphous SiOx films and SiOx/SiNx multi-layers.* Thin Solid Films, 2010. **518**(20): p. 5796-5801.

12. Sasangka, W.A., et al., *Characterization of the Young's modulus, residual stress and fracture strength of Cu–Sn–In thin films using combinatorial deposition and micro-cantilevers.* Journal of Micromechanics and Microengineering, 2015. **25**(3): p. 035023.
13. Zalesak, J., et al., *Cross-sectional structure-property relationship in a graded nanocrystalline Ti1−xAlxN thin film.* Acta Materialia, 2016. **102**: p. 212-219.
14. Koiwa, K., et al., *Investigation of continuous deformation behavior around initial yield point of single crystal copper by using micro scale torsion test.* Scripta Materialia, 2016. **111**: p. 94-97.
15. Motz, C., T. Schöberl, and R. Pippan, *Mechanical properties of micro-sized copper bending beams machined by the focused ion beam technique.* Acta Materialia, 2005. **53**(15): p. 4269-4279.
16. Weihs, T.P., et al., *Mechanical deflection of cantilever microbeams: A new technique for testing the mechanical properties of thin films.* Journal of Materials Research, 1988. **3**(5): p. 931-942.
17. Florando, J.N. and W.D. Nix, *A microbeam bending method for studying stress–strain relations for metal thin films on silicon substrates.* Journal of the Mechanics and Physics of Solids, 2005. **53**(3): p. 619-638.
18. Plappert, M., et al., *Characterization of Ti diffusion in PVD deposited WTi/AlCu metallization on monocrystalline Si by means of secondary ion mass spectroscopy.* Microelectronics Reliability, 2012. **52**(9): p. 1993-1997.
19. Mittereder, T., *Temperature Dependent Die Warpage Measurements up to 400 °C.* 2017.
20. Murarka, S.P., *Multilevel interconnections for ULSI and GSI era.* Materials Science and Engineering: R: Reports, 1997. **19**(3): p. 87-151.
21. Bigl, S., et al., *Film thickness dependent microstructural changes of thick copper metallizations upon thermal fatigue.* Journal of Materials Research, 2017. **32**(11): p. 2022-2034.

Paper B

Fabrication of MEMS based structures for characterization of thin metal films by nanoindentation technique

F. Saghaeian[a,b,*], J. Keckes[b], J. Zechner[c], S. Woehlert[a], K.A. Schreiber[a], H. Pfaff[d], J. Walter[d]

[a] *Infineon Technologies Austria AG, 9500 Villach Austria*
[b] *Department of Materials Physics, Montanuniversitaet Leoben and Erich Schmid Institute for Materials Science, Austrian Academy of Sciences, Leoben, Austria*
[c] *Kompetenzzentrum Automobil-und Industrie-Elektronik GmbH, Europastraße 8, 9524 Villach, Austria*
[d] *Infineon Technologies Germany AG, Wernerwerkstraße 2, 93049 Regensburg, Germany*

IEEE xplore (March 2019)

DOI: 10.1109/EMAP.2018.8660918

Abstract

Micro-Electro-Mechanical systems based structures offer a reliable platform for investigating properties of thin metal film which are strongly influenced by the deposition process as well as post processing conditions during the wafer processing. The present work introduces a methodology to fabricate free standing structures based on silicon on Insulator (SOI) technology, which offers a tool to study material properties of silicon-thin metal interface under different conditions. A variety of micro structures such as straight/curved cantilevers, beams, as well as plus sign and theta specimens of varying dimensions have been fabricated. Different micro structures of silicon having thisckness of 2.8-3µm were deposited with copper films of 1000-3000 nm thicknesses. Among them, cantilevers of different dimensions have been used to study the varying grain size of copper from submicron to micrometer range. By using the nanoindentation technique, the stiffness and modulus of elasticity measurements were carried out for pure silicon cantilevers of varying width and Si-Cu compsite cantilvers of varying copper thicknesses with different grain size. This methodology of fabrication offers flexibility to characterize different kinds of thin films of various dimensions and study the impact of individual process conditions on properties of thin films.

1 Introduction

The microstructure has a vital role in governing the various properties of material and it plays even more crucial role once the material film is deposited as a thin film [1,2]. The microstructure of the thin metal film such as grain size or grain orientation is strongly influenced by thickness of the deposited film as well as by deposition conditions [3,4]. Furthermore, during deposition incorporation of impurities can also influence the properties of film deposited [3,5]. Various thin films exhibits change in fracture strength, hardness, reflectivity or absorption, residual stress by change in their deposition conditions or due to microstructural changes [3-6]. The same phenomenon is exploited in semiconductor industries enormously, where by merely tuning the process desirable properties of thin films are derived. Among different materials such as oxides, nitrides, carbon layers etc., various metal films are used in the semiconductor industry to improve the performance of semiconductor devices. Copper metallization is one classical example in which deposition process is changed as per need to influence properties of copper film deposited [3,5].

In addition to it, various other parameters such as type of substrate, topography and post processing conditions affects the performance of copper film. Therefore, there is a need of well-established platform for the characterization of thin films from their material point of view. For this purpose, micro-electro-mechanical system based structures are right tool [7,8].

Micro-Electro-Mechanical systems based structures are capable of offering defined state of loading thin films to evaluate their material properties. In order to do so, one has to have right choice of structure which can vary from application point of view [7-9]. The study reported here put forth a platform for the fabrication of various free standing structures of different size and form. In addition to it, properties of thin copper films were studied using nanoindentation technique

2 Experimental

The fabrication of relevant structures is carried out using Silicon on insulator (SOI) technology. For this purpose, 200mm diameter SOI wafers consisting of 5µm top active layer, 1µm thick thermal box oxide and 725µm substrate was used. The substrate is with (100) orientation. Dry etching of silicon was carried out with reactive-ion plasma etching technique. A thick TEOS based thermal oxide was deposited using plasma assisted CVD technique. Chemical mechanical polishing (CMP) was carried out to remove the additional

oxide. Metal was deposited at constant deposition rate of 1-2nm/sec. Thin layer of 50nm thick TiW metal barrier was deposited on structures prior to copper deposition. Copper deposition was carried out in a way free standing structures were not mechanically damaged by deposition process.

Nano-indentation was carried out on Nano indenter G200 tool using 40nm indenter tip. Samples were fixed on the sample holder using adhesive glue. Indentation has been carried out by applying maximum displacement of 100µm and load on surface was increased linearly until cantilever has been fractured. The touch down of indenter tip was at distance of 5µm from the tip of cantilever. Every measurement was repeated for 5 times on pristine

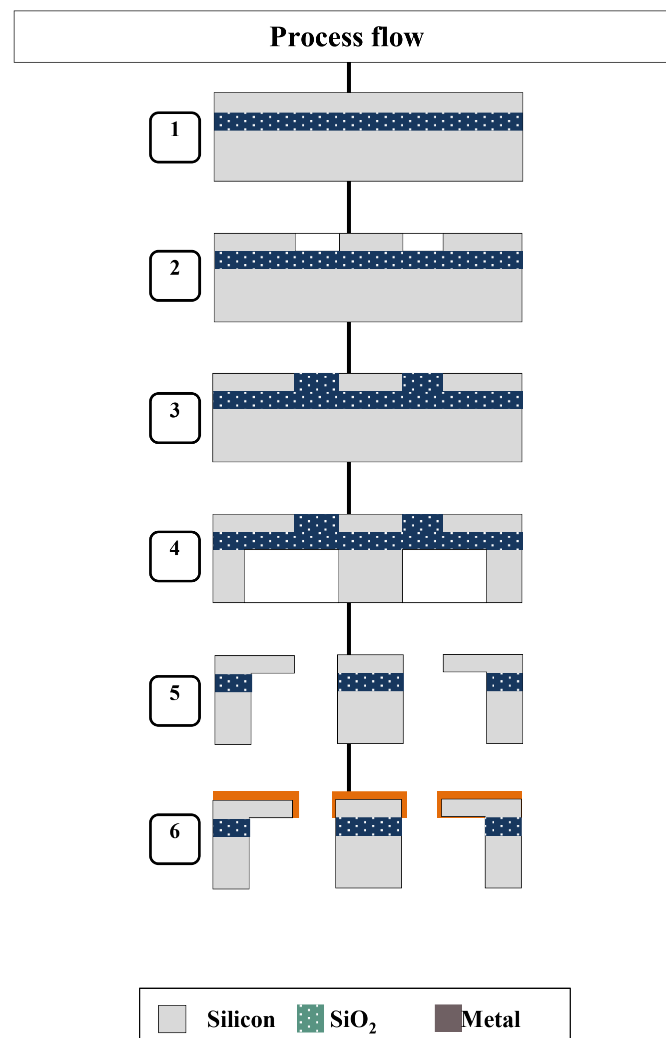

Fig. 1 Schematics showing various steps of fabrication. 1) SOI wafer 2) Front side etch 3) Oxide fill and CMP 4) Backside cavity etch 5) Oxide release etch 6) Metal deposition

cantilevers and average value of load was taken for the calculation. For calculation purpose, metal deposition on the side wall of the cantilever was ignored.

3 Results and discussion

3.1 Fabrication of Micro-Electro-Mechanical systems structures

The fabrication process starts with the formation of alignment marks on the wafer for optical lithography. These process steps remove more than 2µm of top silicon leaving behind 2.8-3µm as final thickness of silicon for structures across the wafer. A brief summary of the complete process flow is as shown in figure 1. Thereafter, using optical lithography and plasma assisted dry etch of silicon, various kinds of structures were etched on wafer front side. These structures include various kinds of cantilevers, bridges, theta shaped structures, plus structures and curved cantilevers. Few exemplary SEM images of fully fabricated structures are as shown in figure 2a-c. After successful front side etching, large cavities will be etched on the wafer backside using same process of dry etch of silicon. However, for backside etching, the front side topography was high. In order to ease the topography, front side cavities were filled using PECVD filler oxide followed by a chemical mechanical polishing to remove additional oxide from wafer surface. This helped to reduce

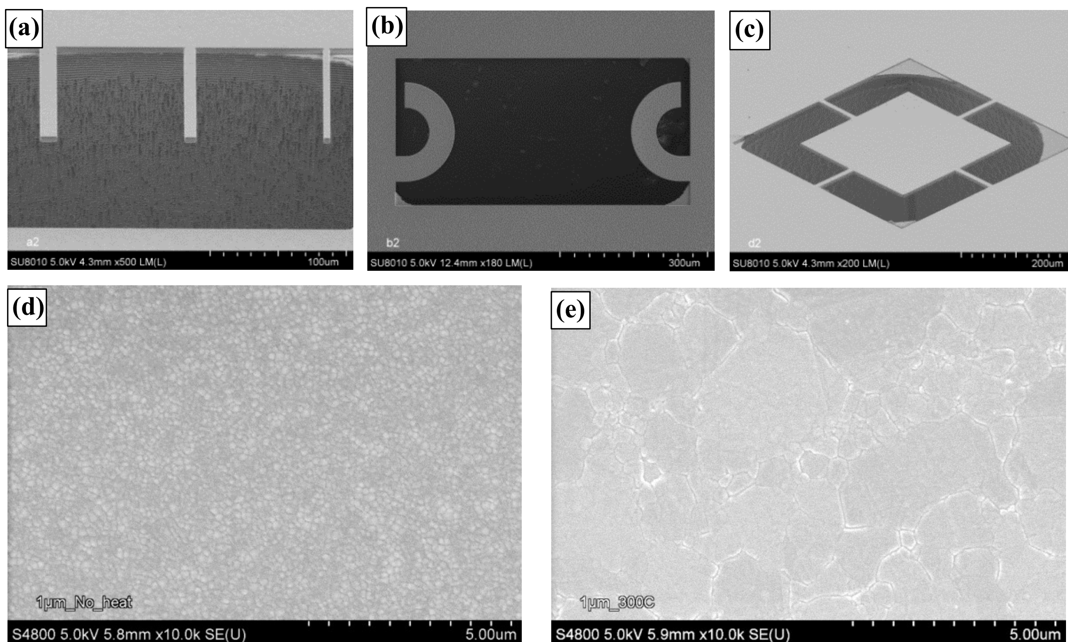

Fig. 2 SEM Micrographs of different structures fabricated (a) Cantilevers, (b) curved cantilever & (C) plus structure and grain (d) Cu as deposited & (e) after annealing at 300°C

the topography drastically. Furthermore, wafer was thinned down to 400µm thickness and with the help of optical lithography aligned to front side; cavities of prerequisite dimensions were etched. Subsequently, the filler oxide and box oxide were etched away to form free standing structures of varying dimensions as shown in figure 2. In a final step, metal deposition was carried out. At first 50nm TiW was deposited as diffusion barrier is needed to avoid reaction between silicon and copper [1] followed by copper in range of 1 to 3µm thickness on various wafers. Wafer was then broken carefully in smaller pieces to carry out the structural tests to evaluate material properties of silicon-copper composite structures

3.2 Nano-indentation of Si-Cu cantilevers

Cantilevers have varying width of 5, 8, and 12µm but of same length of 100µm. They were deposited with Cu thickness of 1, 2 and 3µm. As copper was deposited with a low energy process, columnar nano-crystalline film of Cu was grown on cantilevers and no significant change was observed in grain size with increasing thickness [6]. These Cu deposited cantilevers together with pure Si cantilever were tested using nanoindentation tool. The figure 3 shows nanoindentation plots of various Si and Si-Cu cantilevers for three different widths. As width of the cantilever is increasing the load to fracture is also increasing. Based on fracture load, the stiffness and modulus of elasticity were calculated for pure silicon cantilever. As SOI wafers have (100) orientation, applied force is acting along the plane perpendicular to wafer surface or cantilever length, which would be then (110) plane. For 8 and 12µm Si cantilever Young's modulus was calculated as per equation (1) (where S is stiffness, L is bending length, b is width and h is height of cantilever). The values were 161.5 and 177 GPa respectively which is matching with the literature value of 169GPa [10]. For 5µm width cantilever, the measurement values were below resolution limit of the tool and thus not calculated.

$$Young's\ Modulus\ (E) = \frac{4SL^3}{bh^3} \qquad (1)$$

As a next step, the Si-Cu composite cantilever structures were studied. As expected, the load to fracture has increased with thickness of copper. SEM micrographs of selected Si-Cu cantilever after fracture are as shown in figure 3. The cantilever was found to be broken right at its junction point and Cu film was pulled along fracture direction due to plastic deformation. The values for the fracture load for different Cu thickness of cantilever are summarized in table I.

Width of cantilever	Silicon	Thickness of Cu on cantilever		
		1µm	2µm	3µm
12µm	0.71	1.4	1.9	3.0
8µm	0.36	1	1.5	1.8
5µm	NA	0.3	1.1	1

Table I. Fracture load (mN) for different Cu thicknesses

In addition, cantilevers with 1µm Cu and annealed at different temperatures were investigated. It is observed that the load required for fracture of Si-Cu cantilever decreased significantly right after annealing at 100°C (see table II). The fracture load tends to rise with further annealing to 200 and 300°C. Upon annealing the sample, Cu film deposited on the structure tends to reorient itself to form bigger grain (see fig 2d & 2e). As nanocrystalline grains were grown to micron size, the fracture load and stiffness of the composite Si-Cu beam decreased. The young's modulus calculation for copper demands complex data analysis that can take into account the metal deposited on the side wall and TiW barrier layer present between the silicon and copper layer. This work is currently out of focus and will be explained elsewhere.

Width of cantilever	Silicon	Thickness of Cu on cantilever			
		RT	100°C	200°C	300°C
12µm	0.71	1.4	0.85	0.97	1.05
8µm	0.36	1	0.62	0.61	0.77
5µm	NA	0.3	0.22	0.25	0.36

Table II. Fracture load (mN) of annealed Si-Cu cantilever

4 Summary and conclusion

The current work demonstrates a platform for manufacturing various Micro-Electro-Mechanical systems structures to characterize thin metal films. The method offers ease of manufacturing such structures on large scale and the method is applicable to study various

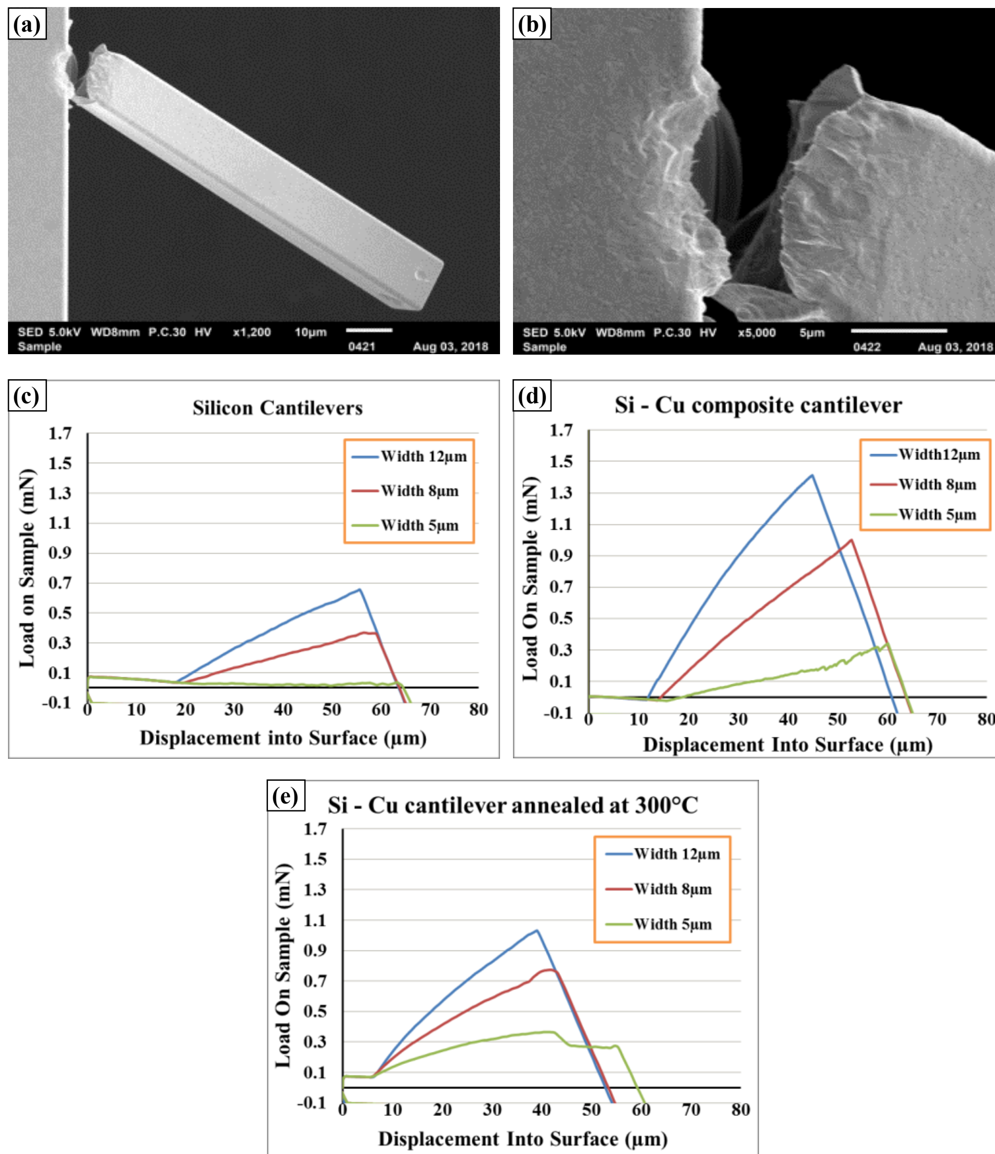

Fig. 3 (a & b) SEM micrographs of indented Si-Cu cantilever and plots for stiffness analysis of (c) silicon cantilever, (d) Si - 1µm Cu & (e) Si - 1µmCu after annealing at 300°C.

material properties of thin films. Using the cantilever structures, primary investigations on silicon structures as well as Si-Cu composite structures were carried out. Modulus of elasticity for silicon cantilevers is matching well with literature values. For Si-Cu composite cantilevers fracture load and thus stiffness found to be decreasing with increase in grain size of copper. With nanoindentation studies, grain growth of Cu has been studied and similarly, phase change or phase formation studies can be carried out.

References

1. Gupta, T., *Copper Interconnect Technology*2008: McGraw-Hill Professional Publishing, Diffusion and Diffusion barriers, DOI 10.1007/978-1-4419-0076-0_3.
2. Ghidelli, M., et al., *Determination of the elastic moduli and residual stresses of freestanding Au-TiW bilayer thin films by nanoindentation.* Materials & Design, 2016. **106**: p. 436-445.
3. Gupta, T., Copper Interconnect Technology2008: McGraw-Hill Professional Publishing, Deposition Technologies of Materials for Cu-Interconnects, , DOI 10.1007/978-1-4419-0076-0_5.
4. Thornton, J.A., *The microstructure of sputter-deposited coatings.* Journal of Vacuum Science & Technology A, 1986. **4**(6): p. 3059-3065.
5. Shacham-Diamand, Y., et al., *Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications*2009: Springer-Verlag New York.
6. Craig, S. and G.L. Harding, *Effects of argon pressure and substrate temperature on the structure and properties of sputtered copper films.* Journal of Vacuum Science and Technology, 1981. **19**(2): p. 205-215.
7. Matoy, K., et al., *A comparative micro-cantilever study of the mechanical behavior of silicon based passivation films.* Thin Solid Films, 2009. **518**(1): p. 247-256.
8. Sasangka, W.A., et al., *Characterization of the Young's modulus, residual stress and fracture strength of Cu–Sn–In thin films using combinatorial deposition and micro-cantilevers.* Journal of Micromechanics and Microengineering, 2015. **25**(3): p. 035023.
9. Florando, J.N. and W.D. Nix, *A microbeam bending method for studying stress–strain relations for metal thin films on silicon substrates.* Journal of the Mechanics and Physics of Solids, 2005. **53**(3): p. 619-638.
10. Jiang, L. and R. Cheung, *A review of silicon carbide development in MEMS applications.* International Journal of Computational Materials Science and Surface Engineering, 2009. **2**(3-4): p. 227-242.

Paper C

Investigation of high cyclic fatigue behaviour of thin copper films using MEMS structure

F. Saghaeian[a,b,*], M. Lederer[c], A. Hofer[a], J. Todt[b], J. Keckes[b], G. Khatibi[c]

[a] *Infineon Technologies Austia AG, 9500 Villach Austria*

[b] *Department of Materials Physics, Montanuniversitaet Leoben and Erich Schmid Institute for Materials Science, Austrian Academy of Sciences, Leoben, Austria*

[c] *Vienna University of Technology, Getreidemarkt 9, A-1060 Vienna, Austria*

International Journal of Fatigue, Volumes 128, 2019, 105179

https://doi.org/10.1016/j.ijfatigue.2019.06.039

Abstract

Fatigue failure of thin metal films used in semiconductor devices poses a serious problem for their structural integrity over the lifetime. In present study, specially designed MEMS based plus structures are fabricated and used to investigate fatigue behavior of thin copper film under cyclic mechanical load. FEM Analysis was employed to assess stress distributions under vibration loading. Under cyclic mechanical loading, plus structures reveal cyclic plastic deformation, together with grain coarsening and change in crystal orientation at the location of stress concentration predicted in simulation. It was found that a reduction in thickness enhances the fatigue resistance of copper films.

1 Introduction

Metal-oxide-semiconductor field effect transistors deploy various metals such as aluminum, copper, gold, tungsten, tantalum, titanium etc. for increasing current conducting efficiency, reducing thermal budget or to curtail power losses [1-3]. Among them, few selected metals are used for forming a low ohmic contact to semiconductors; some of them are used for the metal barriers or via contact metals while major application is for good electrical contact to macro-world and to thermally cool the device efficiently [3-6]. Metals such as aluminum, copper or gold are used as heat capacitors allowing the semiconductor device to work at higher power densities without having overshoot of their temperature limit [1,4-7]. Among them copper outperform aluminum in terms of its thermal conductivity, electrical conductivity, coefficient of thermal expansion (CTE), as well as better mechanical properties [1,3,8].However, due to higher modulus of elasticity, copper thin films impose higher film stress on the substrate compared to aluminum based metallization [1,6,8]. Furthermore, even though CTE of copper is lower than aluminum, it is still about 6 times higher than that of silicon substrate [1,8]. Under high thermal budget, buildup of large intrinsic stresses in thin copper films result in development of high thermo-mechanical loads at Cu/Si interface [1,6,9]. This load increases with increase in the copper thickness and decrease in the final silicon thickness supporting the copper. This situation leads to very high interfacial stresses between silicon and copper. In addition, under severe operating conditions, due to sudden heating and cooling, the interface with higher metal thickness will be subjected to severe mechanical loads, simulating fatigue like situation [6]. Thus, it is matter of immense importance to characterize this interface for its robustness against fatigue loading.

There are several studies available characterizing thin metal films under thermal and mechanical fatigue loading for various applications. Thin films of aluminum, copper or silver were subjected to mechanical fatigue loading by using compliant or rigid substrates [10-15]. Elastic waves generated by utilizing surface acoustic wave (SAW) devices, were used to study the fatigue response of Al thin film under cyclic mechanical stresses [10-11]. By using elastic waves, metal thin films subjected to fatigue loading with ultrahigh frequencies, revealed various new types of defects together with typical defects such as hillock, dendrite or voids. In a similar study, silicon dioxide cantilevers were employed to measure the fatigue behavior of silver thin film [12]. Change in stiffness of composite beam of Ag and SiO2 was taken as indication for the induced damage in silver film by cyclic loading. Eve et. al. adopted the PMMA film as substrate for loading the thin metal films

with equiaxial stress to mimic thermal loading conditions [13]. The test setup can be used to monitor the sample in-situ with optical detection system. However, adhesion of metals on PMMA was enhanced by deposition of chromium layer altering test conditions from real time situation. Wimmer et. al. studied various material properties of copper such as Young's modulus, ultimate tensile strength etc. in correlation with its grain size using a free standing copper structure [14]. However, most of the studies were concentrated on the fatigue behavior of the metal thin film and influences of the substrate and its interface energy were ignored. This makes the comparison of available results quite cumbersome as properties of thin metal film are strongly driven by its microstructure which is ultimately influenced by the deposition process and the type of substrate used [2,5,8].Finally, by changing deposition process not only grain size but also grain orientation of metal can be changed [1,2]. However, choice of process used for the deposition of copper film is mainly driven by the intended application [1-3].

The above brief review reveals that fatigue behavior of thin films on rigid substrates has been subject of extensive studies. However, the trend of reducing dimensions in advanced microelectronics to improve the functionality leads towards production of devices having final wafer thicknesses in range of tens of micrometers. This creates enormous impact on thermomechanical behavior of metallization stack [16,17]. Thus in order to study the impact of substrate thickness on the behavior of metallization layers, specially designed Micro-Electro-Mechanical Systems (MEMS) based plus structures have been developed. Contrary to the available experimental techniques proposed for fatigue testing of thin films, in this study the Si-substrate and the Cu film are in the same thickness range of few microns. Due to the high flexibility of these structures, the deposited metallization layers can be subjected to high bending stresses without inducing fracture in the Si-substrate. Moreover, by changing the thickness ratio of substrate to metallization, amount of mechanical stress induced at the interface can be varied. By application of the proposed methodology, a better insight into the fatigue mechanisms of thin films on ultrathin substrates can be gained. The fabrication process chosen here offers a great degree of freedom to tune the thickness of substrate or that of the film easily. In this work, the functionality of the designed structures has been assessed based on experimental investigation of the fatigue behavior of copper films in combination with finite element method (FEM) simulation. Thereby, FEM simulations were performed to analyze the vibration response of the MEMs structures and to determine the stress distribution in the materials.

2 Experimental

1.1 Fabrication of plus structures

The fabrication of the plus structure was carried out based on silicon on insulator (SOI) technology. SOI wafers with standard thickness of 725µm having 5±0.5µm top silicon and 1µm thick buried oxide were used for this fabrication. In order to develop alignment marks on wafer, ~2µm of top silicon was consumed and 3±0.5µm thickness was available for device fabrication. Plus structures were etched using deep reactive ion etching technique on wafer front side. Thereafter, in order to ease the wafer handling in post processing steps, silicon dioxide was filled in cavities between these structures by using plasma assisted chemical vapor deposition technique and the grown oxide topography was planarized using chemical mechanical polishing. As a next step, wafer thickness was reduced to 400µm final thickness from wafer backside and cavities were etched on this polished surface with perfect alignment to structures on front side of the wafer. Finally, oxide (filled and box oxide) was etched away to get freestanding structures using buffered oxide etch solution of hydrofluoric acid. Four different plus shaped structures were fabricated with same dimensions of central load plate and varying dimensions of the arms/beams. The plus shaped structure was designed to load a stack of thin metal film and substrate with high cyclic load. The central plate of such a freestanding structure undergoes cyclic vibration under mechanical or thermomechanical load. Dimensions of central plate were kept in sub millimeter range to facilitate the detection of plate displacement using laser Doppler vibrometer. Furthermore, due to its unique shape, it induces a very concentrated load at either ends of the beam. It is explained in simulation part in greater detail. Finally, copper film was deposited using DC sputtering technique at rate of 1 to 3nm/sec and deposition pressure of 2-4×10-6 mbar. Prior to deposition of copper, a thin 50nm TiW film was deposited to avoid any kind of reaction between silicon and copper film. TiW deposition rate was 1 to 2nm/sec. The final thickness of silicon in the freestanding structures is in the range of 3 +/- 0.5µm while copper thickness was varied from 1 to 3µm.The sputtering process parameters were optimized to obtain a nano-crystalline Cu film and to avoid damaging the MEMS structures. The scanning electron microscope (SEM) micrographs of Cu deposited plus structures of varying sizes are as shown in fig. 1 and their dimensions are given in Table 1. Fig. 1.e&f show the nano-crystalline columnar microstructure of Cu film which display an average grain size of ~100-300 nm and a dominant 111 texture (shown in forth coming images).More details on fabrication of the plus structures are explained elsewhere [18].

Type of structure	**Dimensions of beam structure (µm)**		
	Length	**Width**	**Aspect ratio**
Plus 1	**50**	**10**	**5**
Plus 2	**100**	**10**	**10**
Plus 3	**200**	**24**	**8.3**
Plus 4	**400**	**24**	**16.6**

Table 1. Showing dimensions and aspect ratio of supporting beam

1.2 Mechanical loading of plus structure:

The plus structures were loaded mechanically using a piezoelectric shaker manufactured by isi-sys and coupled with an Agilent 33220A signal generator. In order to measure the amplitude of vibration, a laser Doppler vibrometer of Polytec CLV 1000 make, was utilized. In current experiment, the vibrational sweep was carried out between 10 to 90 kHz with a sweep interval of 4s and an excitation voltage of 6V. The sample was fixed on the sample holder using acrylic glue.

3 Results and discussion

3.1 FEM Simulations

FEM simulations were conducted for preparation and interpretation of vibration experiments. For this purpose, four above mentioned plus structures of different dimensions or aspect ratios were studied (see Table 1). In order to introduce highest stress in the copper film, it is necessary to vibrate the plus structure at frequencies close to resonance. Therefore, modal analyses were carried out using ANSYS 19 software to determine the resonance frequencies for the different plus structures (see Table 2). Based on this data, for current experiments, plus 3 and plus 4 structures were chosen as their resonance frequencies were lower and within the range of current experimental setup compared to that of plus 1 and plus 2 structures and thus suitable for present study. The mode shapes related to the resonant frequencies are depicted in fig. 2a-d. It was concluded that the first resonant frequencies are

of major relevance for the vibration experiments, because the correlated mode shapes show displacements perpendicular to plus structure while for higher frequencies, displacement was asymmetric. Furthermore, harmonic simulations were performed where the periodic accelerations of the piezo shaker were applied as boundary conditions. These simulations

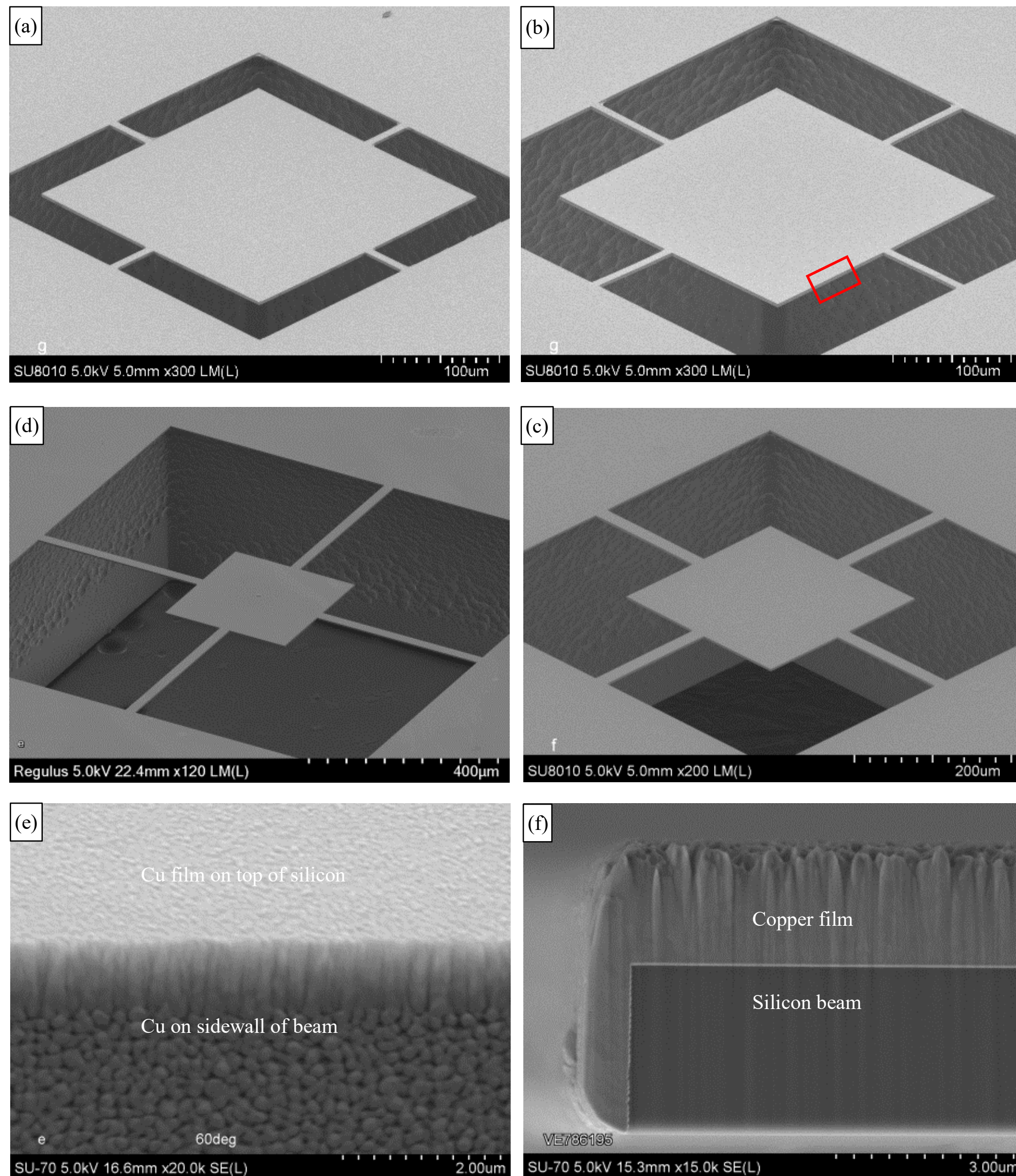

Fig. 1. various sizes of MEMS plus structures fabricated using SOI Technology. (a) Plus 1 (b) plus 2 (c) Plus 3 (d) Plus 4, (e) SEM micrographs showing columnar grain of as deposited copper film on edge of silicon substrate (marked with red box in fig. 1.b). (f) Showing FIB cross-section of one of four beams after Cu deposition. The average grain size of copper was 100-300nm.

were used to evaluate the stress fields in the copper films, whereby measured vibration amplitudes were fitted in the simulation. Corresponding to the experimental procedure, the simulations were done either for a specific frequency or for a sweep, where the frequency was varied within a predefined frequency range. The maxima of amplitudes occur at the

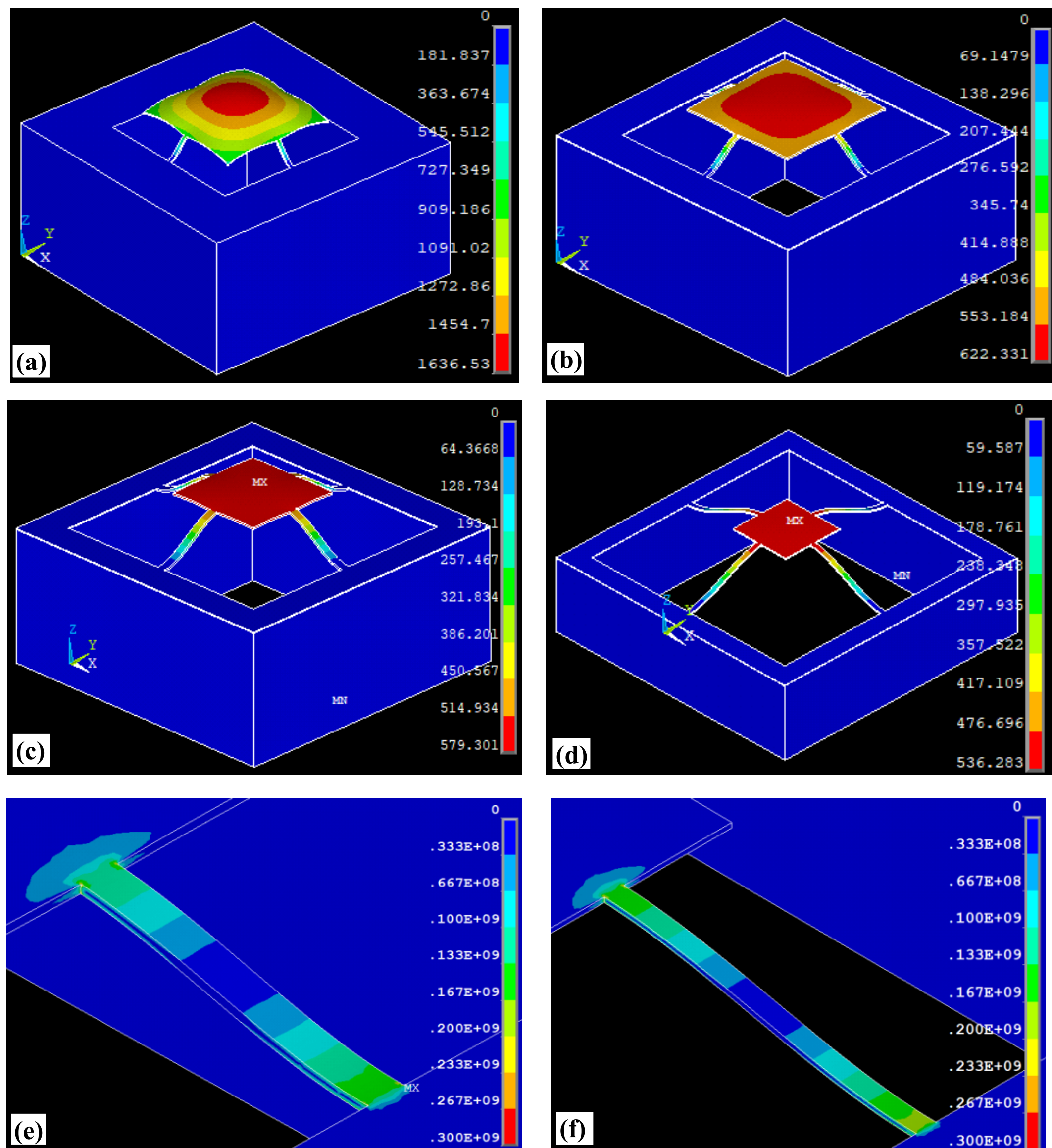

Fig. 2. (a to d) Modal analyses: Displacement plots (displacement vector sum) showing mode shapes [arbitrary units] of four different plus shaped structures deposited with 3µm copper at first resonance frequency (e & f) Harmonic analyses: Plots of the von Mises stress [Pa] for plus 3 and plus 4 structures near to the first resonant frequency.

resonant frequencies. A plot of relative displacement amplitude versus vibration frequency is depicted in figure 3.

The relative displacement was defined as the difference between displacements of membrane and frame. The ratio of displacements observed by comparison of membrane and frame derived through simulation matched with corresponding values observed in the experiments. Since the harmonic analysis may be considered as linear method, one may calibrate the amplitudes assumed in the simulation on the basis of measurements performed in the frequency range well below resonance. However, in the vicinity of the resonant frequency the deformation of the structure increases until plastic deformation occurs in the copper. This behavior was considered as root cause of material damping assumed in the harmonic analysis. The coefficient of material damping used in the simulation was fitted to match the peak values of vibration amplitudes observed in the experiments. Thereby, it was possible to evaluate the stresses arising in the materials, when the vibration is close to resonance. The simulation revealed that the location of stress maxima is at either ends of the beam supporting the central plate (see fig. 2.e&f). It means the maximum of mechanical load was supposed to be exerted at these junction points and the copper shall be subjected to the fatigue loading at these locations. Furthermore, simulation has revealed that by reducing copper thickness (from 3 to 1µm) the resonant frequencies decrease by amount of 26-27%. This is not very unexpected, as due to decrease in net thickness of the structure, resonance frequency tends to fall down.

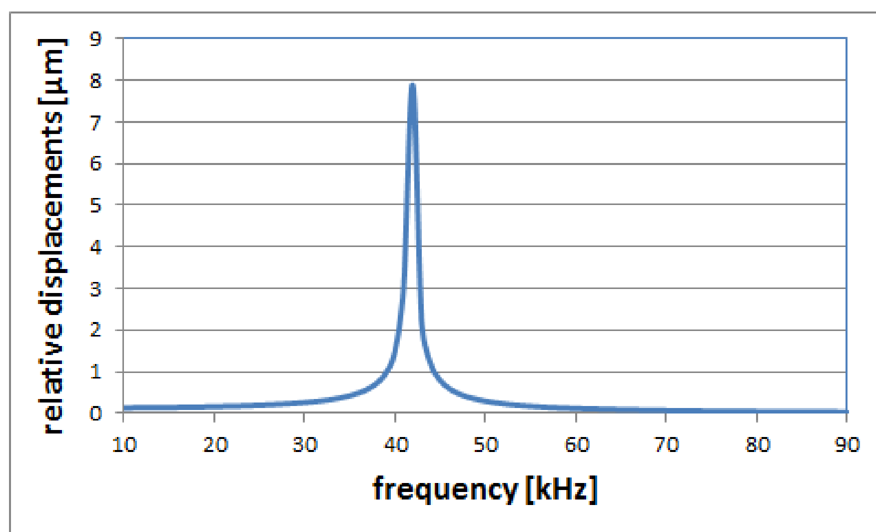

Fig. 3 Plot of membrane displacements [µm] relative to frame in dependence of frequency for the plus 3 structure with 3 µm thick copper film.

As stated above, the thickness of membrane can vary in range 3+/-0.5µm and variation of such a magnitude can cause shift of resonant frequencies. Thus, a plausible thickness value of 3.13 µm was adopted in order to obtain accordance between the theoretical results of modal analyses and experimental values.

Resonant frequency	Plus 1 3 µm Cu	Plus 2 3 µm Cu	Plus 3 3 µm Cu	Plus 4 3 µm Cu
1st	**149244 Hz**	**74090 Hz**	**41584 Hz**	**15607 Hz**
2nd	**205763 Hz**	**122225 Hz**	**88950 Hz**	**45878 Hz**

Table 2. Resonant frequencies of plus structures with 3.13 µm Si thickness and 3 µm copper deposition

3.2 Vibrational loading

Fast sweep excitation method was used to load a plus 3 MEMS structure deposited with 3µm Cu film on piezo shaker to evaluate the behavior of thin copper film under mechanical loading. The frequency range of 10 to 90 kHz was chosen for plus 3 as it covers the first and second mode of simulated resonant frequencies. The peak amplitude for this frequency range was recorded as 7.5µm. This validates the simulation model and analysis carried out based on it. For the same plus 3 structure at a constant frequency of 40 kHz, the amplitude was 1.5µm, which is about 5 times smaller. After an initial loading of 30 min in sweep mode, deformation was detected in copper film under fatigue loading. Thereafter, the frequency range of sweep was narrowed in a systematic manner to vibrate the structure at a particular frequency close to the first resonance frequency as per simulation. The frequency was fine-tuned by measuring the maximum amplitude of vibration using laser Doppler vibrometer. A pristine plus 3 sample was subjected to the sweep frequency range from 30 to 60 kHz. In this case a lower degree of plastic deformation was observed after 30min of cycling and the required time for the sample to obtain the same amount of deformation similar to the first experiment was 8 times longer (240 min). It is thus concluded that, loading at a constant frequency of vibration or a narrow range of sweep, do not result in sufficiently high cyclic stresses to induce fatigue in the copper film. The similar observation was reported in earlier work where sweep was found to be the more efficient mode to induce fatigue failure in silicon micro-cantilevers [19,20]. Thus, to ensure the maximum stress in copper film, the

forthcoming experiments were conducted in sweep mode of operation in above mentioned frequency range.

The time dependent evolution of plastic deformation and formation of slip bands at the surface of Cu film for three different plus 3 structures which were loaded for 30min, 60min and 1 hr. 45min are presented in fig. 4.a,b,c respectively. All experiments showed that the deformation observed in copper film was strongly concentrated in a small region at the either ends of four supporting beams while the remaining area was completely unaffected. This corroborates the outcome of ANSYS simulation, which shows maximum stress was exerted at either ends of the beams during the operation. Apart from sharp corners or edges, the maximal amount of stress in copper films was found at either ends of beams, and it was in the range of 150-200 MPa. Even higher values of stress occur at sharp edges of the structure due to the notch effect. Those stress intensities play a major role in crack initiation, but their volume portion is extremely small. Here, it should also be mentioned that stress values in the elastically anisotropic silicon were somewhat higher than in copper due to the higher elastic constants of this material. However, the main focus of the present study was set on metal fatigue behavior in the copper film. Fig. 4.a shows that at the earlier stages of fatigue loading, slip bands were formed at the intersection of the beam and the central plate resulting in initiation of the fatigue cracks in this area. With increasing the loading cycles, the extent of the surface deformation and roughness increased covering a large portion of the connection area of the beams and the plate. The cracks have grown mostly inwards along the extrusions, which were formed in patches with an inclined angle of about 45° with respect to the axis of the beams (fig. 4.b). Figure 4.c reveals that at this region, even after long time of cycling, still there were areas in which the original nanostructured Cu film was maintained undeformed. In this case, the experiment was stopped at 1hr 45min due to breakage of one connecting beam of structure to substrate because of the extreme load (fig. 4.d). A similar deformation behavior was also observed for plus 4 structure, which were subjected to sweep loading in the range of 5 to 20 kHz for 1 hr. (fig. 4.e). On the other hand, if the copper thickness was reduced from 3µm to 1µm, number of required cycles to induce the fatigue in thin copper increased drastically. An increased in fatigue resistance in thin films of 1µm and thinner was also observed by other investigators [21,22] and was found to be related to the suppression of the formation of characteristic fatigue substructures observed in bulk metals due to the dimensional constraint. In our investigations, the early fatigue was seen after 3 hrs. of loading which is about 6times higher than for 3µm Cu thickness. An exemplary image of fatigue on plus 3

structure with 1µm Cu after 5 hours showing similar features as in 3µm Cu films is presented in fig. 4.f.

As time to failure decreases with plus 4 structure, it indicates that plus 4 structure induces higher rate of mechanical damage in copper film than plus 3. Indeed, the stress level shown in fig. 2.f is somewhat higher than that of fig. 2.e. It means, simply by varying the dimension of the structure, the load applied on the metal thin film can be varied. With change

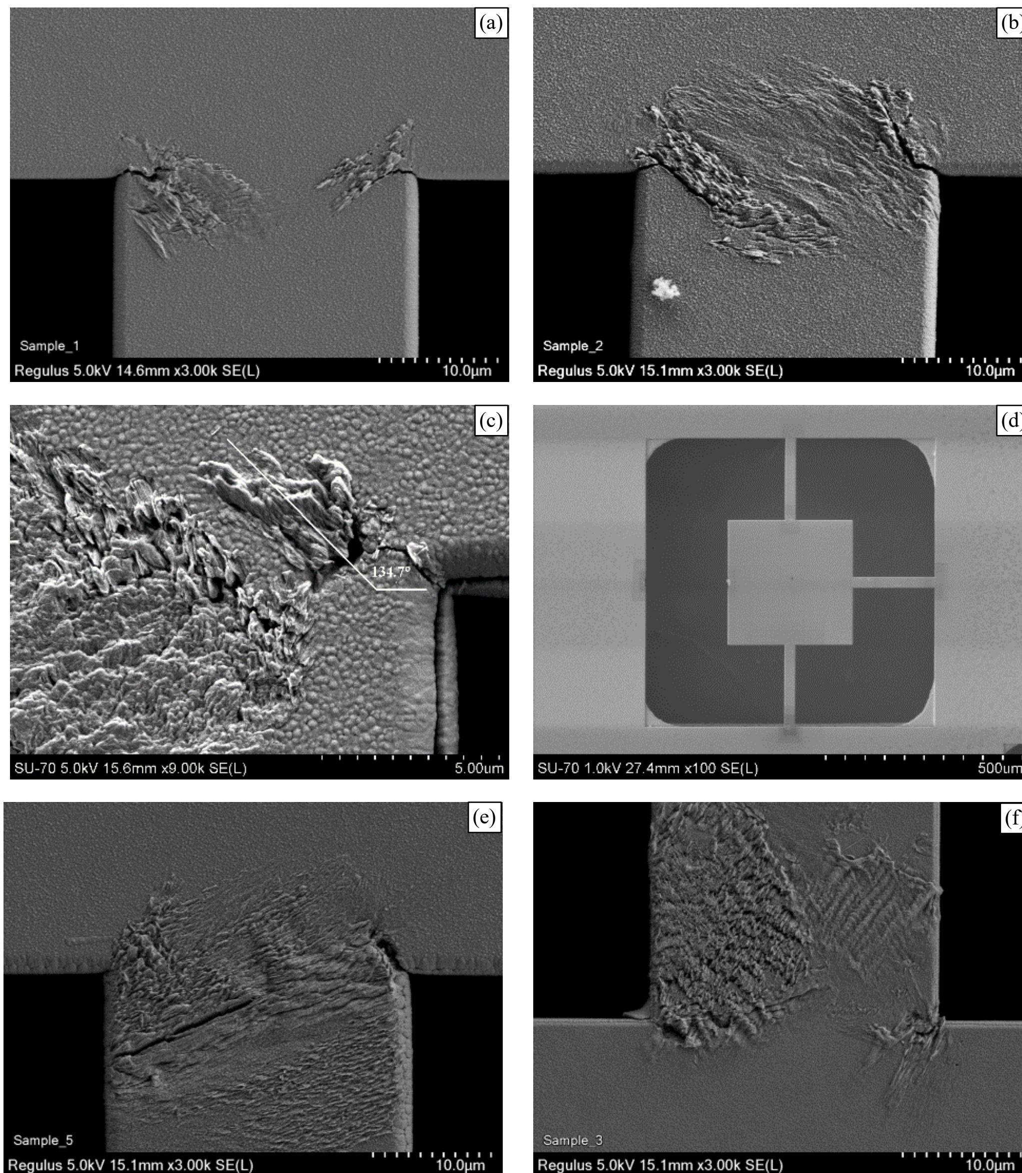

Fig. 4 SEM micrographs of plus 3 structure after mechanical loading for (a) 30min, (b) 60min, (c & d) after 1hr 45 min. (d) one of four beam is broken. (e) Plus 4 after 60 min loading & (f) Plus 3 with 1 µm Cu after 5 hrs. loading.

in dimensions, resonance frequency of structure also changes and as structure shows maximum displacement (amplitude of vibration) at its resonance frequency, only at this frequency the cyclic load is high enough to cause plastic deformation in copper. Thus if arrays of structures with different dimensions are excited in a sweep mode, metal film on these structures will be subjected to different extent of cyclic load. With this methodology, a large data set about load against withstood number of cycles can be generated within short period. Structures of varying dimensions can be fabricated in block format using the fabricated technique developed here. In simulations, it was observed that the thickness of silicon has a major influence on the resonance frequency of a given structure. In consequence, the thickness of the substrate also has a strong influence on the stress distribution and on the lifetime of the samples. However, this should not affect the intrinsic fatigue mechanisms of the copper film. On the other hand, it is worth to mention that, by changing the interface energy by introducing different materials (such as silicon dioxide or silicon nitride etc.) one can influence the material properties of metal film and thereby intrinsic fatigue behavior.

Fig. 4.a-d showed that the initial nano-crystalline grain size of the copper film underwent a large amount of plastic deformation under fatigue loading along with a strong formation of slip lines. During initial loading, slip lines were detected along a direction approximately of 45° to the edge of the structure. It is well known that during the fatigue loading of polycrystalline copper, slip markings form along the most favorably oriented crystals with an angle of ~ 45° between the load axis and the slip direction [23]. With prolonged loading, directions of slip lines were no more ordered along 45°, indicating that other slip systems were activated. In order to investigate the extent of deformation and possible grain growth, further analysis was carried out on the sample, which was subjected to 1hr 45min loading utilizing focused ion beam (FIB) and electron backscatter diffraction (EBSD). FIB was executed on one of the beams at junction point to the substrate (fig. 5.a&b). The cross-sectional FIB micrograph revealed a strong grain growth in the deformed area and the formation of several cracks in the copper thin film but not in the silicon substrate. The nano-crystalline microstructure of the copper has grown, forming micron sized grains under the fatigue loading. The average grain size measured in the loaded area was about 2µm in size. This is however true only for areas of maximum stress concentration, while in other areas, copper retained its morphology in as deposited conditions. Two such a distinctive grain morphologies can be seen aside each other in fig. 5.b. Furthermore, in loaded area, multiple cracks and extrusions were clearly visible (see fig. 5.b). The crack not only has propagated through the copper film preferentially along the grain boundaries

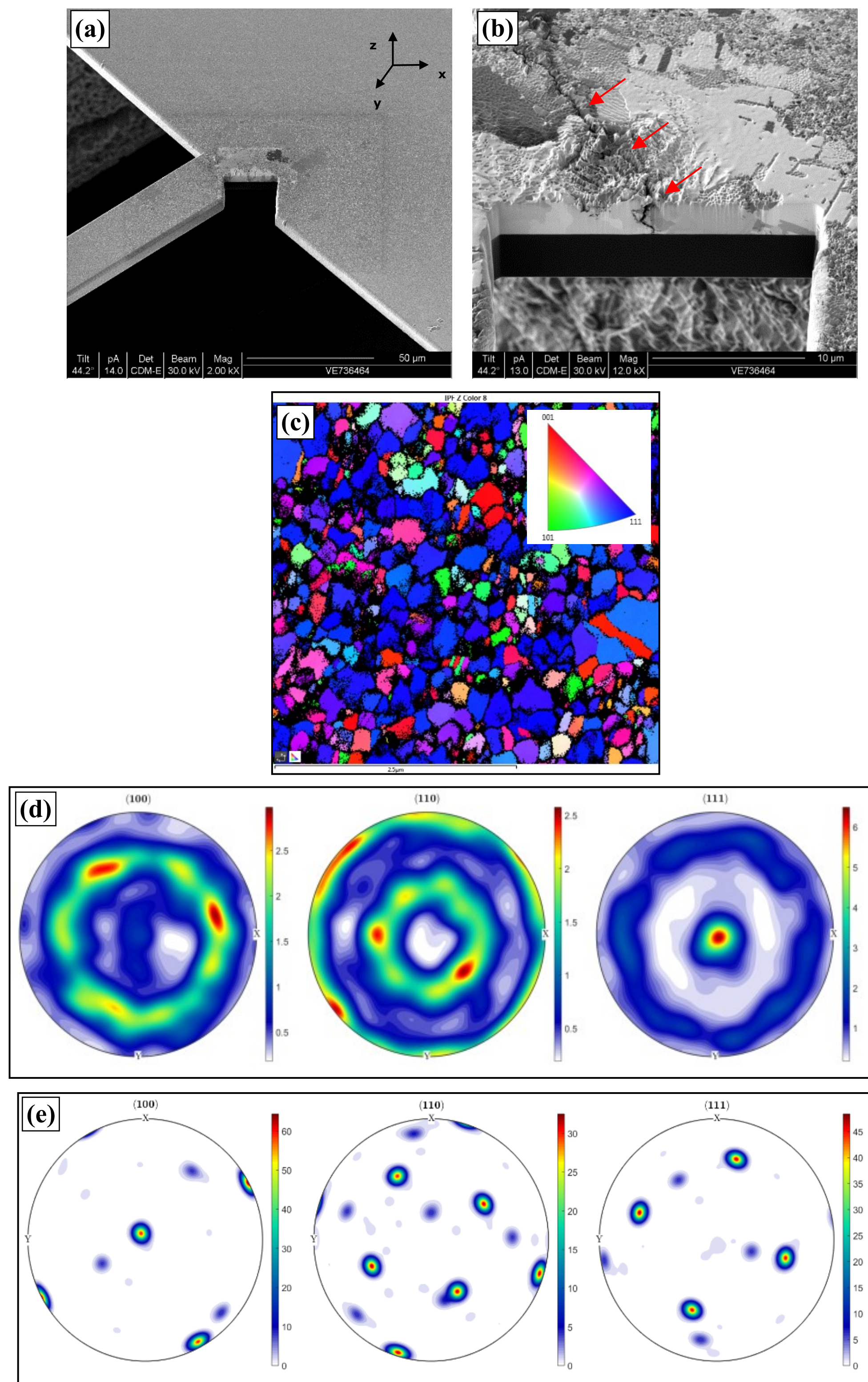

Fig. 5. (a&b) FIB images reveling the deformation and crack formation (marked with red arrows) in Cu film. (c) Inverse pole figure z orientation mapping of as deposited Cu surface. Pole figure plot of Cu surface (d) after deposition (e) after fatigue loading. Crystal orientation in Z axis is changed from (111) to (100) orientation.

(marked with red arrows) but also has reached the copper-silicon interface. However, the

crack has not entered the silicon substrate. Similar features can be observed in fig. 6.a&b, where intergranular cracks were formed within the coarsened grains of the copper film. Moreover, formation of extrusions resulted in a surface roughening of copper film with an average height of extrusions being in the range of 50-100nm.Cracks in film were seen in depth along the slip lines indicating a typical deformation behavior of copper under fatigue loading [14,22,23].

EBSD analysis and pole figure data of as deposited copper and one undergone fatigue loading has shown distinctive differences in their texture (see fig. 5.c-e). The analysis was carried out in depth of the copper film along fibbed surface. The FIB cut was sophisticatedly executed to ensure a good indexing rate for EBSD on the copper thin film. Therefore, the silicon has an amorphous thin layer reducing the indexing rate on the copper to nearly zero, generating a good contrast between the copper thin film and the silicon substrate. The as deposited copper depicts strong (111) grain orientation along z direction in the EBSD analysis and the same can be seen also in the inverse pole figures (IPF) z mapping and in the pole figure plots. As the deposition process was low energy process, copper grains have grown along (111) orientation to reduce the surface energy. On the contrary, copper which has undergone fatigue loading exhibited reorientation of grains along (100) plane. The pole figure (see fig. 5.d&e) reiterates such a change in texture of copper grain from (111) to (100) plane. Under the mechanical loading nano-crystalline copper grains have undergone severe deformation resulting in misorientation in the grown grains. As the strain rate is high, for a given maximum possible stress, crystallization of copper grain tends to take place along a plane having minimum elastic modulus [23,24]. Among all given crystallographic planes, modulus of elasticity is minimum for (100) plane and it is about 60% smaller compared to that of (111) plane [23,24]. Therefore, the grains undergoing deformation tends to recrystallize along (100) orientation. These results also confirm the strain-energy-release maximization (SERM) model [24].

Furthermore, in order to map the stress level variations quantitatively in the deformed grains, kernel average misorientation map (KAM) was generated from EBSD data (see fig. 6.c&d). The orientation of each pixel is compared to its nearest neighbors providing a misorientation in degree. By plotting the misorientation mechanical strain in grains or sub grain structures can be depicted. SEM micrograph as well as IPF z mapping reveal that copper grains have grown bigger in size in depth of the film. However, the

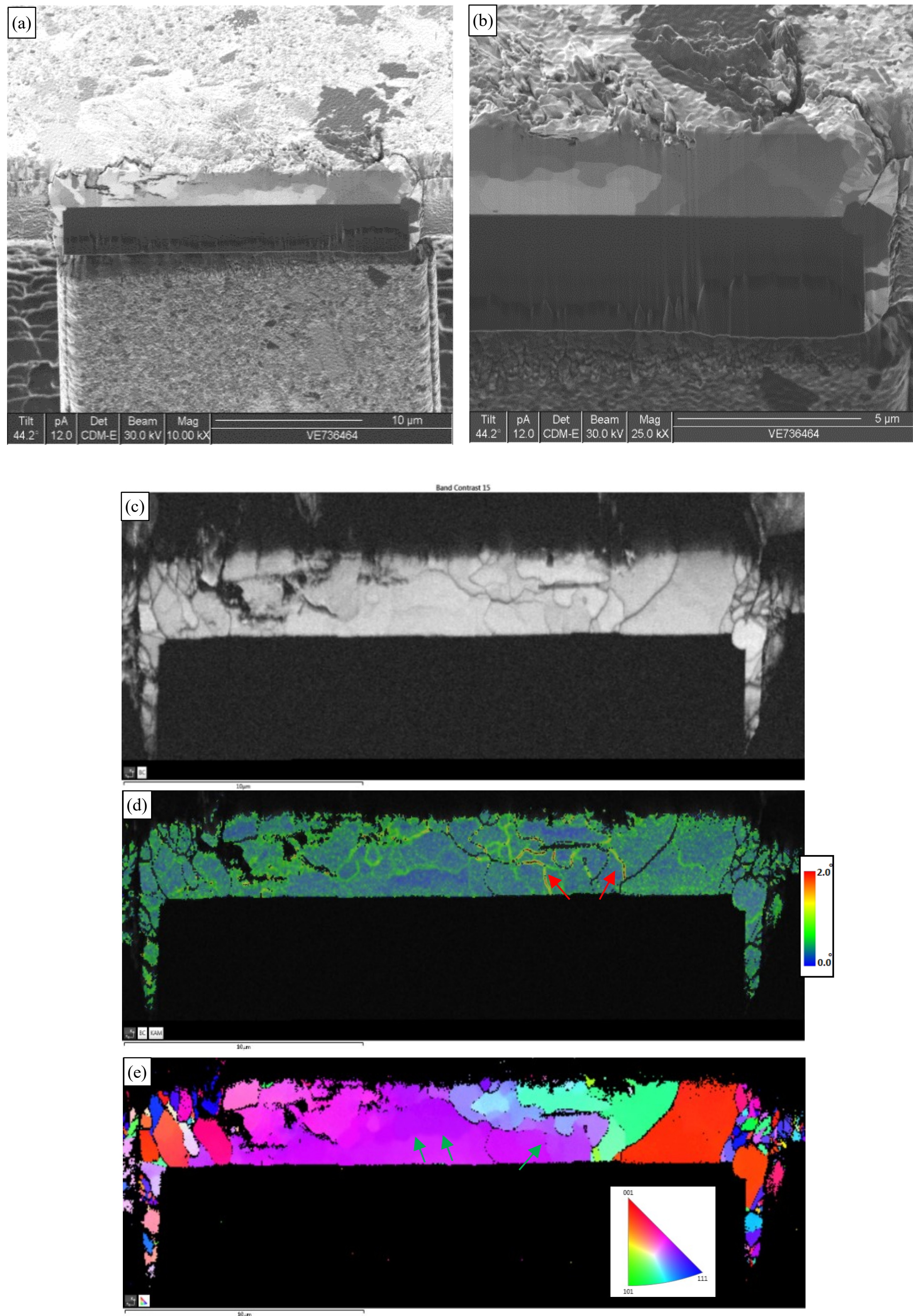

Fig. 6. (a) SEM micrograph after the FIB cut of a beam. (b) FIB image revealed the grain growth and crack formation in Cu film. (c&d) A strong variation in stress level in the film is clearly seen in KAM map. Arrows mark regions of high mechanical stress in a grain (e) IPF x orientation mapping of Cu film after fatigue showing the increased grain size.

KAM map revealed distinctive lines (marked by red arrows) of local strain accumulation due to high mechanical stress inside a single grain as well as at some grain boundaries. In addition to it, in IPF z mapping, some of copper grains showed a clear color gradient indicating the grain is in phase of changing its crystal orientation due to high mechanical stress acting on it (see green arrow on fig. 6.e). As the process of deformation was still not completed, grains were still under a process of rearranging their crystal orientation and thus grains have depicted several strain lines. These strain lines are a possible nucleation site for formation of new cracks in the copper film. The initially deposited nano-crystalline copper grains have undergone severe accumulated mechanical strain leading to grain growth and reorientation. The process of deformation was not logically finished, as one of the four beams supporting the central plate was broken. In spite of the facts that all ends of all four beams were undergoing the fatigue loading during operation, due to fabrication inaccuracies (such as alignment issues, release etch undercut or overcut etc.) the broken arm was loaded severely compared to rest of the beams. Thus it broke prematurely.

As stated before, in the simulation, stress concentrations were found at either ends of the beam, and even higher stress intensities occurred at the corners of this structure. The experimental observations confirm this fact as cracks were found to be initiated in most of the cases at corners (see fig. 4) indicating maximum stress at this place. Furthermore, two FIB cross sections (fig. 5.a and fig. 6.a) and KAM images indicated grain growth and reorientation of grains. These images reveal that recrystallization was completed at the corners while at center part of beam, grain re-orientation and crack formation were still going on, when the vibration experiment was stopped. The stresses induced in the copper film initiated material transformation and thus extrusion, slip line formation, grain growth and grain orientation phenomenon were seen. Since all these phenomena were observed at one particular location in the film, one may conclude that the crystallographic lattice of copper must have undergone severe deformations. Therefore, it is highly possible that crack formation as well as propagation have taken place within the grains and as well along the grain boundaries.

The material dimensions such as thickness and grain size has very strong influence on the fatigue behavior of thin copper film. The existence as well as extent of extrusion seen in thin film during fatigue is also influenced by thickness and grain size. In a study by Zhang et.al. on the fatigue behavior of Cu films on polyimide substrates, extrusions were observed only in the grains sizes of 3µm or above; and on the other hand, fine crystalline copper or thinner copper films have shown no extrusions instead revealed high surface roughness,

faceting of grains with no visible damage in submicron grains, in spite of the fact that grain boundaries develop grooves and cracks in vicinity [21]. In the current situation, the copper film was3µm thick but had nano sized grains due to special deposition condition. However, the copper film not only revealed large amount of extrusions but also strong grain growth and crack formation was observed in the mechanically loaded area. This can be explained based on two hypotheses as follows. The copper film studied here was in as deposited conditions while one studied by the Zhang et.al. was annealed at different temperature for long duration [21,22]. Although fine crystalline copper films were annealed at relatively low temperature, annealing might have eliminated the stress (or strain) present in the film due to deposition process [2,3,25]. It is well known that copper after deposition tends to grow its crystal size under a phenomenon of self-recrystallization [25-27]. This is mainly due to stress relaxation effect. Moreover, the type and topography of substrate has a definite role to play in extent of stress induced the copper [25,28]. However, such a self-growth of crystal size from nano to micron size was not observed in the copper film under investigation. This implies that the stress in as deposited copper film was not high or sufficient for self-recrystallization. During the cyclic loading of the film, the stress required for recrystallization of nano-crystalline copper was offered which led to the grain growth in copper. This is also a reason why grains subjected to the mechanical loading underwent grain growth from nano to micron size, while rest of the grain maintained their as deposited grain size. Another important difference is that, unlike to fine crystalline copper of multiple grains through the film thickness used by Zhang et. al., copper grains in this investigation were columnar structured and thus single grains were present through the entire thickness of the film (see fig. 1.e&f). Thus, there was no grain boundary along the film thickness to stop the dislocation movement. This led to a situation that copper grains subjected to mechanical load, perpendicular to film thickness, underwent deformation and eventual grain growth. The deformation took place predominantly along width of copper crystals, as smallest dimension control the type of dislocation structure [21]. In both scenarios of grain growth due to stress relaxation or dislocation-assisted grain coarsening; fatigue mechanism seems to be dominated by facilitation of plastic deformation in large micron size copper grains, formation of extrusions and crack initiation. Preliminary investigations of our samples indicated that, while cracks were initiated along the extrusions (fig. 4), they favorably have grown along the grain boundaries of the coarsened grains (fig. 5&6).

4 Summary & conclusion

The plus shaped structure studied here is proven to be an excellent MEMS structure for investigating the fatigue behavior of thin films under mechanical loading. The structure corroborates the simulation results and demonstrates ability to load the thin films under concentrated fatigue loading. Furthermore, copper films subjected to mechanical load had a strong (111) orientation generated due to low deposition energy. This film has demonstrated gradual formation of slip marks and extrusions leading to initiation and growth of cracks during plastic deformation. A strong grain growth in the nano-crystalline film together with grain re-orientation from (111) to (100) under high strain energy was demonstrated in a local area. Both phenomena are a true reflection of fatigue deformation of thin copper films under concentrated mechanical loading. In short, plus shaped structures are ideal for studying the behavior of various thin films under different operating conditions such as high mechanical loading, high temperature and to analyze the performance of different types of thin films of metals, alloys, dielectrics etc. for the impact of deposition conditions on their material properties.

Using this fabrication process, the thickness of silicon structure and metal film and their interface can be tuned easily. Various materials such as oxide, nitride or other adhesion promoting materials can be studied to evaluate their influence on interface of thin metal with substrate. Moreover, the impact of different deposition processes such as sputtering or electro-chemically deposited thin copper films, or even an impact of topography can be investigated using these structures in future.

Acknowledgment

The financial support by the Austrian Federal Ministry for Digital and Economic Affairs and the National Foundation for Research, Technology and Development is gratefully acknowledged.

References

1. Murarka, S.P., Multilevel interconnections for ULSI and GSI era. Materials Science and Engineering: R: Reports, 1997. 19(3): p. 87-151.
2. Gupta, T., Copper Interconnect Technology2008: McGraw-Hill Professional Publishing.
3. Rosenberg, R., et al., Copper Metallization for High Performance Silicon Technology. Annual Review of Materials Science, 2000. 30(1): p. 229-262.
4. Hille, F., et al., Reliability aspects of copper metallization and interconnect technology for power devices. Microelectronics Reliability, 2016. 64: p. 393-402.
5. Kaloyeros, A.E. and E. Eisenbraun, Ultrathin Diffusion Barriers/Liners for Gigascale Copper Metallization. Annual Review of Materials Science, 2000. 30(1): p. 363-385.
6. Nelhiebel, M., et al., Effective and reliable heat management for power devices exposed to cyclic short overload pulses. Microelectronics Reliability, 2013. 53(9): p. 1745-1749.
7. Wong, H.Y., N.F. Mohd Shukor, and N. Amin, Prospective development in diffusion barrier layers for copper metallization in LSI. Microelectronics Journal, 2007. 38(6): p. 777-782.
8. Shacham-Diamand, Y., et al., Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications2009: Springer-Verlag New York.
9. Toomey, J.J., S. Hymes, and S.P. Murarka, Stress effects in thermal cycling of copper (magnesium) thin films. Applied Physics Letters, 1995. 66(16): p. 2074-2076.
10. Eberl, C., et al., Damage analysis in Al thin films fatigued at ultrahigh frequencies. Journal of Applied Physics, 2006. 99(11): p. 113501.
11. Eberl, C., et al., Ultra high-cycle fatigue in pure Al thin films and line structures. Materials Science and Engineering: A, 2006. 421(1): p. 68-76.
12. Schwaiger, R. and O. Kraft, High cycle fatigue of thin silver films investigated by dynamic microbeam deflection. Scripta Materialia, 1999. 41(8): p. 823-829.
13. Eve, S., et al., Development and validation of an experimental setup for the biaxial fatigue testing of metal thin films. Review of Scientific Instruments, 2006. 77(10): p. 103902.

14. Wimmer, A., et al., Damage evolution during cyclic tension–tension loading of micron-sized Cu lines. Acta Materialia, 2014. 67: p. 297-307.
15. Heinz, W., R. Pippan, and G. Dehm, Investigation of the fatigue behavior of Al thin films with different microstructure. Materials Science and Engineering: A, 2010. 527(29): p. 7757-7763.
16. Bigl, S., Wurster, S., Cordill, M.J., Kiener D., Substrate-Influenced Thermo-Mechanical Fatigue of Copper Metallizations: Limits of Stoney's Equation, Materials 2017, 10(11): p. 1287-1294.
17. Finot, M., Blech, I.A., Suresh, S., Fujimoto H., Large deformation and geometric instability of substrates with thin-film deposits, Journal of Applied Physics 2017, 81: p. 3457-3464.
18. Saghaeian, F., et al., Design and development of MEMS-based structures for in-situ characterization of thermo-mechanical behaviour of thin metal films. Microelectronics Reliability, 2018. 88-90: p. 829-834.
19. Rafiee, P. and G. Khatibi, A fast reliability assessment method for Si MEMS based microcantilever beams. Microelectronics Reliability, 2014. 54(9): p. 2180-2184.
20. Rafiee, P., Khatibi, G., Solazzi, F., Optically-detected nonlinear oscillations of single crystal silicon MEMS accelerometers, Microelectronics International, 2016, 33(2): p. 107-115.
21. Zhang, G.P., et al., Length-scale-controlled fatigue mechanisms in thin copper films. Acta Materialia, 2006. 54(11): p. 3127-3139.
22. Zhang, G.P., et al., Fatigue and thermal fatigue damage analysis of thin metal films. Microelectronics Reliability, 2007. 47(12): p. 2007-2013.
23. Hertzberg, R.W., P.R. Vinci, and J.L. Hertzberg, Deformation and fracture mechanics of engineering materials1996: J. Wiley & Sons.
24. Park, H. and D.N. Lee, The evolution of annealing textures in 90 Pct drawn copper wire. Metallurgical and Materials Transactions A, 2003. 34(3): p. 531.
25. Lingk, C. and M.E. Gross, Recrystallization kinetics of electroplated Cu in damascene trenches at room temperature. Journal of Applied Physics, 1998. 84(10): p. 5547-5553.

26. Patten, J.W., E.D. McClanahan, and J.W. Johnston, Room-Temperature Recrystallization in Thick Bias-Sputtered Copper Deposits. Journal of Applied Physics, 1971. 42(11): p. 4371-4377.
27. Huang, R., Robl, W., Hajdin, C., Detzel, T., Dehm, G., Stress, sheet Resistance, and microstructure evolution of electroplated Cu films during self-annealing, IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, 2010, 10(1): p. 47-54.
28. Moriyama, M., et al., The Effect of Strain Distribution on Abnormal Grain Growth in Cu Thin Films. MATERIALS TRANSACTIONS, 2004. 45(10): p. 3033-3038.

Paper D

Microstructure and Stress Gradients in TiW Thin Films Characterized by 40nm X-ray Diffraction and Transmission Electron Microscopy

F. Saghaeian[a,b,*] , J. Keckes[b], S. Woehlert[a], M. Rosenthal[c], M. Reisinger[d], J. Todt[e]

a Infineon Technologies Austria AG, 9500 Villach, Austria

b Department of Materials Physics, Montanuniversitaet Leoben

c European Synchrotron Radiation Facility, Grenoble, France

d Kompetenzzentrum Automobil-und Industrie-Elektronik GmbH, Europastraße 8, 9524 Villach, Austria

e Erich Schmid Institute for Materials Science, Austrian Academy of Sciences, Leoben, Austria

Submitted manuscript to Thin Solid Films (Jan 2019)

Abstract

The functionality of TiW diffusion barrier is often correlated with the presence of impurity atoms, diffusion of neighbor layer atoms, and depletion of titanium from the film and seldom attributed to the microstructure of the film. Here in this work, morphological aspects of sputter deposited TiW thin films as well as the influence of process parameters on residual stress of the film were investigated to understand their role in the functionality of TiW as a barrier. Two films, one tensile (+2 GPa) and another with compressive stress (-2 GPa), deposited by varying process conditions show distinctive differences in their microstructure. Both films were composed of α-W crystal structure but film with compressive stress has densely packed microstructure with no inter-granular porosity unlike to the tensile stressed film, where substantial porosity was present. Furthermore, TiW films were studied using a cross-sectional synchrotron 40 nm X-ray nano-diffraction technique which revealed that a gradual stress relaxation takes place in tensile stressed TiW film during its growth while in the compressive film no such relaxation was observed. The stress relaxation is mainly attributed to the increase in grain size during film growth of the tensile film. Based on these investigations, a growth model was put forth to correlate the deposition conditions and morphology of the TiW films grown.

1 Introduction

The microstructure and residual stress of a sputtered film are strongly influenced not only by processing conditions such as process pressure, target power, temperature, substrate crystal structure and topography etc. but also inherent properties of sputtered metals [1,2]. The various process parameters listed above have a strong influence on the crystal structure, as well as on the extent of defects incorporated into the deposited film. The gradients of microstructure and residual stress ultimately define the film's functional properties. Especially, sputter deposited films of refractory metals such as molybdenum or tungsten show a strong influence of process parameters on properties of the correspondent deposited films [3-6]. The same behavior has also been reported for a pseudo-alloy of tungsten with titanium in an extensive study concerning its barrier and adhesion properties [7-11]. It has been demonstrated experimentally that functional properties of these films, such as their adhesion, barrier performance, resistivity, as well as Ti content etc. [9-12], depend on processing parameters such as process gas, deposition pressure or the applied substrate bias voltage. Based on these studies, several degradation models have been put forth, addressing failure of TiW as a barrier layer. Diffusion of power metal into the barrier layer, the composition of TiW films (namely depletion of Ti content), presence of impurity atoms (O2 or N2) etc. are some major factors which have influence on the performance of TiW as a barrier [10-13]. However, microstructure of barrier film carries a primary role in defining the functionality of barrier films which is not yet studied in great detail [14,15]. Thus it is necessary to get more insight into the residual stress of the film, its chemical composition or morphological aspects of TiW to understand its functionality as a barrier. Especially the fatigue behavior is known to depend strongly on the type, magnitude and distribution of residual stresses. Also, such investigation is beneficial, as residual stress of TiW film can be used for certain applications [16].

The major constituent of TiW films is tungsten and thus the films inherit their material properties from tungsten. As a consequence, similar to sputtered pure tungsten films, intrinsic stress of TiW film can also be tuned from tensile to compressive regime by tuning the process parameters [5,6,11,17,18]. In these studies, stress was tuned by adapting different process conditions while the Ti content of these films or the target composition had marginal influence. Evans et. al. have investigated a TiW film from 3% by weight (10% at.) Ti target which is significantly less than other studies and still reported compressive stress in the film [17,18]. This Ti concentration of target is below the solid solubility limit

of titanium in tungsten. Furthermore, Nowicki et. al. have deposited various TiW films with tensile as well as compressive stresses (2 GPa), but having almost same Ti content (~30% at.) in the deposited film [11]. In comparison to it, Plappert et. al. have studied TiW film with considerably less (18% at.) Ti content but had fairly same compressive stress (1.8 GPa) [12]. Additionally, they have explained the effect of Ti re-sputtering due to difference in masses of Ti and W. The depletion of Ti in deposited film was due to the high energy deposition process which can be boosted with additional DC bias. The application of DC bias further enhances this effect, reducing Ti content with increasing value of applied bias [7,9]. It is thus evident that residual stress of the TiW barrier is not dependent on its composition (Ti content) but should have influence of its microstructural aspects such as grain size, grain boundaries etc. which are ultimately governed by the sputtering process itself.

In this present study, a detailed investigation on microstructure, morphology and residual stresses and its correlation to sputtering process will be presented for different TiW films deposited using two sets of deposition conditions.

2 Experiment and methods

For this study, 200 mm diameter Si wafers having orientation along (100) plane and a thickness of 725 µm were used as a substrate. The deposition was carried out from a W30Ti (at. %) target in a DC sputtering. The deposition process is explained in detail elsewhere [12]. TiW films were deposited with constant process pressure during sputtering. This was achieved by controlling the flow of the process gas Ar. The residual stress in two types of deposited films was tuned by changing the sputter pressure as well as by tuning the bias voltage applied on the substrate. Thin films with high compressive stress were deposited using a sputter pressure of 0.2-0.8 Pa and deposition rate of 2 nm/s; additionally 100-600 W RF bias power was applied on the substrate. Two films with thicknesses of 100 and 300 nm were deposited by varying the deposition time (termed TiW-C1 and TiW-C2 respectively). On the other hand, in order to sputter thin films with tensile stress and thicknesses of 100 and 300 nm (termed TiW-T1 and TiW-T2 respectively), sputter pressure was increased tenfold, to 2-8 Pa, and RF power was switched off while keeping the gas flow unchanged. In both cases, the substrate was kept at room temperature and not heated actively.

The titanium content of deposited films was measured using the X-ray fluorescence (XRF) technique. The film's specific resistivity was measured using a four point probe method. The wafer warpage was measured using a commercially available Eichhorn+Hausmann tool which also calculates the film stress based on the Stoney equation [19].

Laboratory X-ray diffraction (XRD) studies were performed using a Rigaku SmartLab 5-circle diffractometer, equipped with Cu-Kα radiation, a parabolic multilayer mirror, a graphite monochromator and a scintillation counter. Phase analysis was carried out in grazing incidence geometry, using a fixed incidence angle of 1.25°. For residual stress characterization, the $\sin^2\psi$ technique was employed in side-inclination mode using the 211 reflection of the TiW solid solution phase. Synchrotron XRD studies with an X-ray nanoprobe diameter of ~40 nm were performed at the Nanofocus extension of beamline ID13 of the European Synchrotron Radiation Facility in Grenoble, France [20-22]. The photon energy was 12.7 keV and transmission XRD patterns were collected on an Eiger X 4M detector using an exposure time of 50 ms. The samples were prepared as mechanically polished cross-sectional slices of 40 µm thickness and scanned along the film growth direction with a step of 20 nm. The experimental geometry was calibrated using a NIST Al2O3 standard powder sample and data treatment was done using the pyFAI software package. The methodology for film depth-resolved residual stress evaluation is described in detail elsewhere [20-22].

In order to obtain more insight in the impact of the applied deposition parameters on the TiW microstructure, transmission electron microscope (TEM) analyses were carried out on a JEM-2100F, JEOL (200 kV) equipped with an image-side CS corrector. The microstructural images were acquired in conventional TEM mode. Additionally, the microstructure of the samples was investigated by scanning electron microscopy (SEM) in a HITACHI S-4800 device, also applying energy-dispersive X-ray spectroscopy (EDX). To complement these imaging techniques, the surface roughness was also characterized using a NX-20 system from Park Systems atomic force microscope (AFM).

3 Results and discussion

The film stress values obtained from wafer curvature measurements and Ti content of the four different films are listed in table Tab. 1. As shown, upon increasing the film thickness from 100 to 300 nm, tensile stress decreases drastically, whereas the stress change was

insignificant for compressive films. The Ti content of the tensile films was measured to be much higher than that of the compressive film, but remained unaffected by deposition time (film thickness).

As a next step, all four films (cf. Tab. 1) were studied using laboratory XRD, confirming that they have a BCC crystal structure (cf. Fig. 1) inherited from their major constituting element W, corroborating earlier reports [6,7]. The inset in fig. 1 shows an expanded view of the 110 peak of the four films, which are all centered around the 2θ angle of the W 110 peak. The peak positions of both compressive films are at lower angles compared to those of the tensile films and are not affected by films thickness, whereas there is a noticeable peak shift between the two tensile films. These observations can be explained by the effect of Ti concentration on the solid solution's lattice parameter, as well as the differing levels of residual stress and amount of crystal defects. As mentioned above, the peaks positions for all four TiW films correspond to those of the α-W crystal structure. It has been reported that W films with compressive stress exhibit a densely packed columnar microstructure (without any porosity) consisting of α-W crystals [6]. In case of tensile stressed films, a columnar microstructure of W with a substantial amount of porosity has been reported, as well as the presence of β-W crystals [6]. In the present study however, the β-W structure was found neither in tensile films nor in compressive films.

Film name	Film thickness (nm)	Stress (MPa)	Ti content (at. %)
TiW-C1	100	-2025	14
TiW-T1	100	2076	28
TiW-C2	300	-1985	13
TiW-T2	300	1621	27

Tab 1. Properties of the investigated TiW films, as measured by wafer warpage and XRF.

In order to investigate the morphology or microstructure of the deposited TiW films, SEM, AFM and high resolution TEM investigations were carried out on the 300 nm thick samples. In fig. 2 a&b it is clearly visible, that the TiW-T film with tensile stress has very high surface roughness in comparison to TiW-C film with compressive stress. Furthermore, the grain size of TiW-T is also found to be significantly smaller in comparison to TiW-C

(Fig. 2 c&d). Both these observations indicate low energy deposition conditions for the film with tensile stress. Additionally, EDX mapping was carried out on top surface as well as on cross-section of both samples (Fig. 2 e-h). The elemental mapping show that Ti and W are uniformly distributed across the film thickness, i.e. no segregation of Ti was observed. These results are corroborated by the abovementioned XRD analysis as no separate peaks for Ti were present in the spectra. Furthermore the Ti concentration as evaluated by EDX in the film with compressive stress was lower in comparison to the TiW film with tensile stress, confirming previous measurements by XRF. Finally, It was found by means of AFM that average (RMS) surface roughness of compressive film was 2.47 nm, whereas the tensile film's average roughness was much higher, at 7.09 nm (AFM height maps not shown).

The TEM images in fig. 3 reveal distinctive columnar grains for both, the tensile

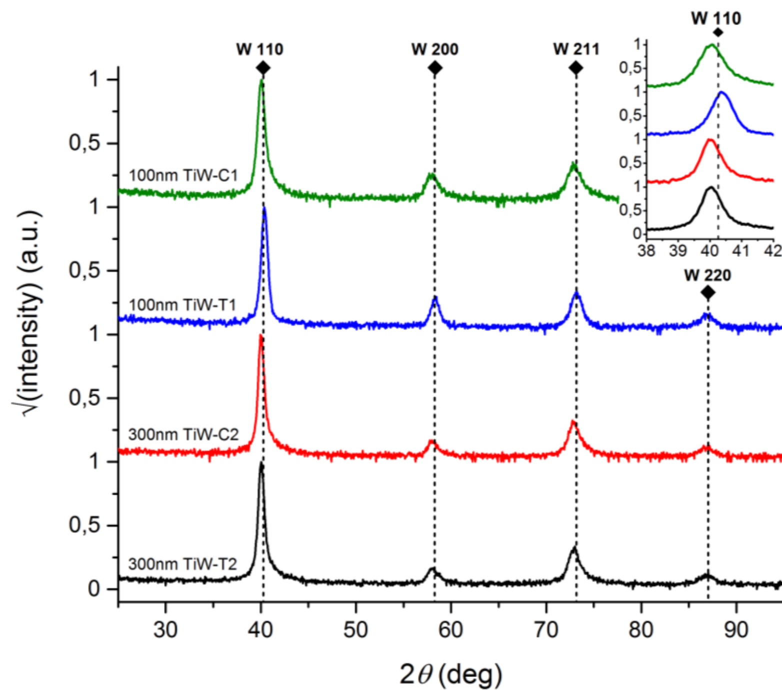

Fig. 1 Laboratory XRD patterns, confirming the BCC crystal structure of the TiW solid solution

(Fig. 3 a,b) and compressively (Fig. 3 c, d) stressed TiW films. The TiW-C film shows densely packed crystals without any signs of porosity. On the contrary, the TiW-T film exhibits numerous thin columnar grains with frequent gaps or pores between them. Furthermore, grains of the TiW-T film have rather faceted ends, unlike TiW-C grains and surface roughness is thus significantly higher than that of the compressive film. According

to the Thornton model, if the film growth conditions allow only surface diffusion processes (zone I), columnar grain morphology with high porosity and faceted surface is deposited. On the other hand, the possibility of bulk diffusion processes promotes equiaxed grains and planarization (starting in zone T, fully developed in zone 3) [1,23]. Thus, the TEM-based morphological investigations indicate that TiW-T films were grown under deposition

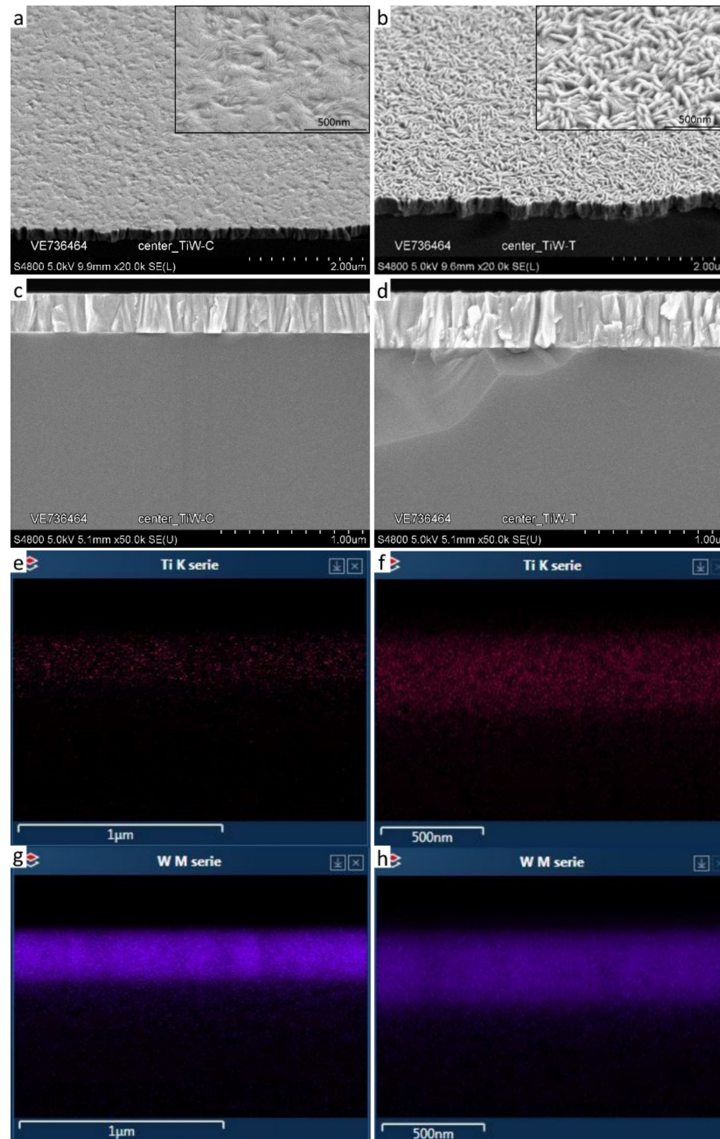

Fig. 2 SEM images showing surface morphology of (a) compressive TiW-C2 film (b) tensile TiW-T2 film. Insets show high resolution images with visible difference in surface roughness. (c & d) depict cross section of TiW films with compressive (TiW-C2) and tensile stress (TiW-T2) respectively. EDX elemental mapping for Ti and W are shown in (e & g) from TiW-C2 film and in (f & h) for TiW-T2 film respectively. Mapping is carried out from cross-section of the films.

conditions resembling zone I of the Thornton model, while TiW-C films were deposited under conditions matching zone T. This attribution to zone T can be made since there crystallites are still distinctly columnar, while their density is increased drastically. This difference in film morphology is due to elevated high energy ion bombardment, which is in turn facilitated by the tenfold decrease in sputtering pressure (increasing the mean free path of neutral and ionized sputtered particles and plasma atoms), as well as the bias voltage applied to the substrate during the deposition of the compressive films.

The film morphology can also be used to understand the stress state of the tensile and compressive films: As grains develop in TiW-T films under low energy conditions with voids and small gaps between them, at some point it becomes energetically favorable for crystallites to coalesce in order to minimize surface energy and thus attractive forces start to act between them. Essentially, this can be viewed as a sort of densification of an under-dense film at the expense of introducing tensile stress. The same analogy has also been used for sputtered pure tungsten films [5, 6]. On the other hand, for the TiW-C films the bombardment by high energy particles increases ad-atom mobility, also promoting bulk diffusion and results in a dense structure with a less jagged surface. Another consequence of ion bombardment is the incorporation of defects into the film, which leads to the accumulation of compressive stress. A main contribution to high compressive stresses is the inclusion of atoms from the process plasma in the crystal lattice. In this case, the lowered process pressure promoted the incorporation of Ar ions into the TiW-C films, which is also corroborated by the increased lattice parameter measured by XRD for these films. Moreover, the observed decrease in Ti content that goes along with the decrease in process pressure can also be explained by the enhanced activity of plasma ions on the substrate. This is due to preferential resputtering of Ti from the films deposited onto the substrate, as the atomic mass of Ar and Ti are similar, whereas W atoms are much heavier [12]. The absence of a strong elemental contrast at grain boundaries and interfaces indicates that there is no segregation of Ti in the prepared samples and that Ti is in fact always present in the form of a (supersaturated) solid solution within BCC structured TiW. From the point of view of Hume-Rothery rules, it is furthermore clear that Ti atoms will always take substitutional positions in a W lattice, as the difference of atomic radii between Ti and W is only 3.7 %.

As the film deposition is a continuous process leading to grain growth during deposition itself, the stress level should show a depth gradient in the films. In order to investigate this, the films were investigated using a cross-sectional synchrotron X-ray nanodiffraction

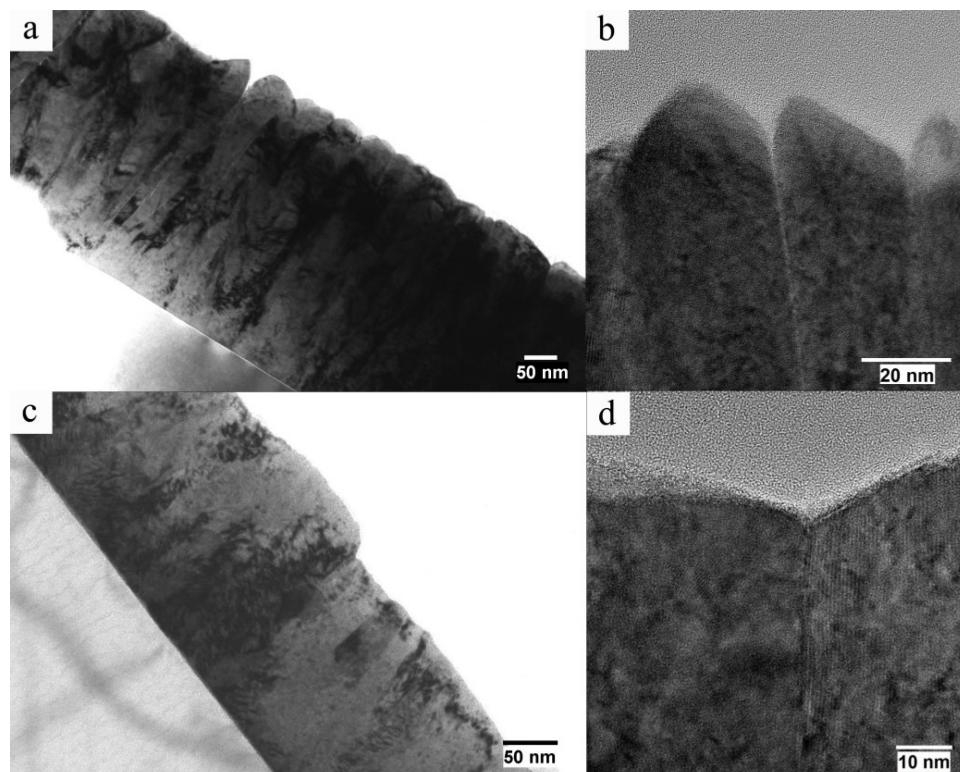

Fig. 3 TEM images of the different TiW films. (a,b) are from tensile TiW-T2 and (c,d) from compressive TiW-C2 film.

technique (see fig. 4). In the case of the two tensile film specimens a marked depth-gradient of residual stresses could be determined, showing a relaxation of film stress during film growth. This behavior is plausible, as high tensile stresses are not sustainable for large film thicknesses. Another interpretation for this is the relation between the developing film microstructure and its tensile load-bearing capacity, where the increase in grain size after the initial nucleation phase is accompanied by a decrease in ultimate tensile strength, hence leading to decreasing film stress as the film grows. A similar behavior has been already reported for pure W films used as conductive layers for hollow through-silicon vias [24].

For the two compressively stressed samples, no significant depth-gradient of residual stress could be measured, indicating rather more stable growth conditions, where films stress might not yet be limited by the material's compressive strength. Additionally, the larger grain size of the TiW-C films is manifested in a larger scatter of residual stress values and a less uniform diffraction peak intensity, which are both due to the worse diffraction statistics,

where a smaller number of grains are within the gauge volume of the X-ray nanobeam, as compared to the nanocrystalline TiW-T films.

Finally, the film thickness-dependent peak width of the two investigated TiW-T films correlates well with the findings of the TEM investigation, namely the presence of a fine-grained nucleation layer leading to broader diffraction peaks close to the substrate interface. However, for the TiW-C films the worse diffraction statistics make a similar interpretation difficult and therefore we refrain from drawing any conclusions here.

Film thickness-averaged residual stresses were also measured by laboratory XRD and qualitatively confirm the results from the synchrotron experiments, although values are somewhat higher (see fig. 5). The explanation for this discrepancy most likely lies in the preparation of the cross-sectional sample slices, which probably relieved some of the stress present in the uncut samples. Since W is an isotropic material and the Ti content is rather

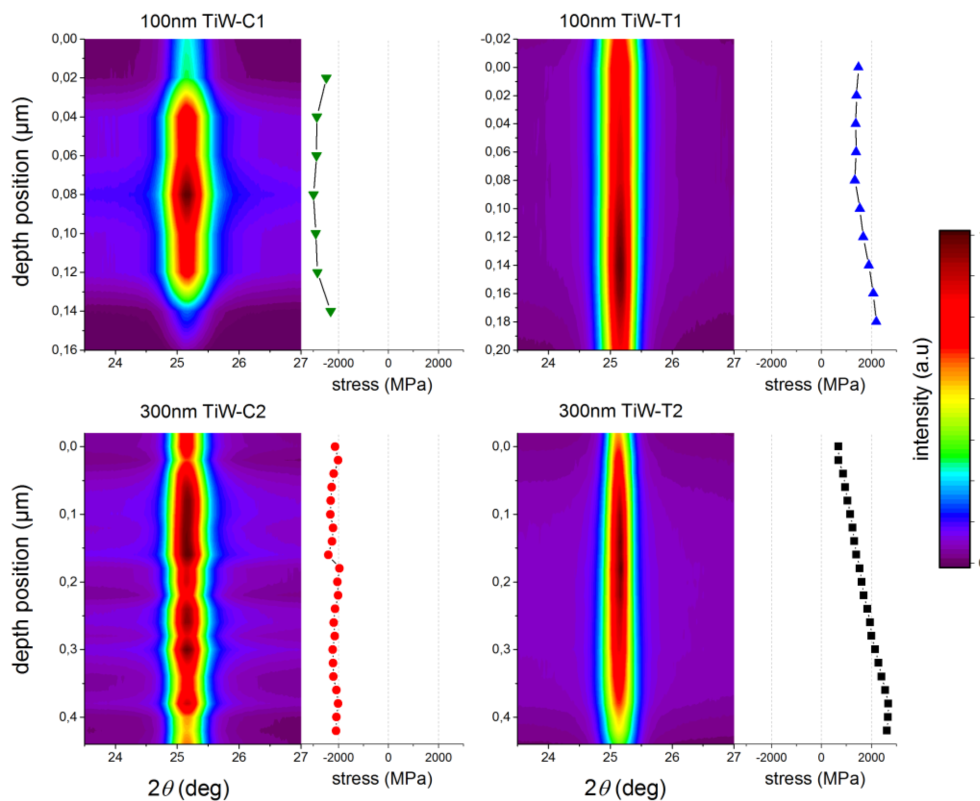

Fig. 4 Cross-sectional synchrotron nanodiffraction revealed the film depth-resolved evolution of the TiW 110 Bragg peak and the corresponding residual stress profiles for both tensile and compressive samples. Due to the diameter of the X-ray nanoprobe, the apparent film thickness is somewhat larger than the real thickness.

low, there should not be any appreciable influence of the specific Bragg peak used for XRD stress evaluation. The influence of the Ti content on the X-ray elastic constants of the material was accounted for in all cases and considering the low scatter of values in the $\sin^2\psi$ and depth-resolved stress evaluations, there can be only little doubt with respect to the precision and reliability of the presented stress values.

In comparison to previous studies on similar TiW barrier layer systems, mostly deposited on Si wafers and by similar methods, but with varying thicknesses and Ti content, the stress values found in this study fall well within the range of known values [11,12,17,25,26]. Moreover, literature values for residual stresses in pure W films [5,6,27] virtually lie within the same limits, illustrating once more that Ti content does not play a decisive role for film stress.

In comparison to the wafer warpage based stress calculation (c.f. Tab. 1), it has to be stated, that the XRD-based technique is sensitive to the measurement position on a wafer, whereas the warpage measurement delivers an average stress value for the entire wafer. The observed discrepancies between these methods therefore indicate a somewhat non-homogeneous

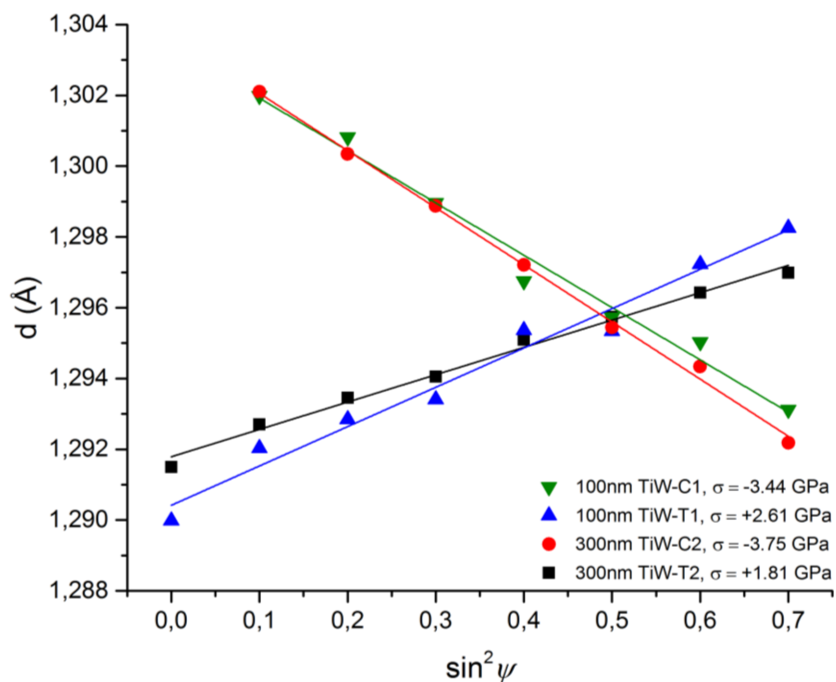

Fig. 5 Residual stress evaluation by means of laboratory XRD qualitatively confirms the wafer curvature and synchrotron measurements.

distribution of residual stress on the wafer, i.e. most likely there is a radial stress gradient on the wafers.

A focus of this work was placed on residual stresses, since they have a major impact on adhesive strength and since tensile stressed films also have porous morphology, which is undesirable for functional properties. In general terms, the stress characterization by three different methods provided a consistent picture about the different films' stress state, but limitations of the respective techniques have to be kept in mind to understand the slight differences between the corresponding measurement results.

4 Conclusion

In this work, TiW thin films were investigated in terms of their microstructure, material composition and stress state, as well as depth-resolved stress distribution. Two coating types with two different thicknesses each were grown obtaining either tensile or compressive residual film stress. Our findings are as follows:

A marked film thickness-gradient of residual stresses has been found in the tensile TiW films, characterized by cross-sectional X-ray nanodiffraction. With increasing thickness, the stress magnitude decreases, indicating either relaxation or decreasing load bearing capacity of the film. Similar observations have been made recently also for a pure W film.

As with pure W films that are manufactured by a similar process, the film stress can be tuned to be either tensile or compressive, just by changing the sputter pressure in the deposition chamber. High pressures decrease the plasma energy and lead to tensile stress, whereas low pressures increase the mean free path for energetic particles and result in compressive film stress.

The low energy growth conditions of tensile films induce a zone I growth morphology with thin, columnar grains and cause a porous film with high surface roughness.

Bombardment by high energy ions of the sputtered metals and the Ar process gas serves to densify and planarize the film, eliminating tensile stress and resulting in zone T growth. High compressive stresses can be achieved by further energizing metallic and plasma ions through the application of a substrate bias voltage. However, preferential re-sputtering of Ti under these conditions results in a diminished Ti content and may be a disadvantage of such an approach.

The combination of high resolution microstructural and residual stress characterization employed in this work proved to be a very useful tool for the correlation of film thickness-dependent growth mechanisms with the respective deposition process parameters. The acquired results add to the understanding of the TiW thin film system and will enable further improvements to its functional performance in various applications.

Acknowledgments

The nanobeam XRD experiments were performed on beamline ID13 at the European Synchrotron Radiation Facility (ESRF), Grenoble, France. We are grateful to Martin Rosenthal and Manfred Burghammer at the ESRF for providing assistance in using beamline ID13. Author Saghaeian is thankful to Dr. Borna Marija for providing valuable input on TEM investigations.

References

1. Thornton, J.A., *The microstructure of sputter-deposited coatings.* Journal of Vacuum Science & Technology A, 1986. **4**(6): p. 3059-3065.

2. Gudmundsson, J.T., et al., *High power impulse magnetron sputtering discharge.* Journal of Vacuum Science & Technology A, 2012. **30**(3): p. 030801.

3. Hoffman, D.W. and J.A. Thornton, *Internal stresses in Cr, Mo, Ta, and Pt films deposited by sputtering from a planar magnetron source.* Journal of Vacuum Science and Technology, 1982. **20**(3): p. 355-358.

4. Hoffman, D.W. and C.M. Kukla, *Determination of film stresses during sputter deposition using an in situ probe.* Journal of Vacuum Science & Technology A, 1985. **3**(6): p. 2600-2604.

5. Itoh, M., M. Hori, and S. Nadahara, *The origin of stress in sputter-deposited tungsten films for x-ray masks.* Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 1991. **9**(1): p. 149-153.

6. Vink, T.J., et al., *Stress, strain, and microstructure in thin tungsten films deposited by dc magnetron sputtering.* Journal of Applied Physics, 1993. **74**(2): p. 988-995.

7. Ramarotafika, H. and G. Lemperiere, *Influence of a d.c. substrate bias on the resistivity, composition, crystallite size and microstrain of WTi and WTi-N films.* Thin Solid Films, 1995. **266**(2): p. 267-273.

8. Ghate, P.B., et al., *Application of Ti: W barrier metallization for integrated circuits.* Thin Solid Films, 1978. **53**(2): p. 117-128.

9. Hartsough, L.D., *Resistivity of bias-sputtered TiW films.* Thin Solid Films, 1979. **64**(1): p. 17-23.

10. Canali, C., et al., *Interdiffusion and compound formation in the c□Si/PtSi/(Ti□W)/Al system.* Thin Solid Films, 1982. **88**(1): p. 9-23.

11. Nowicki, R.S., et al., *Studies of the Ti-W/Au metallization on aluminum.* Thin Solid Films, 1978. **53**(2): p. 195-205.

12. Plappert, M., et al., *Characterization of Ti diffusion in PVD deposited WTi/AlCu metallization on monocrystalline Si by means of secondary ion mass spectroscopy.* Microelectronics Reliability, 2012. 52(9): p. 1993-1997.

13. Oparowski, J. M., et al., The effects of processing parameters on the microstructure and properties of sputter-deposited TiW thin film diffusion barriers, Thin solid films 153, (1987), 313-328.

14. Kaloyeros, A.E. and E. Eisenbraun, *Ultrathin Diffusion Barriers/Liners for Gigascale Copper Metallization.* Annual Review of Materials Science, 2000. **30**(1): p. 363-385.

15. Gupta, T., *Copper Interconnect Technology*2008: McGraw-Hill Professional Publishing.

16. Kennedy, M., et al., *Residual Stress Control to Optimize Pzt Mems Performance.* MRS Proceedings, 2002. 741, J5.37.

17. Evans D. R., et al., *3% Ti-Tungsten Diffusion Barriers I . A Discussion of the Role of the A15 Structure.* Journal of The Electrochemical Society, 1994, 141, 1867-1871.

18. Leet D. M., et al., *3% Ti-Tungsten Diffusion Barriers: II . The Effect of Deposition Temperature and Nitrogen Inclusion.* Journal of The Electrochemical Society, 1995, 142, 2013-2019.

19. Janssen, G.C.A.M., et al., Celebrating *the 100th anniversary of the Stoney equation for film stress: Developments from polycrystalline steel strips to single crystal silicon wafers.* Thin Solid Films, 2009. **517**(6): p. 1858-1867.

20. Keckes, J., et al., *X-ray nanodiffraction reveals strain and microstructure evolution in nanocrystalline thin films.* Scripta Materialia, 2012. **67**(9): p. 748-751.

21. Stefenelli, M., et al., *X-ray analysis of residual stress gradients in TiN coatings by a Laplace space approach and cross-sectional nanodiffraction: a critical comparison.* Journal of Applied Crystallography, 2013. **46**(5): p. 1378-1385.

22. Keckes, J., et al., *30 nm X-ray focusing correlates oscillatory stress, texture and structural defect gradients across multilayered TiN-SiOx thin film.* Acta Materialia, 2018. **144**: p. 862-873.

23. Freund, L.B. and S. Suresh, *Thin Film Materials: Stress, Defect Formation and Surface Evolution*2004, Cambridge: Cambridge University Press.

24. Hammer, R., et al., *High resolution residual stress gradient characterization in W/TiN-stack on Si(100): Correlating in-plane stress and grain size distributions in W sublayer.* Materials & Design, 2017. **132**: p. 72-78.

25. Fugger, M., et al., *Comparison of WTi and WTi(N) as diffusion barriers for Al and Cu metallization on Si with respect to thermal stability and diffusion behavior of Ti*. Microelectronics Reliability, 2014, 54, 2487-2493.

26. Kleinbichler, A., et al., *Annealing effects on the film stress and adhesion of tungsten-titanium barrier layers.* Surface and Coatings Technology, 2017, 332, 376-381.

27. Cordill, M. J., et al., *Adhesion measurements using telephone cord buckles.* Materials Science and Engineering: A, 2007, 443, 150-155.