




Chair of Functional Materials and Materials Systems

Master's Thesis



Development and Characterisation of 3D-
Stacks with Porous Metal Layers

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May 2020

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Acknowledgements

I would first like to thank my thesis advisor Univ.-Prof. Christian Mitterer from the Department of Materials Science at the Montanuniversity Leoben and Dr. Barbara Eichinger and Dr. Martin Mischitz from Infineon Technologies Austria. Their doors were always open in need of guidance or for questions about my research and writing.

I want to express my gratitude to the experts at Infineon Technologies and SAL Villach for their technical support throughout the thesis. They are too numerous to mention individually. I am very grateful for all the help throughout the thesis by each and every one of you.

To my colleagues in DCI and later IFB I say a thank you by heart for a wonderful year in the office and after hours in Villach. I hope we stay in contact far into the distant future. I too thank a not further disclosed artist for a song, which I had on a loop for several hundred times while writing the thesis.

My special thanks go to my family, which always supported me throughout the thesis in Villach and my whole years of studying in Leoben. It would not have been possible without you and I will be thankful for it my whole life.

Abstract

The development of new low-cost, lead-free bonding materials for interconnects in power devices is currently of high interest. Printed and subsequently thermally processed metal sinter pastes, notably Copper (Cu), have shown to form highly reliable metal-metal interconnects on a chip level, whilst taking advantage of the cost-efficient handling on a wafer level. Within the scope of this thesis, pre-selected Cu sinter pastes with different levels of porosity after a pre-conditioning with pressureless sintering were investigated in their capability to form mechanically resilient three dimensional interconnects between stacked Silicon (Si) chips through thermocompression bonding. The optimisation of the bonding process to a mild, but sufficient, process parameter set was achieved through a systematic design of experiment (DoE). In detail, the parameter set consisted of pre-conditioning, bonding temperature, bonding pressure and an optional annealing step. The formed sinter joints were assessed through a preliminary optical inspection with a light microscope and a scanning acoustic microscope. The microstructure of the sintered layer was assessed in a detailed inspection by a scanning electron microscope. The shear strength of the sinter joints was tested in a subsequent shear test and represented the decisive factor in the evaluation of the quality of the formed interconnects. The ideal process parameter set for each sinter paste was evaluated by a linear regression analysis of the DoE of the bonded three dimensional chip stacks. In summary, the processed metal sinter paste layers showed a shear strength of up to 79 MPa for thermocompression bonding with bonding process parameters of up to 400 °C and 50 MPa.

Zusammenfassung

Die Entwicklung von neuen kosteneffizienten, bleifreien Materialien für elektrische Verbindungen in Leistungselektronik ist zurzeit von hohem Interesse. Gedruckte und anschließend thermisch behandelte metallische Sinterpasten, insbesondere Kupfer (Cu), bilden metallische Verbindungen mit hoher Zuverlässigkeit auf Chip-Level, bei gleichzeitigem Vorteil der kostengünstigen Verarbeitung auf Wafer-Level. Im Umfang dieser Arbeit wurden vorausgewählte Cu Sinterpasten, mit unterschiedlichen Porositäten nach der drucklosen thermischen Vorbehandlung, auf ihre Fähigkeit zur Bildung mechanisch stabiler dreidimensionaler Verbindungen von gestapelten Siliziumchips (Si) durch Thermokompressionsbonds untersucht. Die Optimierung des Verbindungsprozesses zu milden, aber ausreichenden Prozessparametern wurde mittels eines systematischen Versuchsplans erreicht. Die Versuchsparameter waren die Vorbehandlung, die Bondtemperatur, der Bonddruck und eine optionale anschließende Wärmebehandlung. Die geformten Sinterschichten wurden in einem ersten Schritt einer optischen Untersuchung mittels einem Lichtmikroskop und einem Rasterultraschallmikroskops unterzogen. Die Mikrostruktur der Sinterschicht wurde mittels Rasterelektronenmikroskop detailliert untersucht. In einem anschließenden Schertest wurde die Scherfestigkeit der Sinterverbindungen ermittelt. Die Scherfestigkeit wurde als entscheidender Faktor für die Qualität der Sinterverbindung festgelegt. Die Evaluierung der idealen Prozessparameter für die jeweiligen Sinterpasten wurde mittels einer linearen Regressionsanalyse der DoE der gebondeten dreidimensionalen Chipstacks durchgeführt. Es konnte gezeigt werden, dass die prozessierten metallischen Sinterpastenschichten eine Scherfestigkeit von bis zu 79 MPa für das Thermokompressionsbonds mit Prozessparametern des Bondvorganges von bis zu 400 °C und 50 MPa erreichen.

List of Symbols

T_m	melting point
ρ_B	bulk density
E_n	Young's modulus
ρ_{el}	electrical resistance
κ	thermal conductivity
$\alpha_{th,n}$	coefficient of thermal expansion
G	shear modulus
ν	Poisson coefficient
Si	silicon
SiC	silicon carbide
Pb	lead
Cu	copper
Ag	silver
a_n	lattice constant
σ_{th}	thermal stress
K_B, K_p	mechanical parameters
ρ_p	density of porous body
γ	free surface energy
A	surface area
Ni	nickel
N_2	nitrogen
H_2	hydrogen
$HCOOH$	formic acid
R_q	surface roughness
ρ_{3D}^{line}	resistivity of 3D-semi infinite sample
V	voltage
I	current
F_{prod}	product of geometric factors
t_{Cu}	layer thickness of the printed copper
A_{Cu}	area of the printed copper
m_{cured}	mass after pre-conditioning
$m_{stripped}$	mass of the blank Si wafer
H_3PO_4	phosphoric acid
P	porosity
Ω_{\square}	sheet resistance
Ω	bulk resistance
psi	pounds per square inch
SF	shear force
T_C	temperature of the pre-conditioning
T_B	temperature of the bonding process
p_B	pressure of the bonding process
Ann	annealing
O_2	oxygen

List of Abbreviations

<i>BE</i>	back-end
<i>CMOS</i>	complementary metal oxide semiconductor
<i>CMP</i>	chemical mechanical polishing
<i>DIC</i>	digital image correlation
<i>DoE</i>	design of experiment
<i>ECD</i>	electrochemical deposition
<i>FAV</i>	formic acid vapour
<i>FAB</i>	fabrication
<i>FE</i>	front-end
<i>GUI</i>	graphical user interface
<i>IC</i>	integrated circuit
<i>IP</i>	inflection point
<i>IQR</i>	interquartile range
<i>MEMS</i>	micro-electro-mechanical system
<i>PCB</i>	printed circuit board
<i>PVD</i>	physical vapour deposition
<i>SAM</i>	scanning acoustic microscope
<i>SEM</i>	scanning electron microscope
<i>TCB</i>	thermocompression bonding
<i>TSB</i>	thermosonic bonding
<i>TSV</i>	through silicon via

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1 Introduction and Motivation

The development of new microelectronic applications is approaching the physical limitations of the used materials. State-of-the-art transistors reached the size limitations of Moore's Law for Integrated Circuits (ICs). The gate dimensions cannot be reduced further due to the occurring tunnelling effects. Therefore, it is necessary to implement 3D stacking into the fabrication of the applications to further progress the application performance [1].

To build such future assemblies, current standard mounting techniques on printed circuit boards (PCBs) or leadframes such as wire bonding and solder bonding have to be adapted. The main limitation of the wire bonding technique is its considerable space requirement due to the need of free-standing bond pads for the connection of ICs. Therefore, wire bonding does not allow complex multilayered structures of ICs, bound by its physical limitations in building stacked assemblies [2]. The complex 3D stacking of chips can be achieved via flip chip technologies permitted by bonding through solder bumps. Solder bumping uses eutectic systems melting at low temperatures, which forms reliable bonds between the chips, while using less surface area in relation to wire bonding. Solder bonding also has the possibility of wafer level processing. A disadvantage of solder bonding is its instability at high temperatures due to the remelting of the bonding material [3]. Substituting the low melting solder material through high melting porous sinter pastes stabilizes the bond to higher temperatures. Porous sinter layers furthermore have the potential to strengthen the bond under a thermal load.

In addition, porous metallic layers possess further benefits compared to the bulk material, which can be utilized for chip technologies. While maintaining the benefits of metals - i.e., the high electrical and thermal conductivity - the porosity of the layer lowers their Young's modulus (E_n) [4]. This lower E_n reduces the resulting thermal stress (σ_{th}) in the bonded stack arising during the operation of the chips. Furthermore, due to the lower E_n of porous metals, the product of E_n and the coefficient of thermal expansion ($\alpha_{th,n}$) is closer to the ones of silicon (Si) and silicon carbide (SiC), which reduces the risk of wafer bow during chip manufacturing. This property enables the build-up of thick metallisation layers on either the frontside or backside of a wafer without the otherwise imminent wafer bow. The inevitable current density increase through further miniaturisations of the chip area has to be compensated by higher layer thicknesses of the metallization [4].

The research question of this thesis is to determine the possibility of substituting the liquid phase solder bonding of low melting pastes through solid phase bonding with higher

temperature stability. The solder pastes are substituted with sinter pastes that form a bond through solid state sintering. The implementation of the new materials should be ideally done without massively changing the current workflow of chip mounting. The aforementioned workflow distributes the pastes through stencil printing on wafer level and realises the joint via solid state sintering by applying thermocompression bonding (TCB) [3], [5]–[8]. The solid state sinter process will be used to stack chips through the formation of solid state interconnections between the initially loose metallic particles in the sinter pastes and the metallic pads of the chips. This bonding process utilizes the atom mobility in solids above a specific temperature, which for a metal is commonly 0.4-times its melting temperature (T_m). This effect is amplified due to the high free surface energy of nano-particulate porous materials and thus can be activated well below $0.4 T_m$ [4], [9].

The supporting high temperatures and pressures of TCB for the sinter process can damage the chip stack and the IC. The establishment of an optimised bonding process including the optimisation of paste characteristics and TCB parameters is discussed within this thesis. The process parameters for different porous copper layers derived from specific copper pastes forming mechanically stable bonds are investigated and analysed in detail.

2 Fundamentals of Printed Metal Sinter Pastes

Solder pastes containing lead (Pb) will be phased out in the European Union over the next few years [10]. Therefore, alternative metal pastes are developed and implemented. Sinter pastes additionally show a higher reliability to solder pastes. The most viable metals are silver (Ag) and copper (Cu). Although these metals have higher melting points as the upper temperature range suitable for solders for microelectronics of roughly 400 °C, they can substitute Pb through the development of a reflow sinter process [11]. The substituting sinter pastes need to be compatible with current manufacturing equipment and product specifications. An overview of characteristic properties of Cu is given in Table 2.1.

Table 2.1. Properties of copper at 20 °C [12].

Crystal Structure	-	fcc
Melting Point	T_m	1083 °C
Bulk Density	ρ_B	8.96 $\frac{\text{g}}{\text{cm}^3}$
Young's Modulus	E_n	110 GPa
Electrical Resistivity	ρ_{el}	1.70 $\mu\Omega\text{cm}$
Thermal Conductivity	κ	385 $\frac{\text{W}}{\text{mK}}$
Coefficient of Thermal Expansion	α_{th}	16.4 $\times 10^{-6} \frac{1}{\text{K}}$
Shear Modulus	G	46 GPa
Poisson Coefficient	ν	0.364

The main component of metal sinter pastes is the metal powder, which can have grain sizes from nanometres (nm) to micrometres (μm). The powder is converted into a stable paste through addition of organic components. The proportion of metal powder in the paste is usually around 80 % [13]. This allows for a structured homogeneous deposition of the material on wafer level.

2.1 Fundamentals of Porous Metals

Semiconductor devices share a general trend of miniaturization. The complexity of design problems is increasing with smaller devices. The thickness of metal layers on chips needs to be raised to counter surging current densities. The current method to manufacture metal layers is by electrochemical deposition (ECD) or physical vapour deposition (PVD). The created bulk material can cause wafer bow due to its mismatch in its lattice constant (a_n), E_n , and $\alpha_{th,n}$ with respect to the substrate. The stresses that lead to wafer bow are described in Equation 1. It describes the resulting thermal stress (σ_{th}) in a body, which is proportional to the temperature change (ΔT) through E_n and $\alpha_{th,n}$ of the material. The strain stems from thermal processing.

$$\sigma_{th} = E_n \cdot \alpha_{th,n} \Delta T \quad (1)$$

The correlation of mechanical properties of the material, for example E_n , and the porosity is described in Equation 2 [14]. There, K_p and K_B are the mechanical parameters, such as E_n , of the porous and bulk material, ρ_p and ρ_B respectively are the density of the porous and bulk material, and z and t are material constants. The most facile approach to decrease the E_n of the metal layer, without major changes, is by increasing its porosity after the correlation shown in Figure 2.1.

$$\frac{K_p}{K_B} = z \left(\frac{\rho_p}{\rho_B} \right)^t \quad (2)$$

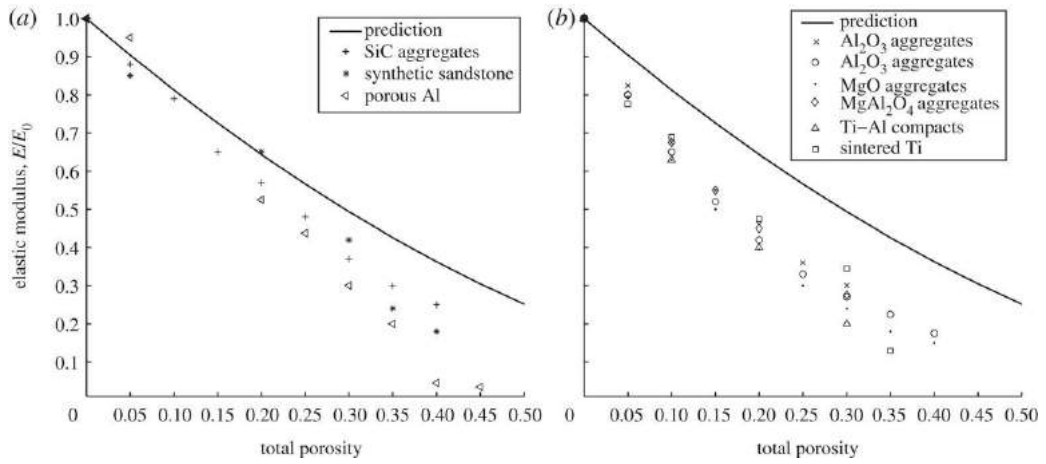


Figure 2.1. The influence of the porosity on the Young's modulus of sintered materials [4].

While maintaining the advantages of metals, i.e. high thermal and electrical conductivity, porous materials additionally offer the benefits of lower stresses in multilayer stacks and higher specific surface area for heat dissipation.

Porous metal layers are mostly manufactured through powder metallurgy processing routes. The particles of the powder are transferred into a solid metal body through solid state sintering. Sintering is a diffusion driven process of solid state particles at processing temperatures below the melting point of the material. The driving force behind the sinter process is the reduction of the specific surface energy (γ) by replacing solid-vapour interfaces with solid-solid interfaces, thus reducing the free surface area (A) of the sintered particles. Equation 3 describes the two main mechanisms active throughout the

sinter process [8]. The total surface energy ($\Delta(\gamma A)$) is reduced by densification, which is described by the term ($\Delta\gamma A$), and coarsening, which is described by the term ($\gamma\Delta A$).

$$\Delta(\gamma A) = \Delta\gamma A + \gamma\Delta A \quad (3)$$

Solid state sintering requires clean surfaces and inert or reducing atmospheres, as the surface energy of solids is small in comparison to the Gibbs energy of metal oxide formation. The surface energy is in the range of $0.5 \frac{\text{J}}{\text{mol}}$ to $500 \frac{\text{J}}{\text{mol}}$, whereas oxide formation usually occurs between $300 \frac{\text{kJ}}{\text{mol}}$ and $1500 \frac{\text{kJ}}{\text{mol}}$ [8]. The surface energy increases with decreasing particle size. The solid-state sintering process consists of three main stages, as shown in Figure 2.2. The initial stage covers neck formation with marginal densification of the compound. The dominating fraction of densification occurs in the intermediate stage up to the formation of isolated pores. In the final stage, marginal densification happens through shrinkage of the isolated pores.

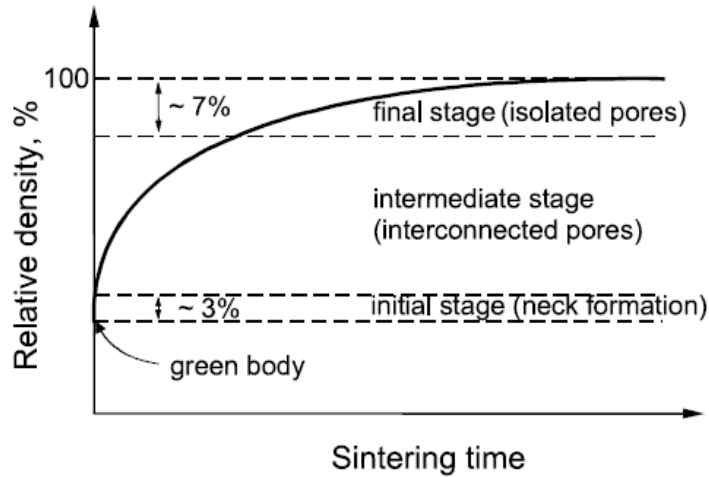


Figure 2.2. Progression of relative porosity over sintering time for solid state sintering [8].

The material transport mechanisms of solid state sintering can be classified into two categories. These categories cover mechanisms which contribute to densification and those which do not densify the material. Figure 2.3 visualises the six main material transport mechanisms governing the sinter process.

Only those mechanisms numbered 4 to 6 in Figure 2.3 contribute to the densification of the porous body. These mechanisms transport material from the bulk to the sinter necks. The mechanisms numbered 1 to 3 transport material from the surface to the sinter neck, which does not result in densification of the sinter body.

The mechanisms active during the sintering process are defined by their path from the initial state of the material in its higher energetic potential, to the final state in its lower energetic potential [6]–[8]:

1. *surface diffusion (mechanism 1 in Figure 2.3)*: The transportation through surface diffusion will migrate atoms from the convex surface of the particle to the concave surface of the sinter neck. Surface diffusion is driven by vacancy mechanisms along the surface and the difference in the chemical potentials of the surfaces with different curvatures. It is the dominant form of diffusion for low- to mid-range temperature steps.
2. *lattice diffusion from the surface (mechanism 2 in Figure 2.3)*: The lattice diffusion from the surface has the same driving force as the surface diffusion. It utilizes the transportation through vacancy mechanisms in the crystal lattice, as against on the surface for surface diffusion.
3. *vapour transport (mechanism 3 in Figure 2.3)*: The driving force for the vapour transport is the vapour pressure difference of the high pressure convex surface of the particle and the low pressure concave surface of the sinter neck through evaporation and condensation.
4. *grain boundary diffusion (mechanism 4 in Figure 2.3)*: The transportation of atoms along the grain boundary is driven by similar mechanisms as surface diffusion. The driving force for the grain boundary diffusion is the reduction of surface energy in the concave sinter neck. Its activation energy is smaller than other diffusion mechanisms, because vacancies can be trapped at the grain boundary. The grain boundary diffusion is comparable to Coble creep, which describes the diffusion controlled creep mechanism, driven by vacancies, along the grain boundary in solids [9]. It is also the driving mechanism behind grain growth due to the excess surface energy on the grain boundary.
5. *lattice diffusion from the grain boundary (mechanism 5 in Figure 2.3)*: The diffusion from the grain boundary through the crystal lattice is driven by vacancy annihilation. It is comparable to Nabarro-Herring creep, which describes the diffusion controlled creep mechanism, driven by vacancies, through the crystal lattice in solids [9]. The atom transport is from the grain boundary, which is an area under compressive stress, to the concave sinter neck, which is under tensile stress.

6. *plastic flow (mechanism 6 in Figure 2.3)*: The plastic flow is comparable to the high temperature creep under constant strain in bulk materials [9]. Its driving force is the formation of dislocations, which will migrate atoms to the concave surface of the sinter neck.

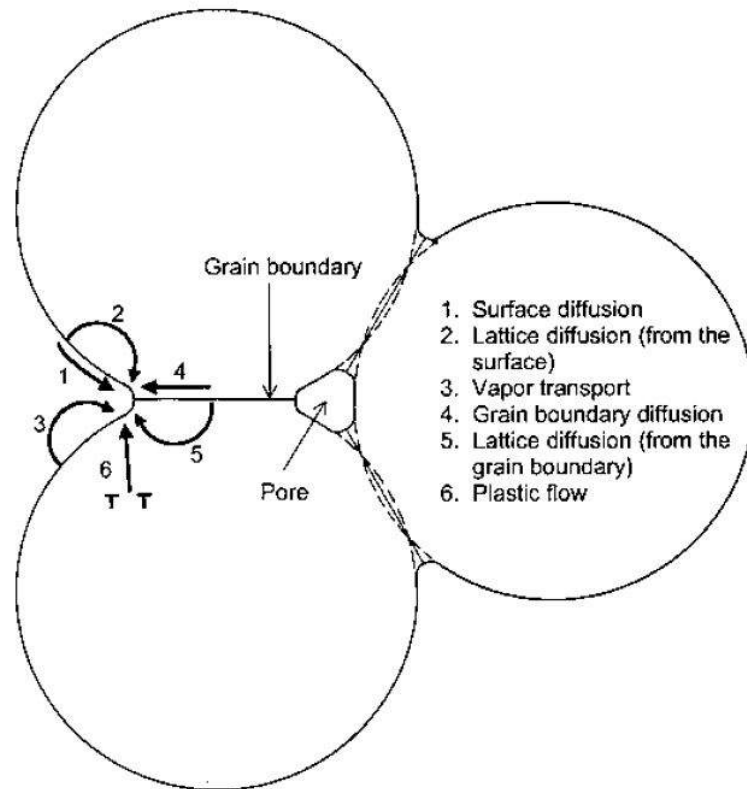


Figure 2.3. Schematic illustration of mechanisms in solid state sintering [6].

2.2 3-D Integration on Wafer- and Chip-Level

The assembly of a semiconductor device in back-end (BE) can represent more than 50% [15] of its overall production cost. A major cost contributor is the single chip handling of BE processes while assembling the final product. The transfer of process steps on chip level in BE onto wafer level in front-end (FE) before dicing has therefore an enormous potential for cost reduction. Traditional wire bonding stacks take up considerable space and have strong limitations in their complexity. A major cost reduction and possibility for more complex structures can be achieved by their substitution through modern bonding techniques.

The limits of Moore's law are reached in the development of next generation ICs in the area of the Internet of Things (IoT). The integration of the third dimension is necessary to allow for an additional miniaturisation on chip level. This can be achieved through

wafer-on-wafer bonding, chip-on-chip bonding and chip-on-wafer bonding. The stacking of ICs can be done through metal-to-metal TCB, through silicon vias (TSVs) and wire bonding [5]. Metallic bonding represents the most advantageous process for producing hermetically sealed cavities of Micro-Electro-Mechanical Systems (MEMS), showing the lowest gas transition through the cavity [16]. TCB of flip-chip technologies allows finer interconnect structures than traditional wire bonded assemblies. It also allows to build-up a multilayer stack on small areas in combination with TSVs [3]. The reduction in base area for a 3-D stack using metallic bonding and TSVs in relation to wire bonding is demonstrated by Figure 2.4. Figure 2.4a shows the traditional wire bonding concept, which needs additional bond pads on the carrier board. The stack, depicted in Figure 2.4b, utilizing thermocompression metallic bonding and TSVs, is narrowed to the size of the bonded top chip stack, while additionally allowing more complex build-ups.

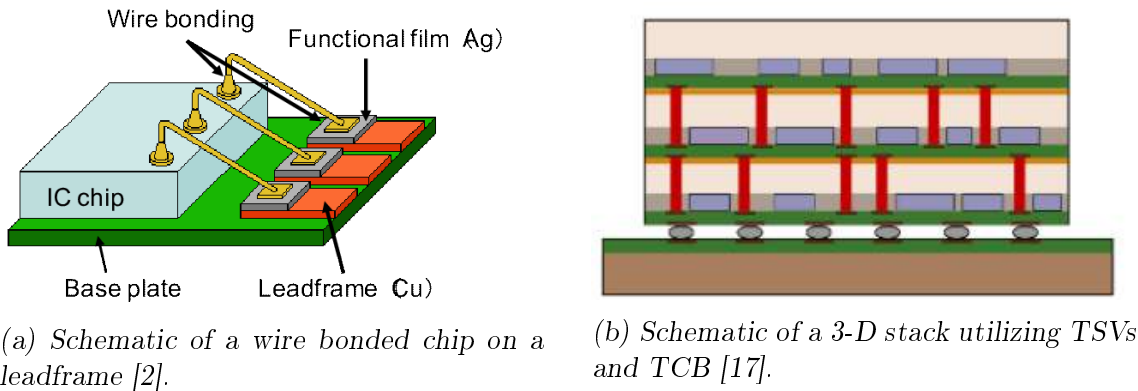
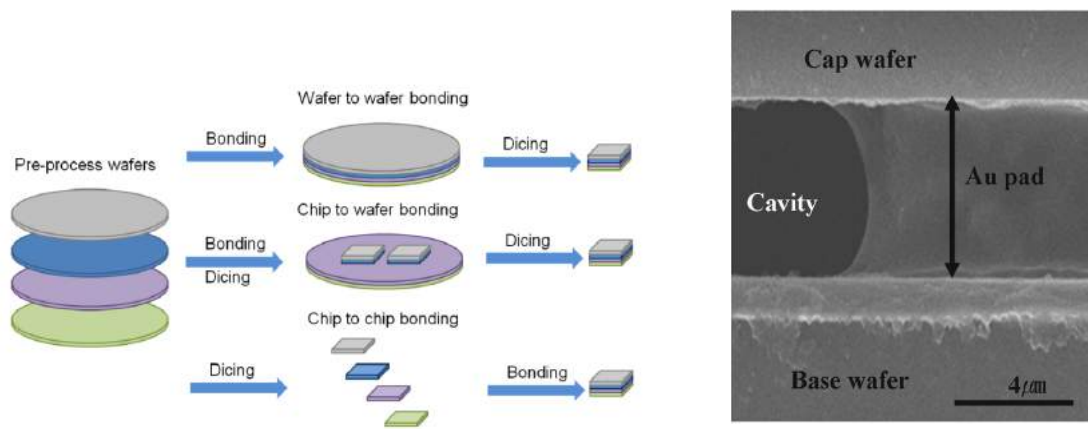


Figure 2.4. Schematic correlation of wire bonding and chip stacking with TSVs and TCB.

2.2.1 Thermocompression Bonding on Wafer- and Chip-Level

TCB is a solid-state welding process below the melting point of the metal [18]. It uses the combination of heating and mechanical pressure to connect two metal surfaces which are in contact. It is the main principle behind wire bonding and can be scaled up to direct bonding of two metallic surfaces on wafer level [2]. The limitations of the process are the temperature, the applied pressure and the cleanliness of the surface. The product of these parameters defines the bonding process of the two surfaces. The temperature of processing steps for Complementary Metal Oxide Semiconductor (CMOS) devices should be kept low to limit diffusion of the doped regions [19]. The temperature can be lowered by applying higher pressure [18]. However, this increases the probability of chip cracking. The parameter set has to be selected at a level which guarantees a bond between the surfaces without damaging the devices. The mandatory product of temperature and pressure is lower for porous materials in relation to their bulk due to the higher free surface energy, caused by their increased surface area. Metallic surfaces with oxides or

contaminants necessitate an aggravated parameter set for the bonding process. TCB can be applied on wafer- and chip-level. The bonding parameters temperature ($^{\circ}C$) and bonding pressure (MPa) have no relation to the size of the bonded area. The bonding of full face wafers [20], structured wafers [18], [21], [22] and single chip stacking [17], [23] are being developed and implemented into fabrication (FAB) workflows. The schematic of a chip-scale TCB substituting solder bumps can be seen in Figure 2.5. Figure 2.5a shows the different scales of the TCB process. The bonding process can be achieved before and after dicing of the wafer, depending on the used tools in the FAB workflow. Figure 2.5b shows the resulting stack for the bonding of structured wafers to achieve a mechanical bond forming a hermetically sealed cavity for MEMS devices.



(a) Schematic of the TCB process on different scales [22]. (b) Cross section of a hermetic cavity produced via TCB [18].

Figure 2.5. Schematics for TCB substituting solder bumps for mechanical and electrical connections.

2.3 Stencil Printing and Paste Conditioning

Stencil and screen printing are used since ancient times. The use for the semiconductor industry started in the 1960s via depositing conductive interconnects [24]. Printing is commonly used to deposit solder paste for bump formation for flip-chip stacks. Presently, the demands set onto interconnects in wafer stacks are increasing beyond the limits of standard solder pastes. Metallic sinter pastes are developed to substitute solder bumps [25]. Metallic pastes require organic additives to protect the particles from agglomeration and oxidation. Due to their composition, the pastes demand additional steps for mechanical and chemical conditioning. Mechanical conditioning by stirring the paste before deposition is necessary to prevent agglomerates. Chemical conditioning is used to remove organic segments in the deposited paste layer. Customarily, chemical condition-

ing is achieved by thermal treatments in different atmospheres. Additional cleaning steps through chemicals could be promising.

2.3.1 Fundamentals of Wafer Level Printing

Stencil printing was adapted from screen printing, while missing the woven mesh of the screen printing mask and utilizing only suitably placed holes in the metal mask. Stencil printing was implemented into FAB processes in the 1960s. By 1999 it was applied in over 90 percent of BE semiconductor fabrications [24]. The advantage of stencil printing is the deposition of structures on wafer level in a single fast process step, as illustrated in Figure 2.6, which leads to significant cost reductions, making the process ideal for low-cost high-volume assemblies. The structured stencil is positioned with respect to the substrate to be printed by aligning the fiducials of the wafer and the stencil. This step is depicted in Figure 2.6a. The paste is placed on the aligned stencil and deposited onto the substrate, through the structured stencil, by moving the paste with a squeegee over the structures, as shown in Figure 2.6b. The final result, depicted in Figure 2.6c, after removing the stencil is the structured deposition of the paste on the substrate.

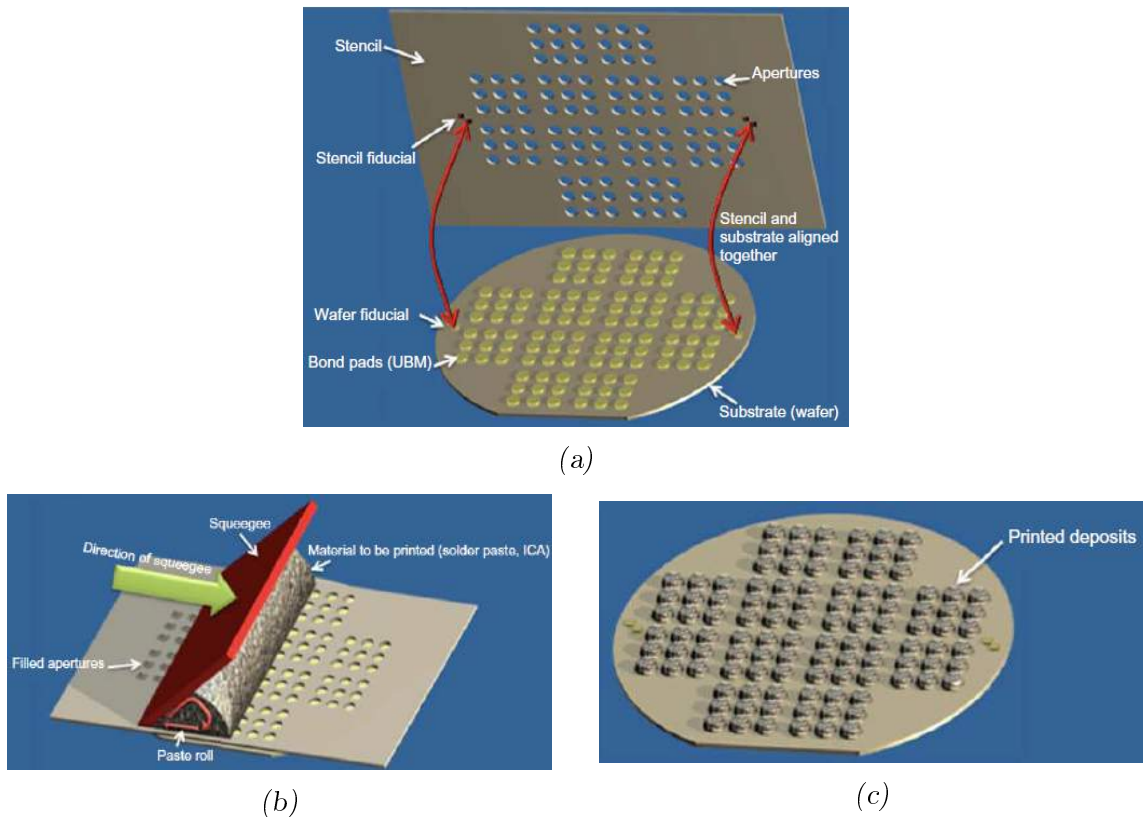


Figure 2.6. Schematic process flow of a stencil print: By aligning the stencil through fiducials (a), the paste is deposited onto the substrate (b) at the desired positions on a wafer level in a single step (c) [24].

The stencil structure can be chemically etched, electroformed or in most cases laser cut. Standard materials for the stencil are nickel (Ni) or stainless steel. Stencil printing allows structured depositions down to a pitch size of $80\ \mu\text{m}$ [26]. The dominant effects on the printing quality are the rheological properties of the deposited material, the quality of the stencil, and the chosen print parameters [24].

A new development for the deposition of metallisations on wafer level is the combination of metal paste and the mounting tape used for handling and sawing of the wafer. Paste pre-deposited onto the tape is transferred onto the wafer in a pre-conditioned state. The wafer is cut after being mounted on the tape and single chips can be picked for the bonding processes [27]. The pick-up process of a single chip with a deposited metal layer from the tape is shown in Figure 2.7.

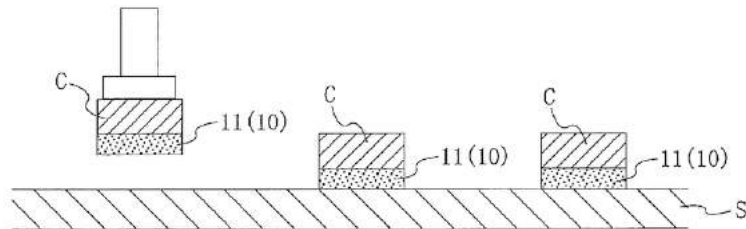


Figure 2.7. Schematic illustration of a pick-up process of single printed chips $[C]$ with a pre-deposited metal layer $[11(10)]$ from the dicing tape $[S]$ [27].

2.3.2 Paste Conditioning under Reductive Atmosphere

Metal sinter pastes, which were used in this thesis, contain organic fractions of up to 20 wt% [13], which have to be removed from the final product. Depending on the used additives, different atmospheres are needed during thermal processing to guarantee sintering of the metal particles and to prevent oxidation. The organic fraction of the paste consists of additives that prevent coagulation and oxidation of the untreated metal particles [13]. Self-reducing pastes include components which disintegrate and form a reducing atmosphere [28]. These pastes only need an inert atmosphere during the curing process, mostly consisting of nitrogen (N_2). Pastes lacking self-reducing ingredients have to be processed in reducing atmospheres. This is commonly done by adding hydrogen (H_2) or formic acid ($HCOOH$) to the inert atmosphere.

The parameters of the thermal treatment are set depending on the metal and the organic additives in the paste. Studies have shown that a pressureless pre-conditioning of the pastes increases the bond quality [29], [30]. The organic components can be removed easier during the pre-conditioning, as the sinter layer surface is not covered by the wafer

stack. The sinter layer stays active by setting the curing temperature at a level that only allows sintering without volume shrinkage and by continuing the bonding process at elevated temperatures and applied pressure.

2.3.3 Chemical Conditioning of Copper Sinter Pastes

Long term stability of the printed layers is crucial, as an in-situ workflow cannot be guaranteed during industrial production. The removal step of organic additives is important for Cu pastes because of the affinity of Cu to oxidise during the workflow. If the additives are removed too early in the process chain, the sinter layer will tend to oxidise. Therefore Cu pastes contain more organic additives than pastes of more noble metals. If the additives are not volatile enough, they will remain in the sinter layer and contaminate the metal. For sinter pastes containing organic residues which cannot be fully removed during the pre-conditioning, additional cleaning processes are necessary. The organics can redeposit on the surface and prevent subsequent bonding processes. The passivation of Cu layers to prevent their oxidation is achieved by depositing monolayers on their surface. The monolayers are desorbed in a thermal step before the bonding process [22]. Examples for removing surface oxides of copper are by chemical removal [22], [31] or by plasma cleaning [32]. Up to the knowledge of the author, there is no literature available on the removal of organic residues from printed sinter layers, only on general cleaning processes on wafer level for organics. However, the use of a plasma asher for the removal of organics is implemented on an industrial level [33]. Reduced surfaces need to be processed in inert atmospheres to prevent re-oxidation. The surface can be passivated through chemical processing, which reduces the surface oxides and forms a protecting passivation layer of thermally decomposable functional groups on the exposed surface [34]. The need of additional cleaning processes can be prohibited by including reducing agents within the additives of the metal pastes. The additives reduce the metal oxides during the sinter process. The in-situ reduction of self-reducing pastes permits bonding processes without pre-conditioning of the deposited layer at elevated temperatures and in reactive atmospheres [13], [35].

2.4 Fundamentals of Surface Interactions for Thermocompression Bonding

The bond strength of the sintered metal layer in the assembly is defined by the properties of the contacting interfaces. TCB, as a diffusion driven process, needs high temperatures. High temperatures on the other hand should be avoided to prevent damaging the assembly. To guarantee a strong bond at low temperatures, the bonding interface has to be free of contaminations and natural oxides. Copper is very susceptible to the formation of surface oxides, which can hinder diffusion processes during TCB. The removal of native oxides and a surface activation step can significantly reduce the bonding parameters and minimize the thermal and mechanical stresses on the assembly [36].

Metallic bonding of two surfaces is achieved by joining the interfaces through solid-state processes, obtained via interdiffusion and grain growth surpassing across the interfaces [37]. The bonding process between two surfaces is fundamentally defined by their roughness and chemical purity. The bond strength decreases with increasing impurity content of the metal layer [38]. The natural surface oxide on Cu surfaces can prevent the bonding of Cu-Cu interfaces if not removed before the TCB process [5]. The surface roughness (R_q) defines the initial contact area of the bonding process, whereby coarse surface regions can lead to voids in the bonded interface [39]. The R_q of comparatively smooth surfaces can be offset through the plastic deformation of surface asperities during the TCB process. The deformation capability is affected by the pre-conditioning of the samples. Further, the bond resulting through the TCB process is influenced by the applied bonding pressure, the bonding temperature, the duration of the thermal treatment and the ambient conditions [37]. The surface oxide can be removed by chemical cleaning, as described in Section 2.3.3. Significantly higher bond strengths can be achieved by removing the surface oxide and performing the bonding process under inert atmosphere. The R_q of the bonding interface can be reduced by chemical mechanical polishing (CMP) [5]. There, the interface is planarized through mechanical abrasion, supported by a chemically active slurry [40].

3 Experimental Setup and Results

3.1 Preliminary Work

Within the project wherein this thesis was written, preliminary investigations performed earlier were continued. The results of these earlier investigations are mentioned continuously, as they are compared with the new data obtained within this thesis.

These preliminary investigations include the paste characterisation of two copper sinter pastes, CP1 and CP2 [41]. CP1 and CP2 are micro-nano pastes with different additives from the same supplier. The characterisation workflow of Dietz [41] as described in Section 4.1 to 4.4 was continued for the paste CP3, which is described in this work. CP3 is a nano paste from a new supplier.

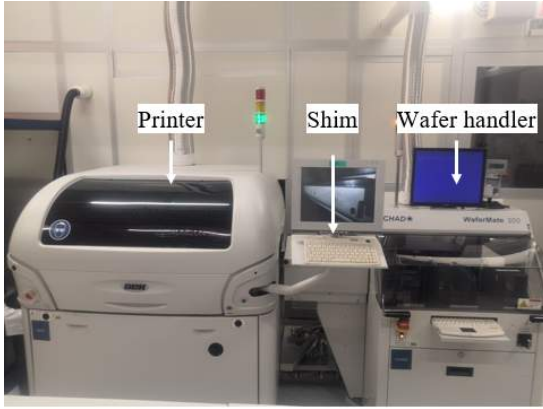
The Design of Experiments (DoE) for the bond tests was already established in the work of Karner [42] for CP1. The DoE table as described in Section 5 for the sample preparation was applied to CP2 and CP3 in this work. The interpretation of the shear test results with the software CEDA Cornerstone was also established by Karner [42] and continued for all DoEs. The program is described in Section 3.2.5 and the evaluation process in Section 5.2.

3.2 Work Environment

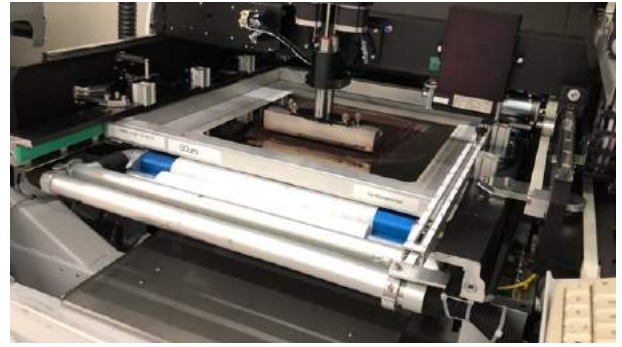
This section describes the materials and machinery used throughout the preliminary preparation steps, up to the build-up and testing of the final die-bonded samples. The wafer printer, single-wafer furnace and fineplacer are described in detail.

3.2.1 Paste Deposition

The paste deposition of all studied materials was done with the semi-automatic stencil printer DEK Horizon 02i [43]. This printer can handle screen and stencil printing. The wafers are fed to the printer by the wafer handler CHAD WaferMate 200 [44], which provides one wafer at a time to the printer on a vacuum stage. The stage is fit with a shim to center the wafer, depicted in Figure 3.1. Within this thesis, only stencil printing is performed. The stencil is a structured metal plate, in the thickness of the final deposited material. The printing process is done via manually depositing the paste on a stencil and dispersing the material homogeneously through the structures by automated squeegees moving over the stencil with predefined pressure. The shear viscosity of the pastes is controlled through the print velocity.



(a) Overview of the stencil printing setup.

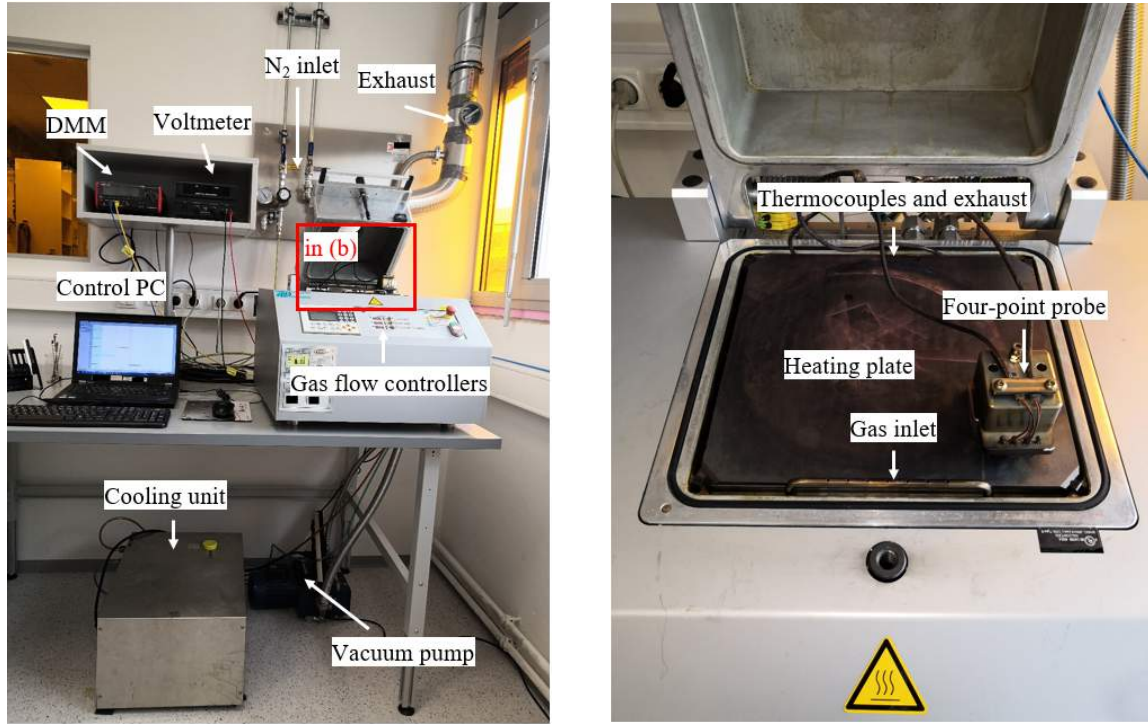


(b) Paste deposition trough stencil printing.

Figure 3.1. Setup of the DEK Horizon 02i stencil printer and CHAD WaferMate 200 wafer handler.

3.2.2 Thermal Processing

After printing, the paste material is defined as being in a "wet" state. To reach a processed metal layer, the wafer has to undergo a variety of thermal processes. The first thermal step is performed immediately after the printing process, by drying the wafer in the YES-11C high vacuum oven by Yield Engineering System [45]. This step is performed in the clean room at a constant temperature of 100 °C. This ensures the evaporation of solvents present in the pastes. At this state the printed layers are permanently stable and can be stored for long periods. The curing process, which can on occasions be separated into different curing steps, was done with the ATV SRO700 single-wafer furnace by ATV Technologie GmbH [46], which can be seen in Figure 3.2. The furnace can process the wafer up to 450 °C under vacuum, down to 5 mbar, or in inert (N_2) or reductive ($N_2/HCOOH$) atmosphere. The formic acid ($HCOOH$) will disintegrate organic compounds in the metal paste after decomposing into water and carbon monoxide or hydrogen and carbon dioxide at elevated temperatures.



(a) Setup of the single-wafer furnace.

(b) Process chamber of the ATV SRO700.

Figure 3.2. Setup of the ATV SRO700 single-wafer furnace.

During the curing process, the sinter curve is recorded by an in-situ four-point measurement head by T.I.P.S. Messtechnik GmbH [47]. The inflection point (IP) shows the temperature with the highest slope of the voltage curve as a consequence of the growth of sinter necks. This temperature is defined as the minimum sinter parameter.

A common curing process for copper pastes is visualised in Figure 3.3. The figure depicts the temperature over time of the furnace program. The multi-step curing process consists commonly of:

- evacuation of the chamber to 5 mbar to prevent an oxyhydrogen reaction;
- heating to 100 °C under vacuum to prevent non-evaporated FAV;
- heating to the maximum curing temperature under reductive atmosphere;
- optional plateau step to anneal the metal layer;
- maximum cooling to room temperature.

The standard curing processes for the characterised and tested copper pastes have no plateau step at maximum temperature. This is done to generate a reactive state, which allows later TCB tests, utilizing sufficient reactivity of the metal layer to form a strong bond between dies.

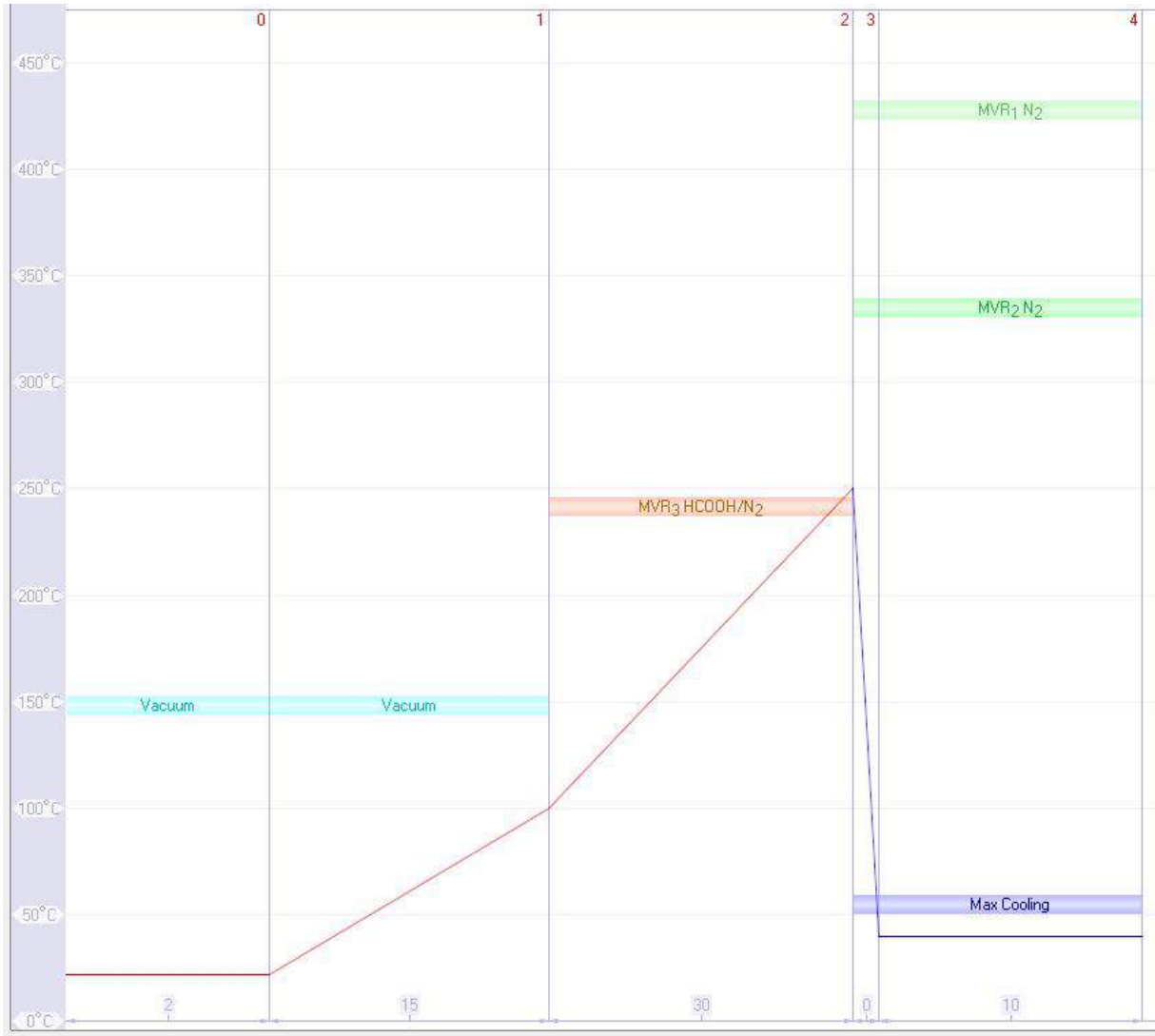


Figure 3.3. Standard furnace process for sinter paste curing. The set atmospheres of the steps are colour coded in the figure. (N_2) is coded in green, (FAV/N_2) is red, vacuum is cyan and maximum cooling is blue. The axes of the furnace process are not depicted to scale.

3.2.3 Bonding Tool

The bonding tests are done by a project partner on the Fineplacer Lambda by Finetech GmbH [48] depicted in Figure 3.4. The fineplacer can handle single dies, which are placed and bonded on a substrate with a bond force of up to 200 N. Both, substrate table and fineplacer, are temperature controlled up to 400 °C. The cooling of the system is achieved by a flow of pressurized air. The bonding process is performed under inert atmosphere (N_2), but additional modules to provide reductive atmospheres (N_2/H_2 or $N_2/HCOOH$) are available.



Figure 3.4. Fineplacer setup to prepare die bonded samples.

3.2.4 Analytical Equipment

3.2.4.1 The Four-Point Probe

The resistance of solid state matter can be precisely measured with the four-point probe technique. For the linear aligned four-point probe, depicted in Figure 3.5, the voltage drop on the inner two contacts can be measured for a constant current set on the outer two pins, allowing to calculate the surface resistance of the measured sample. The resistance of an ideal 3D-semi infinite sample measured with a linear four-point probe is given by Equation 4 [49]

$$\rho_{3D}^{line} = 2\pi s \frac{V}{I} \quad (4)$$

where s is the distance between between two pins, V the voltage drop on the inner two pins and I the applied current on the outer two pins.

For an arbitrary shape of isotropic thin films, as measured in Section 4.2, the resistance can be formulated after the Van-der-Pauw theorem [50] into Equation 5 [49]

$$\rho_{el} = F_{prod} \frac{V}{I} \quad (5)$$

where F_{prod} equals the product of the geometric factors F_1 , F_2 and F_3 , which approach 1 for ideal test geometries. F_1 is the ratio of pin distance to layer thickness; F_2 is the ratio

of the pin distance to the distance of the setup to the sample edge; and F_3 is the ratio of sample size to the distance of the outer pins. The ideal geometry is a very thin layer, has a sufficiently large distance to the edge and an overall large sample size.

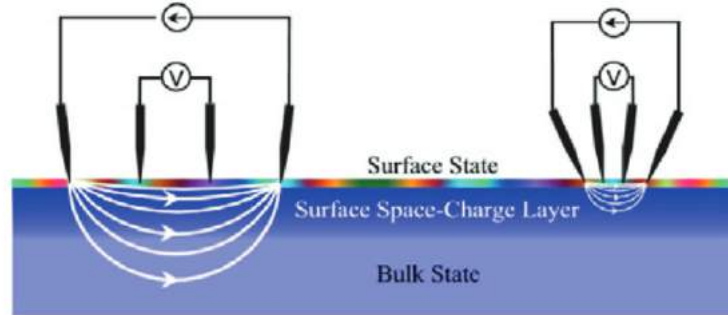


Figure 3.5. Schematics of a four-point probe measurement [51].

3.2.4.2 Additional Equipment

The variety of analytical equipment for the paste characterisation is described in Appendix A in further detail. The list of used tools is as follows:

- **optical microscope [52]:** optical analysis, pre- and post-bonding;
- **scanning electron microscope (SEM)[53]:** structural analysis, pre- and post-bonding;
- **optical profiler [54]:** surface roughness and layer thickness measurement of printed layers;
- **ResMap [55]:** sheet resistance measurement of printed layers;
- **etch bath:** gravimetric porosity determination of the samples;
- **Auger electron spectroscopy [56]:** organic residue detection in the processed samples;
- **surface acoustic microscope (SAM) [57]:** bond quality assessment of dies;
- **shear tester [58]:** shear strength measurement of bonded dies.

3.2.5 Design of Experiment

The Design of Experiment (DoE) is done with a program named CEDA, which is an Infineon-specific Graphical User Interface (GUI) of the commercially available program "Cornerstone" [59], which itself is based on the programming language R [60]. A full DoE

with k continuous or categorical independent parameters consists of 2^k samples [61]. The program analyses the data of the measured samples, weighs the contribution of individual effects and calculates interactions between the input parameters. With these data, the program can predict relevant experimental parameters and their interaction trends regarding the resulting linear model fit. The experimental parameters and interactions can be analysed to define probability values (p-values) [62] of statistical relevance for the measured results. The conventional limit for relevant parameters is set at a probability value of 0.1. At this value, the probability of a statistical relevance is 90%. The interaction trends can be displayed graphically in ordered bar graphs, called Pareto charts [63]. The single effects are displayed as bars in the order of their weight, starting with the most influential positive interaction down to the most negative [63]. The influence of the interaction is depicted by its absolute value. A negative value defines an indirect interaction. The variance of measured values is best shown in so-called box plots [64].

3.2.5.1 The Significance Table

The significance table is an output of the CEDA analysis for a DoE. The table lists the terms of the linear regression with the calculated p-values for the orthogonally scaled linear regression of the DoE. The terms are the constant, the independent experimental parameters of the DoE and the interactions of the individual parameters. The p-values are colour coded due to their significance in the significance table, as can be seen in Table 6.3 in Chapter 6.2. Significant terms are coloured green and yellow. Insignificant p-values above the threshold of 0.1 are coloured in shades of blue. The terms considered for the linear regression of the system are coloured solidly. Independent terms with a p-value above 0.1 are included if a higher grade interaction of the term is considered for the linear regression analysis.

The fitting of the linear regression model is done through the least square method [65]. The coefficient of determination, R-square, describes the error of the fitted polynomial to the measured values. The error of the polynomial is called residual. The coefficient describes the variance of the independent variables in the system. The R-square of a fitted polynomial is calculated after Equation 6. R-square is the fraction of the sum of explained variances of the sum of the overall variances [66]. The explained variance is defined as the residual at the i^{th} point of the computed regression polynomial (f_i) to the mean value of all n measurements (\bar{y}). The overall variance is defined as the residual at the i^{th} point of the measured value (y_i) to the mean of all n measurements. An R-square value close to 1 with a low root mean square (RMS) error suggests a good model fit.

$$R^2 = \frac{\text{explained variance}}{\text{overall variance}} = \frac{\sum_i^n (f_i - \bar{y})^2}{\sum_i^n (y_i - \bar{y})^2} \quad (6)$$

3.2.5.2 Multi-variable Linear Regression

The CEDA analysis of a DoE computes a linear regression model for the independent parameters to fit the measured values. The analysis uses a multi-variable linear regression with the format of Equation 7. The equation describes the fitting of the dependent parameter (y), which relates to the measured values, through the constant (C) and the independent parameters (x_i) multiplied by the regression coefficient of the parameter (a_i). The regression coefficient describes the individual influence of the independent parameter on the dependent parameter [66].

$$y = C + a_1x_1 + a_2x_2 + .. + a_nx_n \quad (7)$$

The measurement set should be broad enough to allow a reliable model fit through a overdetermined system. Including irrelevant parameters in the model increases the fit for the measurement set, but decreases the overall fit of the model for measurement predictions. Therefore the model is filtered for relevant parameters. The selection of relevant parameters is done by computing either a NULL-model, including no independent parameters, or by including all independent parameters in a full model. The independent parameters are characterised by individually including or excluding the parameter in the computed systems and checking for an increase of fit for the model system to the measured values [66].

4 Paste Characterisation

The investigated copper pastes are provided by an external distributor. Within the previous works [41], [42], many general paste characteristics have already been established. The main goal of the characterisation of further pastes is to integrate pastes, which generate metal layers with a wide range of porosities and physical properties. The already established paste CP1 serves as a setpoint with a medium porosity of roughly 32%. The particle size distribution of CP1 covers nano- to micrometres. Subsequently introduced pastes are based on micro, micro-nano and pure nano-particles, mixed with different additives. The highly porous paste, denoted CP2, consists of micro-nano particles and was characterised within previous work [41], but not investigated in a bonding DoE. The paste here called CP3 is a pure nano-particle paste. CP3 has a porosity similar to CP1 [30].

4.1 General Appearance and Printability

Since the printing viscosity of the pastes varies, according to the distributors, between 6 Pa s and 200 Pa s, the overall appearance and easy-handling of the tested pastes is of high importance. Depending on the additives added to the copper particles, the pastes show different characteristics regarding homogeneity and long term stability. The ideal paste does not agglomerate over time; is easily distributable, while not dripping; and shows shear viscous behaviour during the printing process. According to the distributor, CP3 shows an ideal viscosity of 20 Pa s during the printing process. CP3 presents no loss in quality after long term storage in empirical observations within the thesis. The viscosity of CP1 varies depending on the modification between 30 Pa s and 80 Pa s and the viscosity of CP2 is 10 Pa s, as recorded by the distributor. All viscosities are specified for a shear rate of $50 \frac{1}{s}$. Some discarded pastes experience segregation of copper and additives, which results in dried flakes that worsen the print results. CP3 shows a very smooth, reflective surface, which is confirmed by R_q measurements using the optical profiler. The R_q was measured on pre-conditioned wafer quarters of the printed copper pastes, as depicted in Figure 4.3 in its dried state. The R_q -values were $1.84 \mu\text{m} \pm 0.09 \mu\text{m}$ for CP1 and $2.56 \mu\text{m} \pm 0.36 \mu\text{m}$ for CP2, while CP3 has an R_q of $0.11 \mu\text{m} \pm 0.03 \mu\text{m}$. The box plot depicted in Figure 4.1 shows the median R_q and the interquartile range (IQR), which encloses the middle 50% of the measured values of the pre-conditioned wafer quarters. The box plot additionally depicts the whiskers and outliers, marked as red dots, of the statistical analysis. The median R_q of the pre-conditioned wafer quarters were $1.84 \mu\text{m}$ for CP1, $2.52 \mu\text{m}$ for CP2 and $0.10 \mu\text{m}$ for CP3. The calculated IQR of the measurements were $0.10 \mu\text{m}$ for CP1, $0.41 \mu\text{m}$ for CP2 and $0.02 \mu\text{m}$ for CP3.

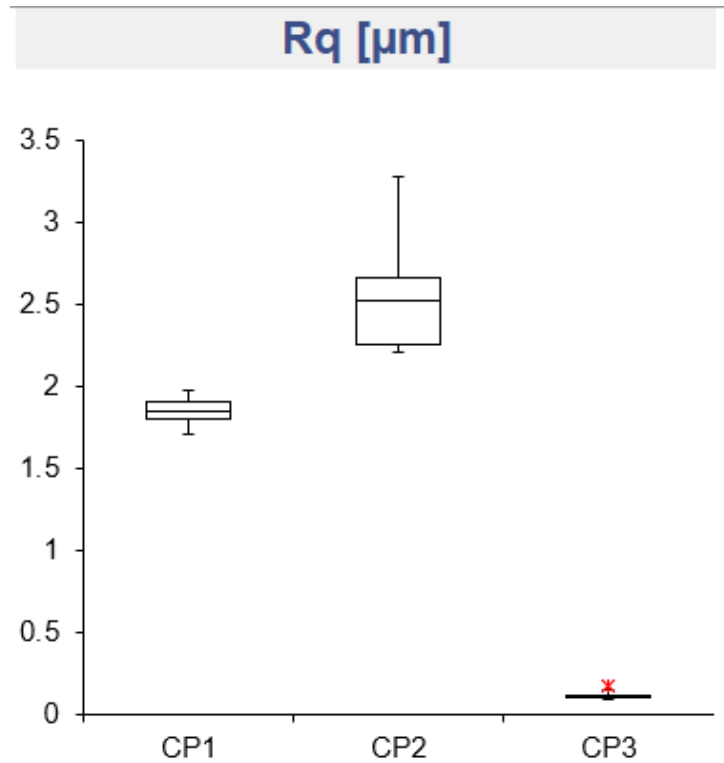


Figure 4.1. Box plot of the measured R_q of printed copper pastes after pre-conditioning with the standard curing program up to 400 °C and a plateau step of 0 s.

4.2 Sinter Properties

The sinter behaviour is investigated by in-situ measurements with a four-point probe. The probe is placed on the printed wafer and monitors the voltage with an applied constant current of 1 A over a default curing program up to 400 °C. The resulting graph of this measurement, depicted in Figure 4.2, shows a steep decline over a small temperature window. The inflection point (IP), which is defined as the point of interest for sintering, is located in this window.

The IP for CP3 is at 159 °C [30]. The sinter range indicating neck growth reaches from 150 °C to 180 °C [30], where the resistance shows a plateau. The IP for CP1 is at 165 °C [30] and for CP2 at 182 °C [30], with respective plateaus starting at 225 °C [30] and 275 °C [30]. The measurements are interpreted qualitatively to identify the relevant temperature ranges for the curing of each paste.

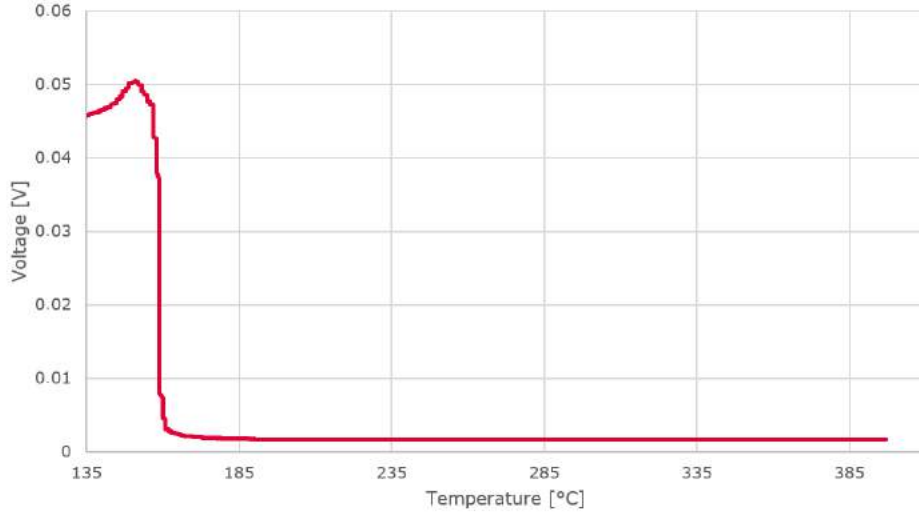


Figure 4.2. Change of voltage during sintering of the CP3 paste over temperature.

4.3 Porosity Estimation

The printed wafers are prepared by scratching a rectangular pattern of the dimensions $40\text{ mm} \times 40\text{ mm}$ to create a step between the substrate and the surface of the printed structure, depicted in Figure 4.3. The samples are cured with the furnace program "400_000", which is defined as a default program with a maximum temperature of 400°C and a plateau step of 0 s. The scratches in the cured wafer are used to measure the layer thickness t_{Cu} of the deposited paste with the optical profiler, while R_q is determined in the enclosed area using the same device. The area A_{Cu} of deposited paste on the sample is measured with the software ImageJ [67] to calculate the volume of deposited copper. The cured sample is weighed (m_{cured}) and then stripped of Cu by putting it in a phosphoric acid (H_3PO_4) bath. The stripped Si-wafer is weighed again ($m_{stripped}$) to determine the mass of stripped copper. By measuring volume and mass, the calculated density ρ_p in relation to bulk copper (ρ_b) implies the porosity P of the layer. The calculated porosity P of CP3, derived according to Equation 8, is $17.6\% \pm 1.2\%$. A 2D image analysis by Wijaya provided a porosity of $33.3\% \pm 3.8\%$ [30] for CP3. The porosities of CP1 and CP2 are measured as $31.7\% \pm 2.3\%$ [30] and $57.5\% \pm 2.9\%$ [30], respectively.

$$P = \frac{\rho_p}{\rho_b} = \frac{m_{cured} - m_{stripped}}{A_{Cu} * t_{Cu} * \rho_b} \quad (8)$$

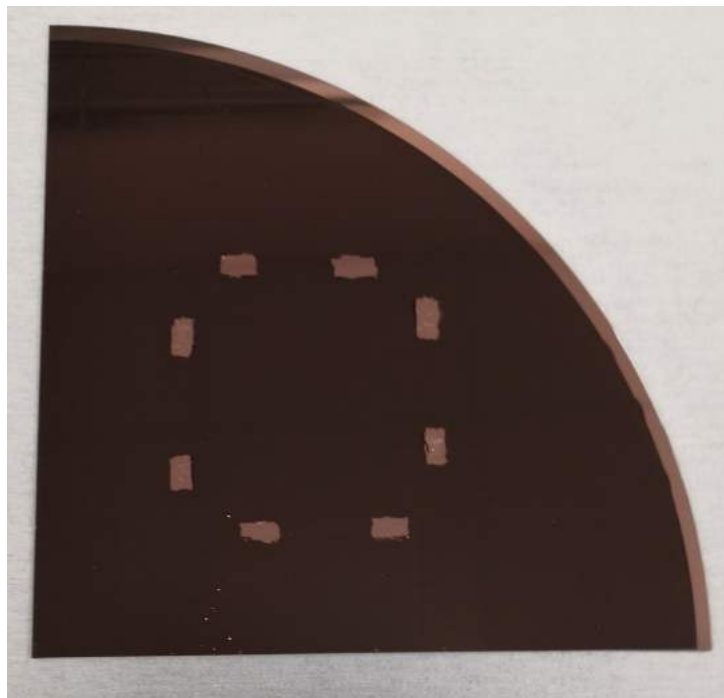


Figure 4.3. Scratched pattern on dried CP3 for optical profiler measurements.

The layer thickness of the prepared wafer quarters were measured with the optical profiler. The Cu paste CP3 on the wafer quarter is reduced from roughly $50\ \mu\text{m}$ wet thickness after printing to $14.25\ \mu\text{m} \pm 0.83\ \mu\text{m}$ after the pre-conditioning. CP1 and CP2 with a wet layer thickness of roughly $50\ \mu\text{m}$ show respective layer thicknesses of $19.30\ \mu\text{m} \pm 1.37\ \mu\text{m}$ and $23.80\ \mu\text{m} \pm 5.08\ \mu\text{m}$ after pre-conditioning. The lower shrinkage rate in comparison to CP3 is assumed to be caused by the distinct organic fraction of the copper pastes [30]. The box plot analysis depicted in Figure 4.4 shows the median layer thicknesses of $19.0\ \mu\text{m}$ for CP1, $22.5\ \mu\text{m}$ for CP2 and $14.0\ \mu\text{m}$ for CP3. The calculated IQR of the measurements are $1.5\ \mu\text{m}$ for CP1, $9.0\ \mu\text{m}$ for CP2 and $1.25\ \mu\text{m}$ for CP3.

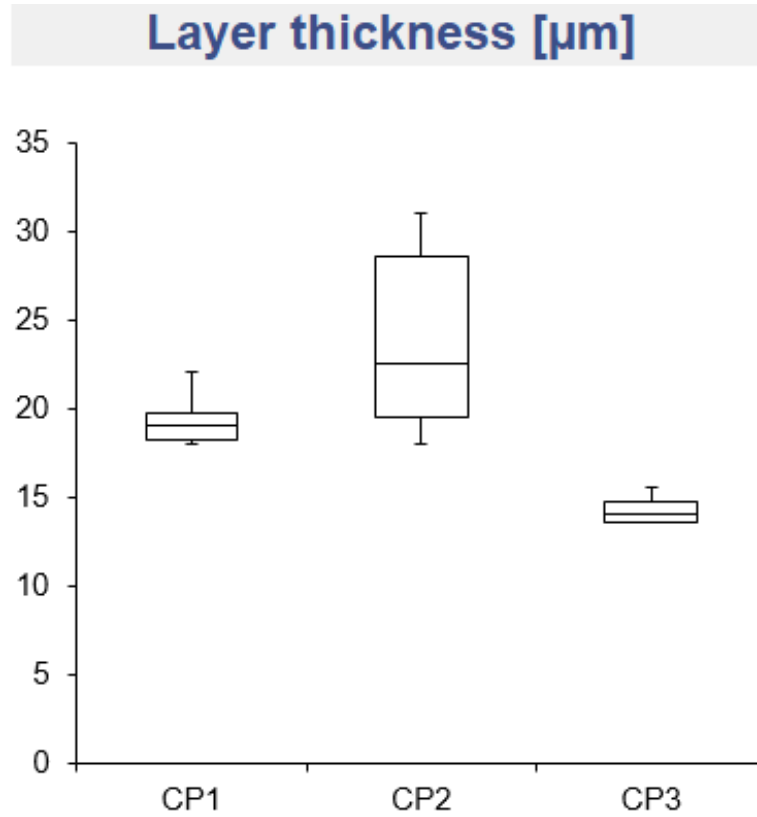


Figure 4.4. Box plot of the measured layer thicknesses of printed copper pastes after pre-conditioning with the standard curing program up to 400 °C and a plateau step of 0 s.

4.4 Resistance Calculation

The specific resistance of the printed copper layers cured using the 400_000 furnace profile is measured with the ResMap 168 by CDE Inc. [55] inside the area enclosed by the scratches for the thickness measurements. The ResMap is an automated four-point-probe, which measures the sheet resistance. The sheet resistance multiplied by the layer thickness gives the bulk resistance Ωm . The sheet resistance of CP3 is measured at $2.73 \text{ m}\Omega_{\square} \pm 0.07 \text{ m}\Omega_{\square}$. Multiplied by the layer thickness t_{Cu} the bulk resistance is calculated as $3.89 \mu\Omega\text{cm} \pm 0.33 \mu\Omega\text{cm}$, which is 2.3 times the resistance of bulk Cu. CP1 and CP2 have a resistance of $5.6 \mu\Omega\text{cm} \pm 0.5 \mu\Omega\text{cm}$ [30] and $21.1 \mu\Omega\text{cm} \pm 1.7 \mu\Omega\text{cm}$ [30], respectively.

5 Thermocompression Bonding

Henceforth, the newly characterised paste CP3 as well as the in previous works characterised paste CP2 [41] are tested using TCB. The DoE setup can be seen in Table 5.1 [42], whereby the sample size is reduced from 16 to 12 for CP2. This could be done because specific parameter sets show low shear strengths for CP1 and thus were removed for CP2. The sample size is raised back to 16 for CP3, because it is speculated that this paste could have a more reactive surface than the previously investigated pastes. The objective is to find the lowest, still reliable bond parameters. CP3 shows unexpected difficulties during TCB in comparison to CP1 and CP2, due to assumed organic surface contaminations. CP2 is tested at first in a small pre-test to determine whether the workflow and bond parameters of CP1 are viable for other pastes. These samples are part of the full DoE.

Table 5.1. DoE for the evaluation of optimised bonding parameters. The input parameters are curing, bonding temperature, bonding pressure and annealing.

Sample	Curing	Thermocompression Bonding		Annealing
	Curing Temperature T_c [°C]	Bonding Temperature T_B [°C]	Bonding Pressure p_B [MPa]	400°C, 3h
1	250	250	15	no
2	250	250	15	yes
3	250	400	15	no
4	250	400	15	yes
5	250	250	50	no
6	250	250	50	yes
7	250	400	50	no
8	250	400	50	yes
9	400	250	15	no
10	400	250	15	yes
11	400	400	15	no
12	400	400	15	yes
13	400	250	50	no
14	400	250	50	yes
15	400	400	50	no
16	400	400	50	yes

5.1 Optical Evaluation

The results of a processing step can be quickly evaluated through optical inspection. The deposited copper sinter paste changes its colour gradually during the sintering due to loss of additives from brown to pink, depicted in Figure 5.1. The sinter grade of the copper particles is correlated to the change of colour [41], [68]. The sinter quality of characterised pastes is evaluated through SEM imaging of the printed metal layer after processing. In the pressureless sintered metallic layer, sinter necks between the particles and no satellites should be visible [69]. Satellites are small particles that are not sintered to the matrix. Figure 5.2 shows a cross section SEM image of the pressureless sintered sample of CP3

at 400 °C. The sinter process is sufficiently progressed, but the sample shows occasional satellites in its pores.

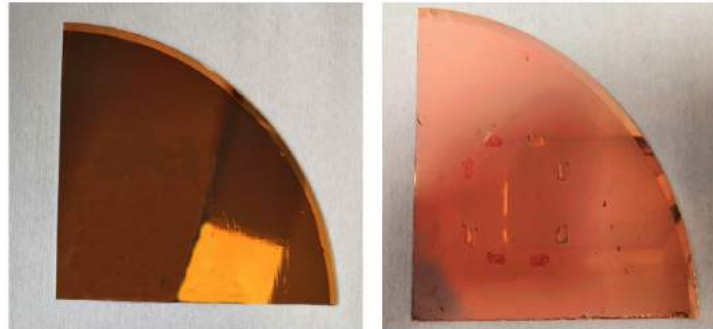


Figure 5.1. Colour comparison of a quarter wafer of pre-conditioned CP3 in an unsintered state (left) and after pressureless sintering (right).

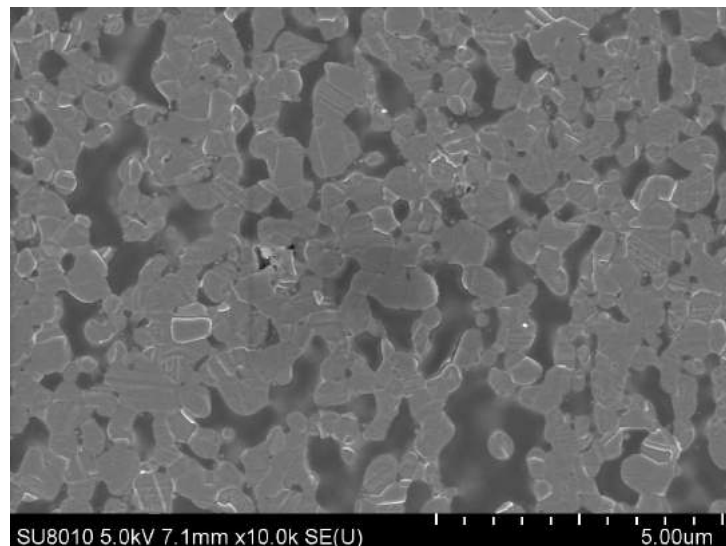


Figure 5.2. SEM image of a polished, pressureless sintered sample from a quarter wafer of pre-conditioned CP3.

The surface morphology and layer thickness are measured with an optical profiler. The R_q is relevant for the bonding process and the shrinkage of the printed layer through thermal processing is important for further FAB-processing. Figure 5.3 shows the false colour topographic image in the range of $-1.07\ \mu\text{m}$ to $+1.09\ \mu\text{m}$ of a measured sample of CP3. The white and red coloured areas are above the median level and the black and blue areas are below the median level. The image in addition shows inconsistencies in the layer thickness due to printing and thermal processing.

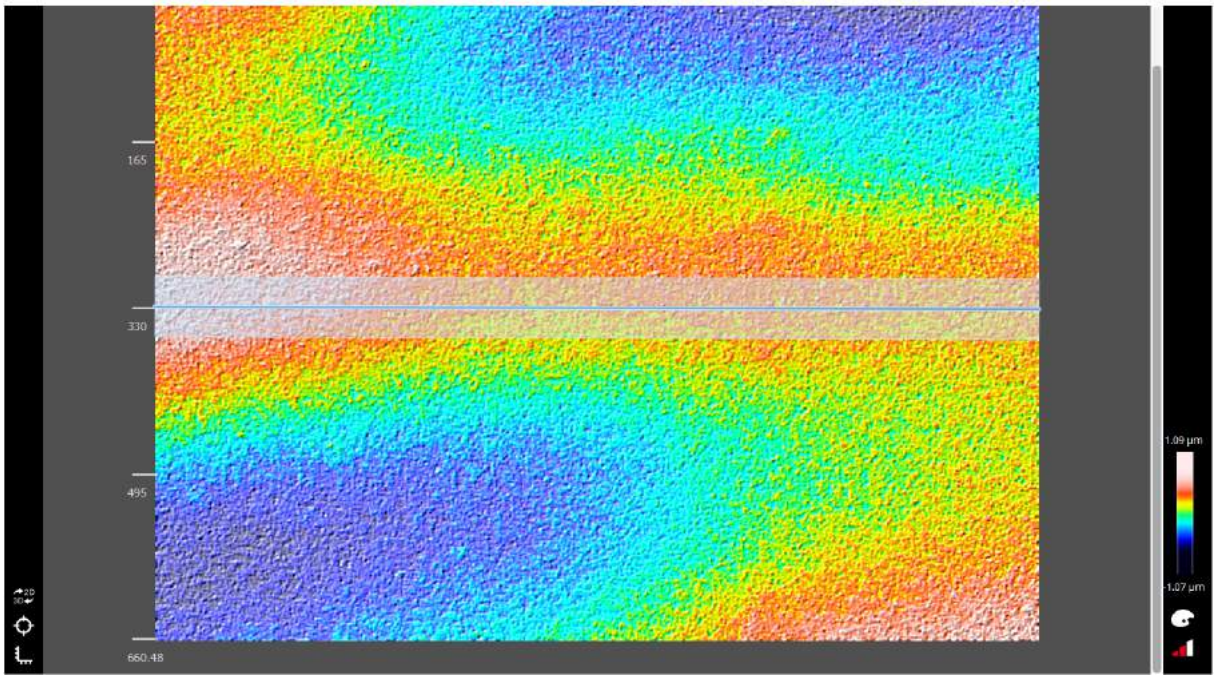


Figure 5.3. False colour image of a pressureless sintered sample from a quarter wafer of pre-conditioned CP3.

A sample of each parameter set in the bonding DoEs is prepared for optical evaluation. The sample is embedded in resin and prepared for a cross section analysis. The prepared cross section is investigated under an optical microscope to check for bleed out of paste through the bonding process [70] and delamination caused through the embedding process, which would be a sign of insufficient bonding. A well-bonded sample, depicted in Figure 5.4, shows no noticeable features of an insufficient bonding process.



Figure 5.4. Picture of sample 3 of CP3 taken with an optical microscope.

The microstructure of the sample, depicted in Figure 5.5 for CP3, is checked by SEM. The sample should indicate neck growth between the particle structure and should be void of satellites. Satellites can be the cause of electrical failures [71] and empirical observations of tested copper pastes have linked the occurrence of satellites after the pre-conditioning to insufficient sintering. The pictured sample depicts sufficient sinter neck growth and distinctive satellites on the surface of the copper particles. This might indicate sufficient sintering in CP3 despite the presence of satellites due to the low thermal treatment during the pre-conditioning. Its fine copper particles display a significant reflow at low pre-conditioning temperatures, which might not be sufficient to remove the satellites. Figure

5.6 shows sample 3 of the bonding DoE for CP3. The microstructure displays no initial particle structure and the satellite count is drastically reduced. This might indicate a sufficient additional thermal treatment during the bonding process to avoid sources of electrical failures. The image can additionally be used to measure the porosity of the metallic layer after the bonding process through digital image correlation (DIC).

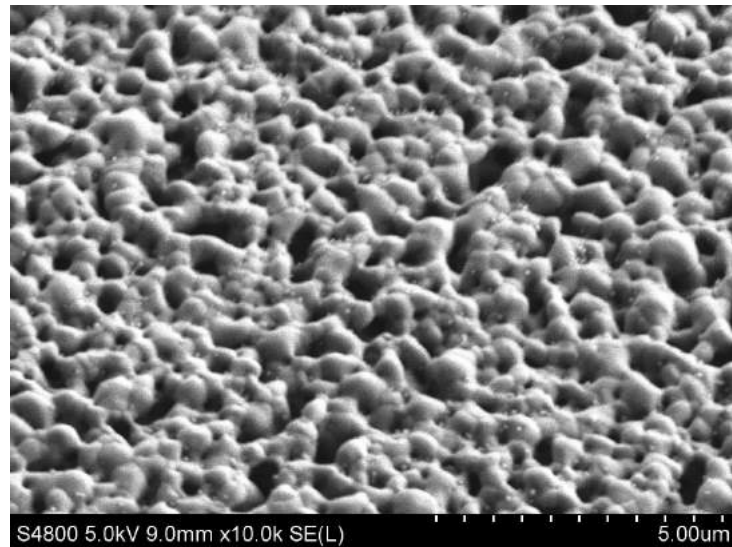


Figure 5.5. SEM image of the surface of a pressureless sintered sample from a quarter wafer of pre-conditioned CP3.

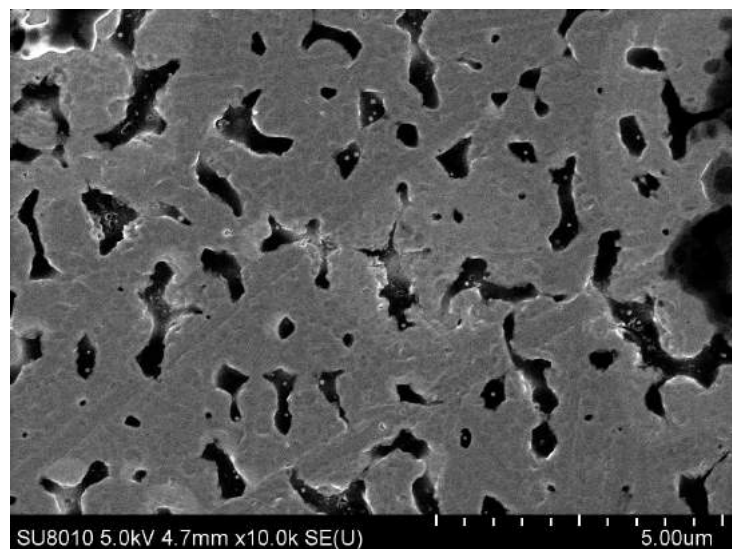


Figure 5.6. SEM image of the cross section of the pressure-sintered sample 3 of CP3.

A second sample with the same parameter set is prepared for imaging by SAM. Figure 5.7 shows a resulting exemplary SAM image. The SAM imaging exhibits the continuity in the bonding interface of the top chip. Voids are depicted as bright spots in the image [72]. Figure 5.7 shows no such voids for the top interface. The contrast in the surrounding area

of the die highlights the porosity of the non-bonded metal layer. The exemplary image in Figure 5.8, taken with an optical microscope after the shear test correlates with the SAM image above. The bright area is the bare Si substrate visible through the delamination of the seedlayer on the bottom chip. In some cases, a crack can migrate through the Si bulk and decrease the theoretical bond strength.

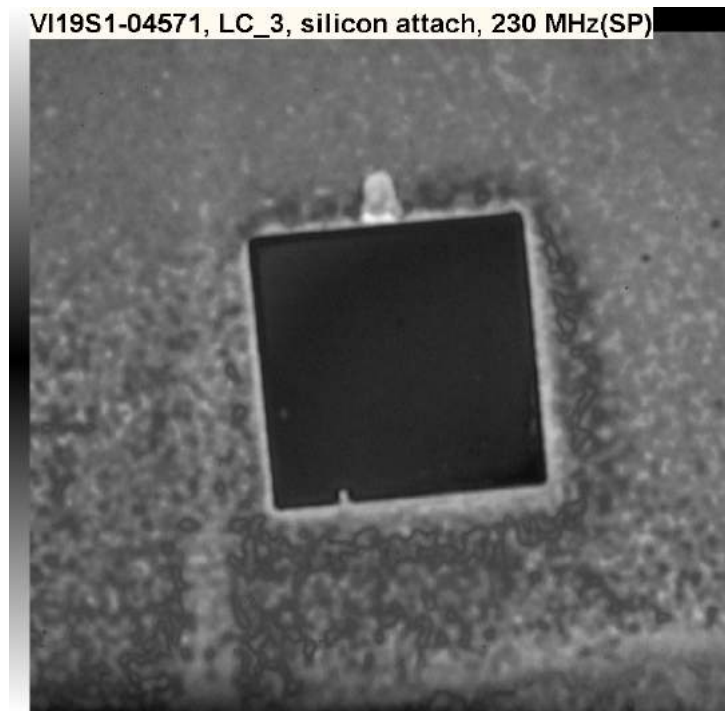


Figure 5.7. SAM image of sample 3 of CP3 after TCB.



Figure 5.8. Optical microscope image of sample 3 of CP3 after SAM imaging and the shear test.

5.2 Shear Tests

A sample of each parameter set in the bonding DoEs is prepared to measure the shear strength of the bonding interface produced during the bonding process.

The shear force of the bonded stack is defined as the maximum force applied by measuring the force-displacement diagram, depicted in Figure 5.9. At this point the critical crack growth is initialized and the bonded interface of the stack delaminates.

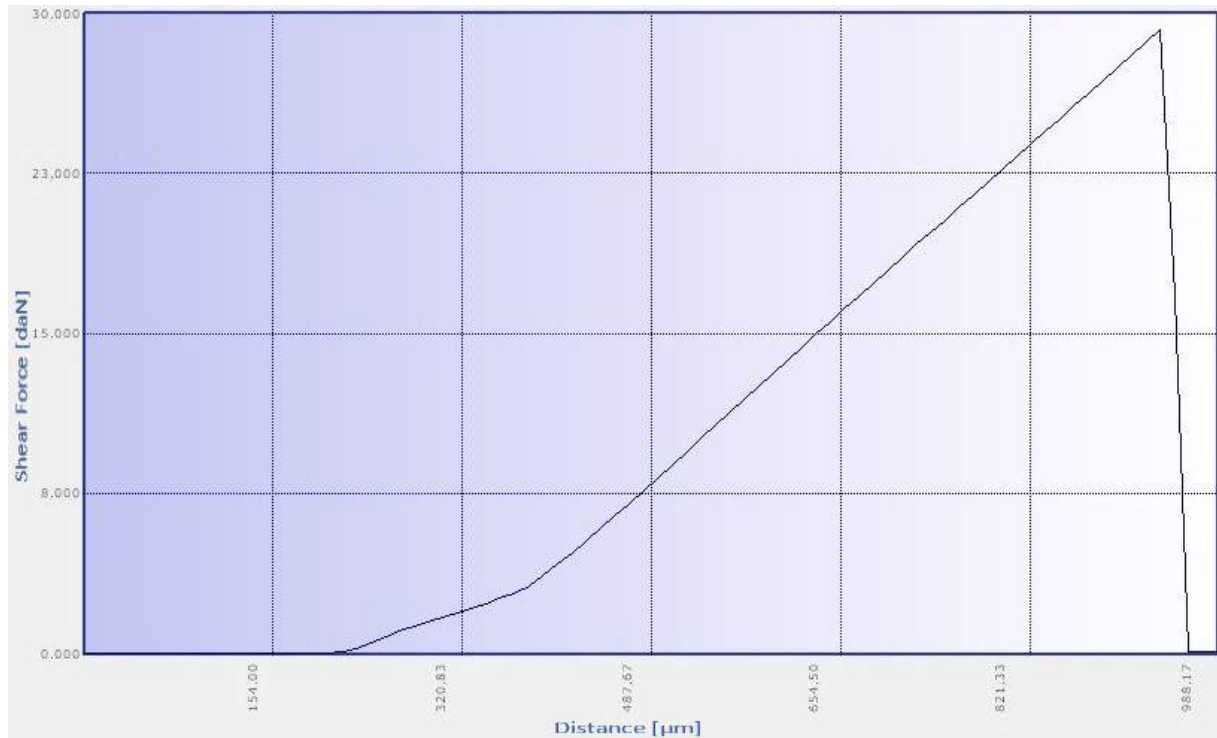


Figure 5.9. The force-displacement diagram of sample 8.1 for the DoE in Section 7.2.

6 Results of the Thermocompression Bonding

6.1 Results for the CP1 DoE

In a pre-dating project, the DoE for CP1 was done by Karner within his master thesis [42]. As evident from Table 6.1, the best bonding results were achieved for low curing temperatures, high bonding temperatures, high bonding pressure and an annealing step.

Table 6.1. Shear strengths for the CP1 DoE by Karner [42].

Sample	Curing	Thermocompression Bonding			Annealing	Shear Test
	Curing Temperature T_c [°C]	Bonding Temperature T_B [°C]	Bonding Pressure p_B [MPa]	400°C, 3h	Shear Force [MPa]	
1	250	250	15	no	2.57	
2	250	250	15	yes	12.40	
3	250	400	15	no	39.09	
4	250	400	15	yes	28.75	
5	250	250	50	no	24.35	
6	250	250	50	yes	37.87	
7	250	400	50	no	> 40	
8	250	400	50	yes	> 40	
9	400	250	15	no	0	
10	400	250	15	yes	11.32	
11	400	400	15	no	6.82	
12	400	400	15	yes	33.10	
13	400	250	50	no	34.25	
14	400	250	50	yes	17.73	
15	400	400	50	no	> 40	
16	400	400	50	yes	> 40	

6.2 Results for the CP2 DoE

The reduced DoE for CP2 with 12 samples shows sufficient bond strength of all parameter sets, listed in Table 6.2. The graphical analysis is done by plotting the linear regression analysis of an irregular fraction factorial system in Cornerstone. Table 6.3 shows a table of all p-values for the parameters and interactions. Only parameters and interactions below a p-value of 0.1 are considered. P-values below 0.1 are deemed as a statistically significant effect. The parameter "Annealing" (Ann) is included, because it is needed to factor in relevant higher degree interactions, according to the strong heredity principle [73]. The Pareto chart arranges the parameters and interactions by their weight in the linear regression model, whereby the most left bar describes the biggest coefficient of the linear regression model. A negative weight indicates a negative coefficient in the linear regression model. Figure 6.1 shows the Pareto chart for all relevant parameters and interactions for the CP2 DoE. The most important parameters for the resulting shear strength (SF) of the bonded CP2 samples are the curing temperature (T_c) during the pre-conditioning and the bonding temperature (T_B). The preferred parameter setup for bonded samples of CP2 is a low temperature pre-conditioning and a high temperature TCB, due to the correlations of the coefficients for (T_B) and (T_c) in the linear regression model.

Table 6.2. Shear strengths for the CP2 DoE.

Sample	Curing	Thermocompression Bonding		Annealing	Shear Test
	Curing Temperature T_c [°C]	Bonding Temperature T_B [°C]	Bonding Pressure p_B [MPa]	400°C, 3h	Shear Force [MPa]
1	250	250	15	no	27.53
2	250	250	15	yes	30.44
3	250	400	15	no	41.43
4	250	400	15	yes	9.31
5	250	250	50	no	11.49
6	250	250	50	yes	17.19
7	250	400	50	no	37.82
8	250	400	50	yes	74.55
9	400	250	15	no	\
10	400	250	15	yes	\
11	400	400	15	no	8.29
12	400	400	15	yes	5.59
13	400	250	50	no	\
14	400	250	50	yes	\
15	400	400	50	no	6.51
16	400	400	50	yes	13.50

Table 6.3. Significance table of CP2 bond tests.

Term Significance	
Term	SF
Constant	0.001
T_C	$5 \cdot 10^{-1}$
T_B	0.001
p_B	0.062
Ann	0.302
$T_B * T_C$	
$p_B * T_C$	0.393
Ann * T_C	0.012
$p_B * T_B$	0.047
Ann * T_B	0.015
Ann * p_B	0.127
R-Square	0.991
Adj R-Square	0.969
RMS Error	3.664
Residual df	3
Transformation	Untran

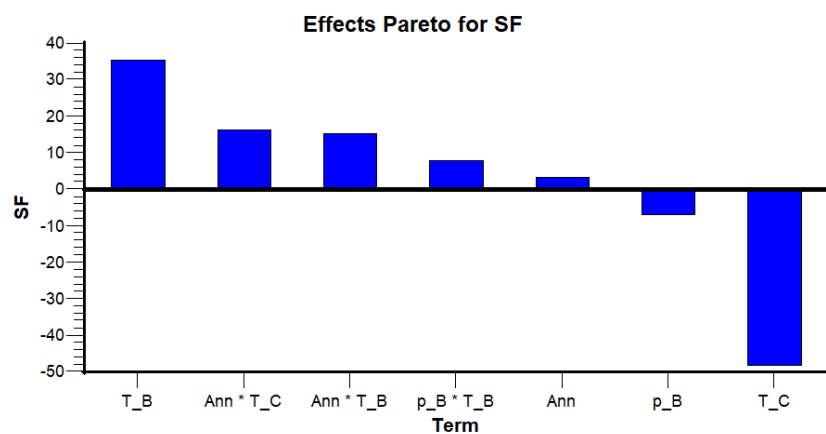


Figure 6.1. Pareto chart of CP2 bond tests.

The interaction graph, shown in Figure 6.2, describes the correlation of different parameter sets and the resulting shear strengths. The interaction graphs show an increased shear strength (SF) for sets with low curing (T_C) and high bonding temperatures (T_B). It is assumed that the low curing temperature is not sufficient to fully sinter the copper layer and the interrupted sinter process can be continued during TCB. Annealing (Ann) further increases the shear force of low curing and high bonding temperature samples. The bonding pressure (p_B) is of lower significance for the shear strength of CP2, presumably due to the high porosity of its microstructure, which might facilitate the densification

at lower bonding pressures in relation to less porous pastes. It is hypothesised that the thermal treatment is the significant factor for CP2, because of its coarse copper particles in relation to other copper pastes. The low temperature range of the pre-conditioning at 250 °C is close to the measured inflection point, which indicates the beginning of sinter neck growth between the copper particles, as depicted for CP3 by the steep decline in Figure 4.2. It can be assumed, that the sinter necks are not fully developed after the pre-conditioning, which would allow uncomplicated particle movement at a lower bonding pressure [74]. Therefore CP2 might be, in contrast to CP1, never sintered to a saturated level during the pre-conditioning.

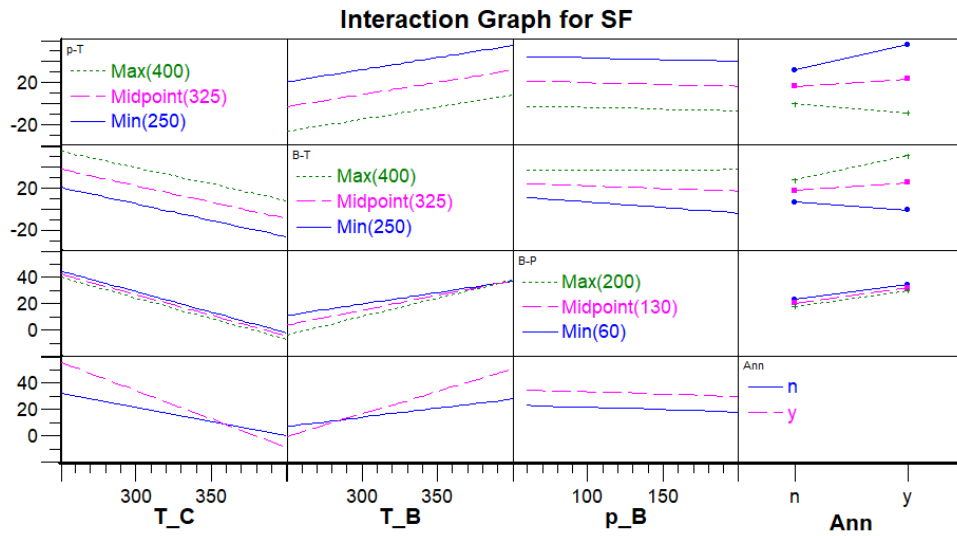


Figure 6.2. Interaction graph of the parameters T_C , T_B , p_B and Ann for the bonding DoE of CP2.

6.3 Results for the CP3 DoE

The full factorial DoE of CP3 shows insufficient bond strength for most parameter sets, which is especially pronounced for the samples with low bond parameters in temperature and pressure. The bonded top dies of the samples marked with a shear strength of 0 MPa in Table 6.4 detached before the actual shear strength measurement could be conducted. Further processing to prevent this problem is discussed in Section 7.2. The graphical analysis was performed with the software CEDAS Cornerstone. The significant parameters for the bonding process are curing temperature (T_C) and bonding temperature (T_B), as depicted in Table 6.5. Figure 6.3 shows the Pareto chart for all relevant parameters and interactions. The thermal treatments of the pre-conditioning, TCB and annealing are the significant coefficients in the linear regression model, whereby a low temperature during pre-conditioning is beneficial, because of its negative coefficient in the regression model.

Table 6.4. Shear strengths for the CP3 DoE.

Sample	Curing	Thermocompression Bonding		Annealing	Shear Test
	Curing Temperature T_c [°C]	Bonding Temperature T_B [°C]	Bonding Pressure p_B [MPa]	400°C, 3h	Shear Force [MPa]
1	250	250	15	no	0
2	250	250	15	yes	0
3	250	400	15	no	>40
4	250	400	15	yes	79.15
5	250	250	50	no	0.98
6	250	250	50	yes	4.78
7	250	400	50	no	46.84
8	250	400	50	yes	72.70
9	400	250	15	no	0
10	400	250	15	yes	0
11	400	400	15	no	20.17
12	400	400	15	yes	39.26
13	400	250	50	no	0
14	400	250	50	yes	0
15	400	400	50	no	3.47
16	400	400	50	yes	7.46

Table 6.5.
Significance table
of CP3 bond tests.

Term Significance	
Term	SF
Constant	$5 \cdot 10^{-3}$
Ann	0.091
p_B	0.128
T_B	0.003
T_C	0.005
Ann * p_B	0.799
Ann * T_B	0.378
Ann * T_C	0.382
p_B * T_B	0.299
p_B * T_C	0.21
T_B * T_C	$1 \cdot 10^{-1}$
R-Square	0.849
Adj R-Square	0.794
RMS Error	12.4
Residual df	11
Transformation	Untran

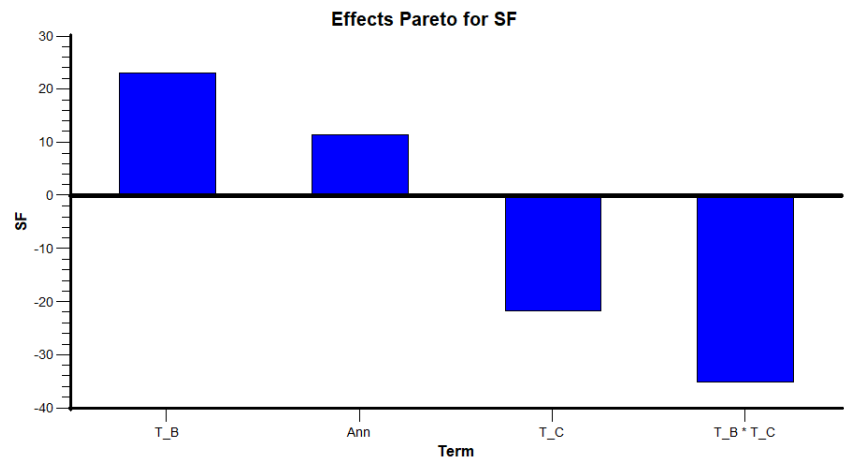


Figure 6.3. Pareto chart of CP3 bond tests.

As shown in the interaction graphs for the shear strength (SF) in the bonding DoE of CP3, depicted in Figure 6.4, the highest shear strengths are achieved with low curing (T_C) and high bonding temperatures (T_B). The annealing process (Ann) improves the bond strength for all parameter sets. It is hypothesised, that the bonding pressure (p_B) is insignificant because of the smooth surface of CP3. The (p_B) during TCB is assumed to be necessary to compensate for the low contact area of surfaces with high R_q , to support the reflow of the sintered copper layer [75]. The smooth surface enables

a higher initial contact area of the bonded samples during TCB, which allows the use of lower (p_B). Due to the fine particle microstructure of CP3, the thermal treatment is the most significant parameter. CP3 might sinter to its full potential during pressureless pre-conditioning at 400 °C, which would hinder further sintering during TCB [74].

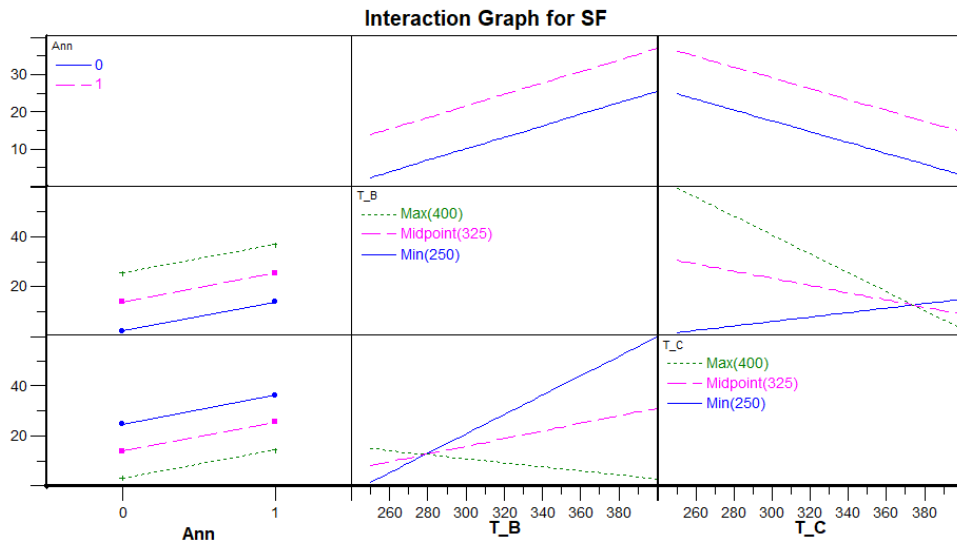


Figure 6.4. Interaction graph of the parameters Ann , T_B and T_C for the bonding DoE of CP3.

7 Chemical and Physical Paste Conditioning

To further optimize the performance of the investigated copper pastes in the TCB tests, chemical and physical treatments are applied. The assumption for the correlation between the bond strength of the die and the R_q of the substrate is derived from studies on direct bonding of silicon wafers [39], where a smooth surface is necessary to guarantee a void-free wafer stacking. The hypothesis in this work is that the TCB of porous layers might benefit from a similar approach. Areas of initial contact during the bonding process experience the peak force of the bonding process, whereas areas with lower topography may not come into contact with the bonded die at all. Although the R_q of CP3 ($0.11 \mu\text{m} \pm 0.03 \mu\text{m}$) is significantly lower than that of CP1 ($1.84 \mu\text{m} \pm 0.09 \mu\text{m}$) and CP2 ($2.56 \mu\text{m} \pm 0.36 \mu\text{m}$), the surface characterisation of CP3 shows a high content of carbon, as evident from the Auger spectroscopy analysis of pre-conditioned CP3 summarised in Appendix B.2. The surface contamination might prohibit the forming of sintered bonds between the copper substrate and the sputtered copper surface of the die. Due to the large amount of non-bonded dies, the bonding DoE of untreated CP3 shows that the organic surface barrier cannot be broken during TCB. Thus, to remove the organic surface contamination, a DoE with various chemical cleaning processes was prepared.

7.1 Influence of Surface Roughness

To minimise R_q of CP1 and CP2, a chemical mechanical polishing (CMP) is applied to the pre-conditioned wafers. To avoid possible delamination of the printed layer during the CMP step, only the high-temperature samples with a curing temperature of 400°C were treated with CMP. As indicated by Table 7.1, CP1 and CP2 are processed in two iterations. In the first run the wafers are polished with a default CMP process at a pressure of 4 psi (275.79 mbar) for 120 s. The imperial unit psi (pounds per square inch) is a default parameter for CMP processes and equals 68.95 mbar. With the information of the surface roughness and the layer thickness resulting from the first run, the second iteration was performed with a reduced pressure of 2 psi (137.90 mbar) for an increased period of 180 s. The assumption is that the reduced surface roughness can also be achieved at lower pressures, while reducing the abrasion rate, to preserve higher layer thicknesses.

Table 7.1. DoE for the evaluation of the influence of the CMP parameters on the R_q of CP1 and CP2.

Sample	Paste	Pressure [psi]	Duration [s]
CP1_120	CP1	4	120
CP2_120	CP2	4	120
CP1_180	CP1	2	180
CP2_180	CP2	2	180

Figure 7.1 shows the SEM surface image of sample CP1_120 of the CMP DoE after the treatment. The peaks of the printed copper layer are flattened to plateaus through the CMP treatment, which increases the initial contact area during the bonding process.

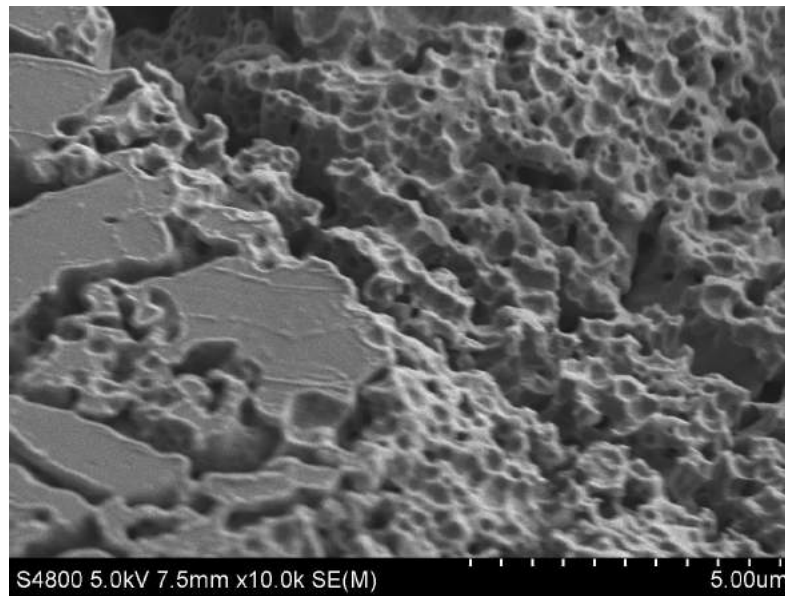


Figure 7.1. SEM image of sample CP1_120 after CMP treatment.

Depicted in Table 7.2, the prepared wafers for CMP had a pre-conditioning layer thickness of $19.3\ \mu\text{m} \pm 1.4\ \mu\text{m}$ for CP1 and $23.8\ \mu\text{m} \pm 5.1\ \mu\text{m}$ for CP2. The R_q of the provided samples was $1.84\ \mu\text{m} \pm 0.01\ \mu\text{m}$ for CP1 and $2.56\ \mu\text{m} \pm 0.16\ \mu\text{m}$ for CP2. The measurements on the samples CP1_0 for CP1 and CP2_0 for CP2, as depicted in Figure 7.2 and Figure 7.3 show that the printing process and pre-conditioning provides a CP1 wafer with homogeneous layer thickness and R_q , but the measured wafer of CP2 displays significant fluctuations in the layer thickness and R_q . The fluctuation of the layer thickness is a well-known problem, which stems from tolerances of the printing process when the paste is deposited with deviations in a wet state and then thermally processed [30]. During this curing process, inhomogeneities in particle and binder distribution can cause inhomogeneous shrinkage of the printed layer. CMP is the standard process in FAB workflows to achieve planar layers. The properties of copper paste layers depends on the sintered particles. Depending on the pre-conditioning, single microparticles may be fully removed

during CMP and can leave significant cavities in the surface. Figure 7.2 shows the box plot for the layer thickness of CP1 and CP2 before and after the CMP treatments. Figure 7.3 shows the R_q of the samples in the CMP DoE from 7.1. The statistical analysis of the CMP treated wafers depicted in the box plots shows the deviations of the layer thickness and R_q between the measured positions on the wafers. The CMP treatment of CP1 with 4 psi (275.79 mbar) for 120 s presents the best results. The treatment reduces the fluctuations of layer thickness and R_q of the pre-conditioned CP1 wafer significantly, while minimising the thinning of the CP1 layer. The CMP treatment of CP1 with 2 psi (137.90 mbar) for 180 s is not as beneficial as the CMP treatment with 4 psi (275.79 mbar) for 120 s. Both CMP treatments lead to no simultaneous improvement for the fluctuations of layer thickness and R_q for CP2, as evidenced by the outliers, which are displayed as red dots in the box plots. The copper particles of CP2 are coarser in relation to CP1, which presumably leads to the larger surface roughening for the CP2 wafers. It is assumed that the high porosity of the microstructure of pre-conditioned CP2 results in the formation of fragile sinter necks between the particles in relation to CP1. This might lead to the breakage of the sinter necks and full abrasion of surface copper particles.

Table 7.2. Resulting layer thickness and R_q for CP1 and CP2 after two different CMP treatments.

Sample	Layer Thickness [μm]	Surface Roughness [μm]
CP1_0	19.3 ± 1.4	1.84 ± 0.01
CP2_0	23.8 ± 5.1	2.56 ± 0.16
CP1_120	18.7 ± 0.6	0.66 ± 0.01
CP2_120	14.5 ± 3.8	1.62 ± 0.06
CP1_180	6.5 ± 2.0	0.69 ± 0.02
CP2_180	9.7 ± 1.9	2.02 ± 0.17

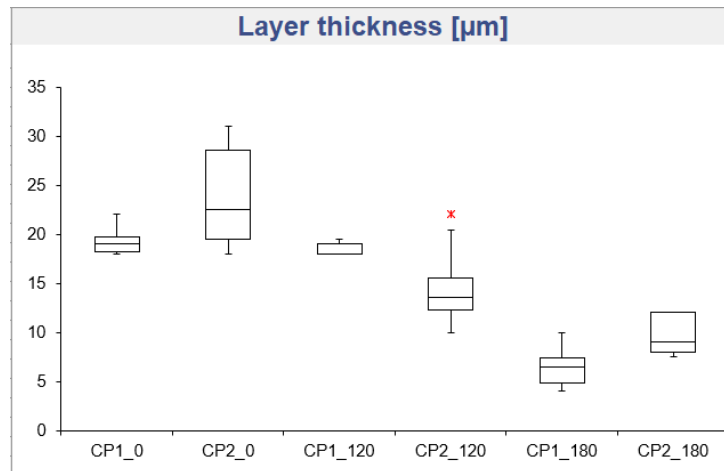


Figure 7.2. Box plots for the layer thickness of the two different CMP treatments in relation to untreated CP1 and CP2.

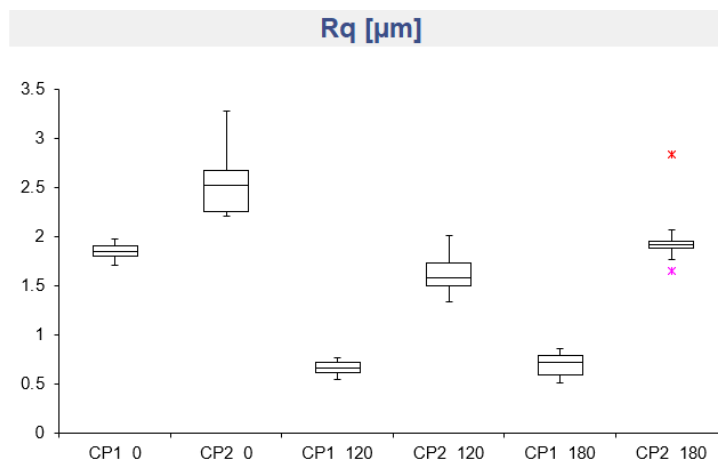


Figure 7.3. Box plots for the R_q of the two different CMP treatments in relation to untreated CP1 and CP2.

The linear regression analysis of the CMP treatments with the program CEDA Cornerstone displays the process parameters for the minimisation of R_q and the preservation of the layer thickness of the printed copper paste wafers in Table 7.3. Only the parameters with a p-value of less than 0.1 are considered as statistically relevant. The Pareto chart for R_q , depicted in Figure 7.4, indicates the direct correlation of the porosity and the indirect correlation of the CMP pressure to the resulting R_q . The correlation with the porosity is assumed to originate from the microstructure of the sintered copper pastes, which might lead to surface breakouts of particles through the CMP treatment. The remaining layer thickness after the CMP treatment is solely defined by the process duration, as shown in the Pareto chart in Figure 7.5. It is theorised that the process pressure does not deform the microstructure of the pre-conditioned copper layer and that the CMP treatment has a roughly linear abrasion rate.

Table 7.3. Significance table of CMP tests for the parameters R_q and layer thickness.

Term Significance		
Term	R_q	lay
Constant	$3 \cdot 10^{-5}$	$7 \cdot 10^{-4}$
por	0.001	0.701
time	0.545	0.023
pres	$7 \cdot 10^{-4}$	0.482
R-Square	0.994	0.763
Adj R-Square	0.989	0.703
RMS Error	0.078	3.44
Residual df	3	4

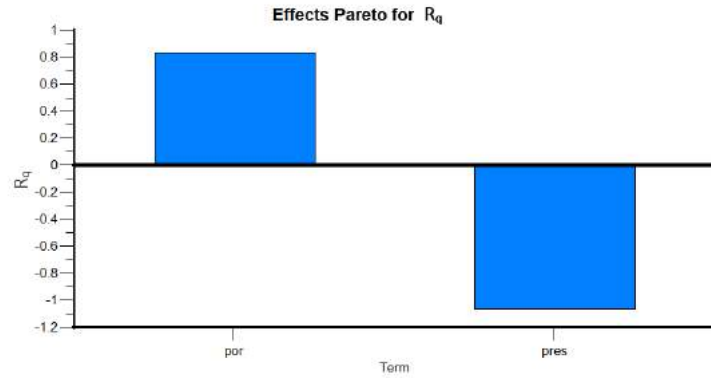


Figure 7.4. Pareto chart for R_q .

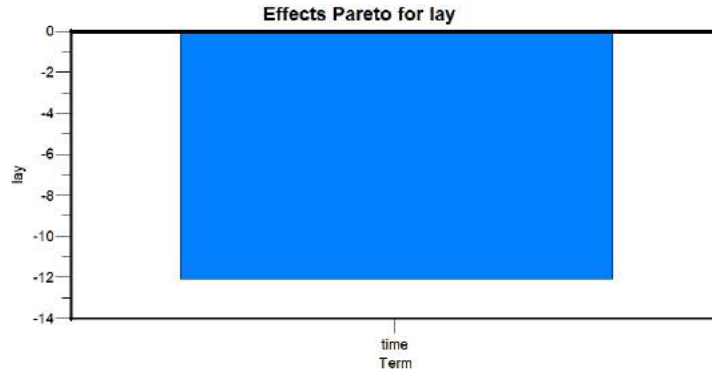


Figure 7.5. Pareto chart for layer thickness.

Sample 1 of the CMP DoE is further split into eight bond samples and the shear strengths are compared to those of untreated CP1 samples [42], bonded with the same parameter set. The list of samples in the bonding DoE and the measured shear strengths can be seen in Table 7.4. Sample 1 for the untreated CP1 detached, before it could be measured. Samples 7 and 8 surpassed the limit of the used shear test setup at 40 MPa.

Table 7.4. Shear strengths for the CMP DoE of CP1.

Sample	Curing	Thermocompression Bonding		Annealing	Shear Test	
	Curing Temperature T_c [°C]	Bonding Temperature T_B [°C]	Bonding Pressure p_B [MPa]	400°C, 3h	Untreated Shear Force [MPa]	Treated Shear Force [MPa]
1	400	250	15	no	16.77	0
2	400	250	15	yes	21.36	11.32
3	400	400	15	no	5.42	6.82
4	400	400	15	yes	17.56	33.10
5	400	250	50	no	36.77	34.25
6	400	250	50	yes	41.21	17.73
7	400	400	50	no	20.61	>40
8	400	400	50	yes	22.51	>40

The linear regression analysis with the program CEDA Cornerstone of the shear data for the CMP DoE shows that the statistically significant parameters for the resulting shear force (SF) are the bond temperature (T_B) and the interaction effects between the bond pressure (p_B) and R_q , as well as between (T_B) and the annealing step (Ann), as evident from Table 7.5. The parameters (p_B), R_q and (Ann) have p-values above 0.1 and are therefore not statistically relevant, but are included for their interactions due to the strong heredity principle. The Pareto chart depicted in Figure 7.6 displays that the coefficients of R_q , (T_B), (p_B) and (Ann), as well as the interactions of (Ann) with (p_B) and (Ann) with (T_B) contribute significantly to the linear regression model of the shear strength (SF) of the CMP TCB samples.

Table 7.5.
Significance table
of CMP bond tests for
CP1 for the parameter
surface roughness.

Term Significance	
Term	SF
Constant	$1 \cdot 10^{-7}$
R_q	0.968
p_B	0.793
T_B	$3 \cdot 10^{-1}$
Ann	0.104
p_B * R_q	0.002
R_q * T_B	0.428
Ann * R_q	0.941
p_B * T_B	0.438
Ann * p_B	0.143
Ann * T_B	0.027
R-Square	0.874
Adj R-Square	0.791
RMS Error	6.104
Residual df	9
Transformation	Untran

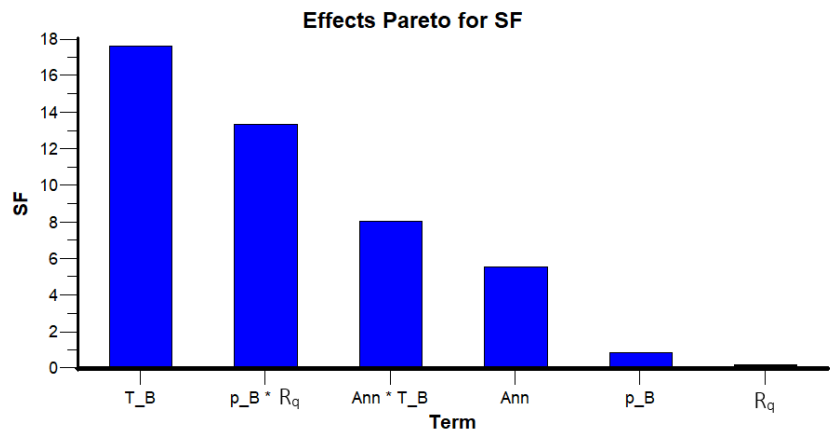


Figure 7.6. Pareto chart of CMP bond tests for CP1.

The interaction graph of the CMP treated bonding DoE is depicted in Figure 7.7. It is obvious that the most important parameters are the individual process temperatures. It is crucial to preserve the reactivity of the porous sinter layer, qualitatively given by its surface energy. The reactivity throughout the workflow is preserved by incrementing process temperatures. This influences the ability to form bonds during the TCB and the subsequent annealing step. The second significant parameter is the correlation between the R_q and the bond pressure, each of which, separately, are insignificant. For low pressure bonding, a smooth surface is beneficial. Through planarization of the substrate, the

contact area to the die is increased and the bond strength increases with the bonded area of the die [75]. The CMP process is in itself a potential source for critical mechanical damages to the substrate through abrasive forces. These defects can reach the critical size to provoke bond failures. In combination with high bond pressures, the substrate can crack and diminish the shear strength of the bonded structure. A non-controllable parameter is the homogeneity of the pressure distribution over the area of the die. A lack of homogeneity can lead to reduced bonded areas and in succession to reduced shear strengths.

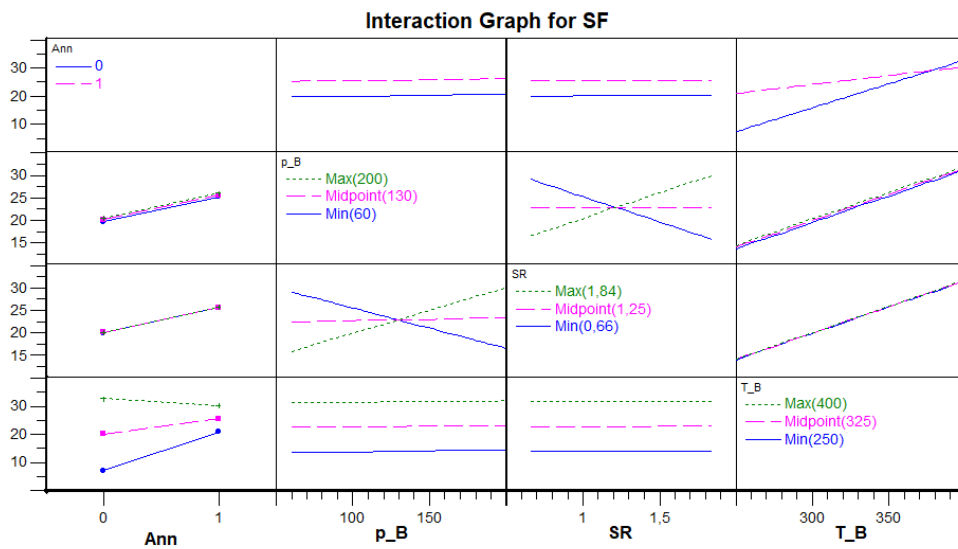


Figure 7.7. Interaction graph of the parameters Annealing (Ann), bond pressure (p_B), R_q and bond temperature (T_B) for the bonding DoE of CMP treated CP1.

7.2 Influence of Organic Surface Contaminations

Auger electron spectroscopy of CP3, as summarised in Appendix B.1, indicates a high carbon content on its surface. To remove the surface organic residues, a cleaning DoE was applied within the master thesis of Dillinger [76] including a commercial stripping agent, a plasma asher and cascade cleaning by alternating furnace processes in ambient and reducing atmospheres. The cleaned samples are evaluated in a bonding DoE. As depicted in Table 7.6, none of the used cleaning processes improved the bondability of CP3.

Table 7.6. Shear strengths for the cleaning DoE.

Sample	Cleanin process	Thermocompression Bonding		Shear Test
		Bonding Temperature TB [°C]	Bonding Pressure p_b [MPa]	Shear Force [MPa]
3.1	Plasma Asher	400	50	16.83
3.2	Plasma Asher	400	50	4.46
5.1	Cascade curing 1 cycle	400	50	0.13
5.2	Cascade curing 1 cycle	400	50	2.22
7.1	Cascade curing 5 cycles	400	50	7.14
7.2	Cascade curing 5 cycles	400	50	1.17
8.1	Untreated	400	50	28.29
8.2	Untreated	400	50	2.58

8 Discussion

After preliminary paste characterisations, CP3 is selected for bonding tests in addition to the reference pastes CP1 and CP2.

The micro-nano-particle paste CP2 shows the highest R_q with $2.56 \mu\text{m} \pm 0.16 \mu\text{m}$ and the lowest shrinkage of layer thickness from the printed $50 \mu\text{m}$ to $23.8 \mu\text{m} \pm 5.1 \mu\text{m}$ through thermal processing with the default program "400_000". The nano-particle paste CP3 yields the highest shrinkage from the initially printed layer of $50 \mu\text{m}$ to $14.25 \mu\text{m} \pm 0.83 \mu\text{m}$ in layer thickness and the lowest R_q with $0.11 \mu\text{m} \pm 0.03 \mu\text{m}$ after the default thermal processing. CP1, as a micro-nano-particle paste, shows intermediate sinter characteristics with an R_q of $1.84 \mu\text{m} \pm 0.01 \mu\text{m}$ and a layer thickness reduction from the printed $50 \mu\text{m}$ to $19.3 \mu\text{m} \pm 1.4 \mu\text{m}$ after the default thermal processing. The R_q of the thermally processed pastes correlates qualitatively with the upper particle size limit of the copper pastes.

The packaging density of the copper pastes before and consequently the porosity after the default thermal processing is mainly influenced by the organic additives, but less by their particle size distributions. CP1 has a porosity, after the default thermal processing, of $31.7\% \pm 2.3\%$, which is similar to CP3 at $33.3\% \pm 3.8\%$. CP2 has the highest porosity of $57.5\% \pm 2.9\%$, which consequently leads to the highest resistance of the pastes at $21.1 \mu\Omega\text{cm} \pm 1.7 \mu\Omega\text{cm}$. CP1 has a resistance of $5.6 \mu\Omega\text{cm} \pm 0.5 \mu\Omega\text{cm}$. The electrical resistance is, as evidenced, proportional to the porosity [77]. The smaller particle size of CP3, in comparison to CP1 and CP2, leads to a lower resistance at $3.89 \mu\Omega\text{cm} \pm 0.33 \mu\Omega\text{cm}$ through the homogeneous microstructure of CP3. CP3 starts the neck growth of the particles at its inflection point for a pressureless sinter process at lower temperatures, i.e. at 159°C , in comparison to CP1 at 165°C and CP2 at 182°C , due to its smaller particle size and therefore higher free surface energy. The potential of pressureless sintering, until the resistance plateau is reached, additionally is at lower temperatures for CP3 compared to CP1 and CP2, which correlates to existing literature [6].

Bonding chip stacks through TCB is achieved with all three of the tested copper pastes. The arbitrarily set threshold for a sufficient shear strength of the chip stack is defined at 30 MPa. The threshold is set at this level from empirical knowledge in BE testing of mounted chips. An additional arbitrary level is the first crack initiation during shear tests in Si chips, which can be observed as low as 50 MPa.

All three pastes yield samples with TCB process parameter sets which exceed the aforementioned thresholds, as can be seen in the Tables 6.1, 6.2 and 6.4. CP1 shows the most equalized shear strength for the tested TCB parameter sets in the bonding DoEs, as depicted in Figure 8.1.

The reference paste CP1 yields shear strengths for bonded samples from 2.57 MPa to above 40 MPa without a CMP treatment, as listed in Table 6.1. The reduced DoE for CP2 indicates shear strengths ranging from 5.59 MPa to 74.55 MPa, as listed in Table 6.2. The shear strength of CP2 decreases with higher temperatures during the pre-conditioning. This might be related to the high porosity of CP2. The sinter neck growth rate increases with higher temperatures with no concomitant increase in density. Non-pressure assisted sintering may lead to pores with higher volumes [7], which can act as crack initiation defects at lower stresses [78]. It is assumed that samples of CP3 with insufficient bonding temperature and bonding pressure could not be bonded through the organic surface contamination. Successfully bonded samples of CP3 show a shear strength in the range of 0.96 MPa to 79.15 MPa, as listed in Table 6.4. CP3 requires higher temperatures to form a bonding interface, but its bonding properties do not depend on the applied pressure in the range of the DoE, which protects the setup from mechanical damages. This may relate to the residual free surface energy of the microstructure of CP3 after the thermal pre-conditioning [6]. CP2 in relation to CP3 may have more residual free surface energy, but due to its significantly higher porosity needs higher bonding pressures to assist the densification process during TCB. CP3 shows bond strengths for low bond pressures that are comparable to the results of high pressures for the other pastes.

The graphical visualisation of the shear strengths for the samples of the bonding DoEs for the copper pastes is depicted in Figure 8.1. The topmost shear strength is achieved for CP3 at 79.15 MPa. The bonding parameters for this sample were a pre-conditioning at 250 °C, a bonding temperature of 400 °C, a bonding pressure of 15 MPa and an additional annealing step. Shear strengths in corresponding research projects of copper pastes were measured at roughly 35 MPa for the bonding parameters of 250 °C and 10 MPa, as well as roughly 42 MPa for the bonding parameters 300 °C and 10 MPa [79]. Further research projects showed shear strengths of roughly 40 MPa with the bonding parameters 300 °C and 10 MPa [80], as well as roughly 40 MPa for the bonding parameters 400 °C and 15 MPa [81]. A shear strength of 40 MPa is achieved for nine of the 44 samples in the DoEs for the three copper pastes CP1, CP2 and CP3. The highest shear forces for all three pastes are achieved with low temperature pre-conditioning and high temperature bonding. This relates to the hypothesis that the sinter process can be done discontinuously as long as

the follow-up steps are performed at elevated temperatures in relation to the previous thermal budget the metal layer has seen so far.

This utilizes further residual free surface energy of the porous metal layer. The densification effect through the applied pressure for the TCB in addition assists the resumed sinter process [80].

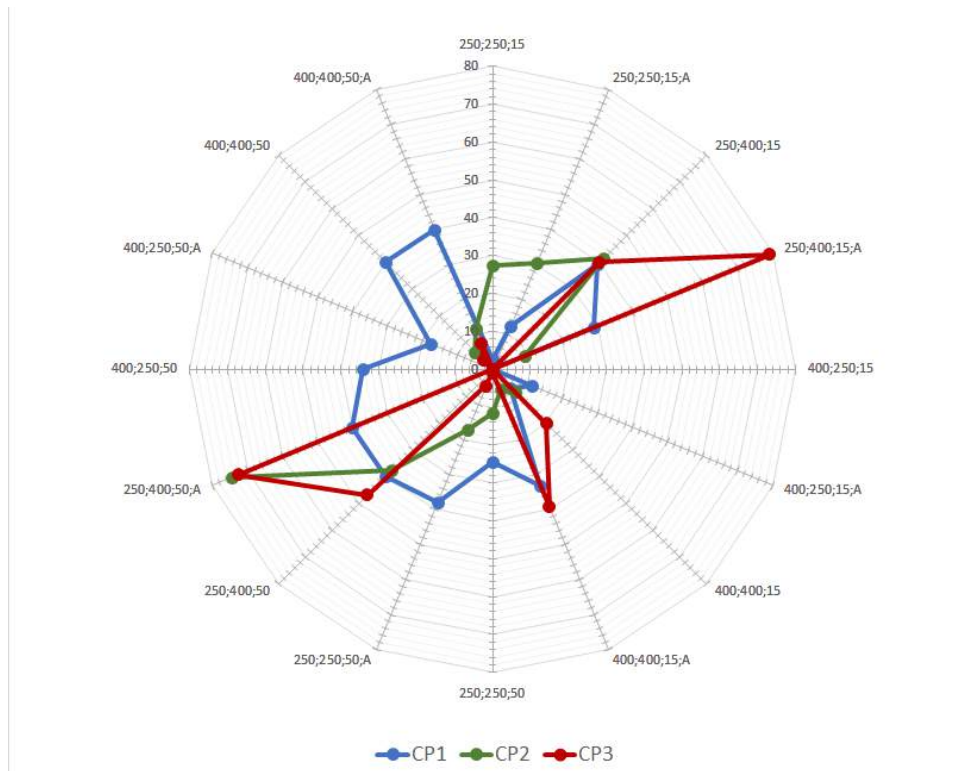


Figure 8.1. Radar chart of the resulting shear strengths of the DoEs for the copper pastes CP1, CP2 and CP3.

A CMP treatment for the pressureless sintered copper paste CP1 can increase the bond strength of chip stacks bonded with low bonding pressure and temperature from 11.32 MPa to 21.36 MPa, as listed in Table 7.2. In contrast, the CMP treatment decreases the bond strength of stacks with high bonding pressure and temperature from above 40 MPa to 22.51 MPa. This might be caused due to damages in the layer, induced during the CMP process [75].

Chemical cleaning of CP3 did not yield an improvement. All cleaning processes decreased the shear strength of the chip stacks in relation to untreated CP3, as listed in Table 7.6. This might be due to surface roughening of CP3 caused during the cleaning processes, while not fully removing the surface contamination.

9 Conclusion and Outlook

New workflows, including the 3D vertical integration of chip stacks, are developed to allow further miniaturisation and performance increase of devices. Within this thesis, three Cu pastes were characterized and experimentally investigated to establish a workflow for TCB to build up a wafer stack. The target was to condition the paste and define the parameter setup for the TCB process for each selected Cu paste.

CP3 has due to its narrow particle size distribution and specific binder chemistry a homogeneous pore distribution and a resulting smooth surface. The paste characterisation shows the correlations of its particle size distribution to the reduced R_q and layer thickness of CP3 after curing. The R_q of pre-conditioned pastes is in the range of the particle size. The R_q of micro-particle pastes can be reduced with a CMP treatment.

Other than with the unknown binder chemistry of each paste, the porosity correlates to the particle size distribution. Pastes containing nano-particles show closer packaging densities and therefore lower porosity. This influences the shrinkage of the printed layer during the thermal treatment. The resulting layer thickness is assumed to be dominated by the binder chemistry of the pastes. Due to higher initial contact area between the particles, pastes containing increasing proportions of nano-particles sinter at lower temperatures. Smaller particles have a higher free surface energy and therefore a lower activation force for the sinter process. The resistivity of the printed Cu pastes is connected to the porosity of the layer due to the higher defect density. With lower porosity values, the resistivity of the printed layer decreases. The pure nano-particle paste CP3 has a value of twice the resistivity of bulk Cu, while the pure micro-particle paste CP2 has a twentyfold resistivity compared to bulk Cu of $1.70 \mu\Omega\text{cm}$.

The best bonds, through TCB, are generally achieved for low pre-conditioning at a (T_C) of 250°C and a high bonding temperature (T_B) at 400°C for all three pastes. The shear strength reaches more than 40 MPa for CP1, 37.82 MPa for CP2 and 46.84 MPa for CP3. The additional annealing step shows slight improvements of the shear strength throughout the experiments to more than 40 MPa for CP1, 74.55 MPa for CP2 and 72.70 MPa for CP3. With the exception of CP3, higher bonding pressure (p_B) of 50 MPa relates to an increase of the bond quality in the tested pressure window. CP1 shows adequate bond strengths over the complete parameter setup of the TCB tests, while CP3 shows the highest bond strength for optimized bond parameters. The disadvantage of CP3 is its very selective process window during TCB due to the detected organic surface contamina-

tion, which is not fully removable through the pre-conditioning step. A CMP treatment is beneficial for CP1 and able to increase the shear strengths for TCB at lower pressures (p_B) of 15 MPa from 11.32 MPa to 23.36 MPa. CMP treated samples show lower shear strengths for high bonding pressures of 50 MPa due to the mechanical defects resulting from the CMP step. The shear strength decreases from more than 40 MPa before to 22.51 MPa after the CMP treatment.

The chemical cleaning of CP3 to remove the organic surface contamination is not suitable to increase the shear strength of TCB samples. The cleaning processes even decreases the bonding strength due to the visible surface roughening of CP3, through chemical degradation of its surface.

Subsequent work in the field of 3D vertical stacking has to focus primarily on reliability assurances to allow the integration of the technology on production level. The reliability and long term stability of the interconnects is very important for microelectronic devices and not yet tested for Cu TCB chip stacks. The parameter set of the workflow has to be optimized to be implemented into the work route of a FAB production workflow for chip assemblies. The printing of porous metal layers has a high potential for the manufacturing of thick metallisation layers on both the frontside and backside of chips. Additionally, the concept to combine the structured paste deposition with the stacking of full face wafers before dicing has to be investigated. This process will substitute the printing step and result in formation of homogeneous porous metal layers. The separated chips will be processed with the same TCB workflow of stencil printed samples.

List of References

- [1] E. P. DeBenedictis, M. Badaroglu, Chen, T. M. Conte, and P. Gargini, “Sustaining moore’s law with 3d chips”, *Computer*, vol. 50, no. 8, pp. 69–73, 2017, ISSN: 0018-9162. DOI: 10.1109/MC.2017.3001236.
- [2] Y. Tsutsui, K. Yamasaki, K. Maekawa, T. Niizeki, A. Bucheeri, M. Mita, Y. Matsuba, N. Terada, and H. Saito, “Size effect of ag nanoparticles on laser sintering and wire bondability”, in *Proceedings / 60th Electronic Components and Technology Conference (ECTC), 2010*, Piscataway, NJ: IEEE, 2010, pp. 1870–1876, ISBN: 978-1-4244-6410-4. DOI: 10.1109/ECTC.2010.5490705.
- [3] H. Clauberg, A. Marte, Y. Yang, J. Eder, T. Colosimo, D. Buergi, A. Rezvani, and B. Chylak, “High productivity thermocompression flip chip bonding”, in *Electronic Components and Technology Conference (ECTC) , 2015 IEEE 65th*, IEEE, 5/26/2015 - 5/29/2015, pp. 22–29, ISBN: 978-1-4799-8609-5. DOI: 10.1109/ECTC.2015.7159566.
- [4] A. V. Manoylov, F. M. Borodich, and H. P. Evans, “Modelling of elastic properties of sintered porous materials”, *Proceedings of the Royal Society A: Mathematical, Physical and Engineering Sciences*, vol. 469, no. 2154, p. 20120689, 2013, ISSN: 1364-5021. DOI: 10.1098/rspa.2012.0689.
- [5] A. K. Panigrahy and K.-N. Chen, “Low temperature cu–cu bonding technology in three-dimensional integration: An extensive review”, *Journal of Electronic Packaging*, vol. 140, no. 1, p. 3, 2018, ISSN: 1043-7398. DOI: 10.1115/1.4038392.
- [6] M. N. Rahaman, *Sintering of ceramics*. Boca Raton, FL: CRC Press, 2008, ISBN: 0849372860.
- [7] P. Liu and G.-F. Chen, *Porous materials: Processing and applications*. Amsterdam, Boston, and Paris: Elsevier and Butterworth-Heinemann, 2014, ISBN: 0124077889.
- [8] S.-J. L. Kang, *Sintering: Densification, grain growth, and microstructure*, ser. Materials science & engineering. Amsterdam: Elsevier, 2005, ISBN: 0750663855. [Online]. Available: <http://site.ebrary.com/lib/alltitles/docDetail.action?docID=10186221>.
- [9] J.-S. Zhang, *High temperature deformation and fracture of materials*. Woodhead Publishing, 2010, ISBN: 978-0-85709-079-9.
- [10] European Parliament, *Directive 2011/65/eu of the european parliament and of the council of 8 june 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment text with eea relevance of l 174*, 1.7.2011.

- [11] A. A. Wereszczak, B. R. Chen, and B. A. Oistad, "Reflow-oven-processing of pressureless sintered-silver interconnects", *Journal of Materials Processing Technology*, vol. 255, pp. 500–506, 2018, ISSN: 09240136. DOI: 10.1016/j.jmatprotec.2018.01.001.
- [12] *Copper, cu; cold drawn*. [Online]. Available: <http://www.matweb.com/search/DataSheet.aspx?MatGUID=1980eb23287a4408adc404dd39293942&ckck=1>.
- [13] M. Kajita, T. Takahashi, A. Kano, and T. Sato, "Development of a curable conductive copper paste in air", *Transactions of The Japan Institute of Electronics Packaging*, vol. 8, no. 1, pp. 151–155, 2015, ISSN: 1883-3365. DOI: 10.5104/jiepeng.8.151.
- [14] Schueler P., "Mechanische Eigenschaften und Versagensmechanismen offenzelliger Aluminiumschaum-Strukturen", PhD thesis, Technical University Berlin, Berlin, 2016.
- [15] R. Bowman, L. Peters, and D. Potter, *Cost effective IC manufacturing, 1998-1999*. Scottsdale, Ariz.: Integrated Circuit Engineering Corp, 1997, ISBN: 1-877750-60-3.
- [16] J. W. Gardner, V. K. Varadan, and O. O. Awadelkarim, *Microsensors, MEMS, and smart devices*. Chichester and New York: J. Wiley, 2010, ISBN: 1601190816. DOI: 10.1002/9780470846087. [Online]. Available: <http://onlinelibrary.wiley.com/book/10.1002/9780470846087>.
- [17] J. Knechtel, O. Sinanoglu, I. M. Elfadel, J. Lienig, and C. C. N. Sze, "Large-scale 3d chips: Challenges and solutions for design automation, testing, and trustworthy integration", *IPSJ Transactions on System LSI Design Methodology*, vol. 10, no. 0, pp. 45–62, 2017. DOI: 10.2197/ipsjtsldm.10.45.
- [18] G.-S. Park, Y.-K. Kim, K.-K. Paek, J.-S. Kim, J.-H. Lee, and B.-K. Ju, "Low-temperature silicon wafer-scale thermocompression bonding using electroplated gold layers in hermetic packaging", *Electrochemical and Solid-State Letters*, vol. 8, no. 12, G330, 2005, ISSN: 0254-0584. DOI: 10.1149/1.2077077.
- [19] H. Takeuchi, A. Wung, X. Sun, R. T. Howe, and T.-J. King, "Thermal budget limits of quarter-micrometer foundry cmos for post-processing mems devices", *IEEE Transactions on Electron Devices*, vol. 52, no. 9, pp. 2081–2086, 2005, ISSN: 0018-9383. DOI: 10.1109/TED.2005.854287.
- [20] T. Fukushima, H. Hashiguchi, H. Yonekura, H. Kino, M. Murugesan, J.-C. Bea, K.-W. Lee, T. Tanaka, and M. Koyanagi, "Oxide-oxide thermocompression direct bonding technologies with capillary self-assembly for multichip-to-wafer heterogeneous 3d system integration", *Micromachines*, vol. 7, no. 10, 2016, ISSN: 2072-666X. DOI: 10.3390/mi7100184.

- [21] C. Huyghebaert, J. van Olmen, Y. Civale, A. Phommahaxay, A. Jourdain, S. Sood, S. Farrens, and P. Soussan, “Cu to cu interconnect using 3d-tsv and wafer to wafer thermocompression bonding”, in *International Interconnect Technology Conference (IITC), 2010*, Piscataway, NJ: IEEE, 2010, pp. 1–3, ISBN: 978-1-4244-7676-3. DOI: 10.1109/IITC.2010.5510444.
- [22] J. Fan, D. F. Lim, and C. S. Tan, “Effects of surface treatment on the bonding quality of wafer-level cu-to-cu thermo-compression bonding for 3d integration”, *Journal of Micromechanics and Microengineering*, vol. 23, no. 4, p. 045 025, 2013, ISSN: 0741-3106. DOI: 10.1088/0960-1317/23/4/045025.
- [23] P. Gagnon, C. Bergeron, R. Langlois, S. Barbeau, S. Whitehead, C. Tyberg, R. Robertazzi, K. Sakuma, M. Wordeman, and M. Scheurmann, “Thermo-compression bonding and mass reflow assembly processes of 3d logic die stacks”, in *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, IEEE, 30.05.2017 - 02.06.2017, pp. 116–122, ISBN: 978-1-5090-6315-4. DOI: 10.1109/ECTC.2017.53.
- [24] R. Kay and M. Desmulliez, “A review of stencil printing for microelectronic packaging”, *Soldering & Surface Mount Technology*, vol. 24, no. 1, pp. 38–50, 2012, ISSN: 0954-0911. DOI: 10.1108/09540911211198540.
- [25] L. D. Carro, J. Zuercher, S. Gerke, T. Wildsmith, G. Ramos, and T. Brunswiler, “Morphology of low-temperature all-copper interconnects formed by dip transfer”, in *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, IEEE, 30.05.2017 - 02.06.2017, pp. 961–967, ISBN: 978-1-5090-6315-4. DOI: 10.1109/ECTC.2017.123.
- [26] D. Manassis, R. Patzelt, A. Ostmann, R. Aschenbrenner, and H. Reichl, “Technical challenges of stencil printing technology for ultra fine pitch flip chip bumping”, *Microelectronics Reliability*, vol. 44, no. 5, pp. 797–803, 2004, ISSN: 0026-2714. DOI: 10.1016/S0026-2714(03)00361-5.
- [27] Ichikawa T., Sugo Y., Shimoda M., Mita R., “Composition for sinter bonding, sheet for sinter bonding, and dicing tape having sheet for sinter bonding”, WO2019092960, 2019. [Online]. Available: <https://patentscope.wipo.int/search/en/detail.jsf?docId=W02019092960&tab=PCTBIBLIO>.
- [28] Y. Gao, W. Li, C. Chen, H. Zhang, J. Jiu, C.-F. Li, S. Nagao, and K. Suganuma, “Novel copper particle paste with self-reduction and self-protection characteristics for die attachment of power semiconductor under a nitrogen atmosphere”, *Materials & Design*, vol. 160, pp. 1265–1272, 2018, ISSN: 0264-1275. DOI: 10.1016/j.matdes.2018.11.003. [Online]. Available: <http://www.sciencedirect.com/science/article/pii/S0264127518308098>.

- [29] S. Hascoët, C. Buttay, D. Planson, R. Chiriac, and A. Masson, “Pressureless silver sintering die-attach for sic power devices”, *Materials Science Forum*, vol. 740-742, pp. 851–854, 2013. DOI: 10.4028/www.scientific.net/MSF.740-742.851.
- [30] Eichinger B., “Characterization of stencil-printed copper sinter pastes and use cases for implementation in semiconductor industry”, PhD thesis, University of Graz, Graz, 2020.
- [31] K. N. Chen, C. S. Tan, A. Fan, and R. Reif, “Copper bonded layers analysis and effects of copper surface conditions on bonding quality for three-dimensional integration”, *Journal of Electronic Materials*, vol. 34, no. 12, pp. 1464–1467, 2005, ISSN: 0361-5235. DOI: 10.1007/s11664-005-0151-0.
- [32] J. H. Hsieh, L. H. Fong, S. Yi, and G. Metha, “Plasma cleaning of copper leadframe with Ar and Ar/H₂ gases”, *Surface and Coatings Technology*, vol. 112, no. 1-3, pp. 245–249, 1999, ISSN: 0257-8972. DOI: 10.1016/S0257-8972(98)00779-8.
- [33] L. Zafonte and R. Chiu, “Uv/ozone cleaning for organics removal on silicon wafers”, in *Optical Microlithography III: Technology for the Next Decade*, H. L. Stover, Ed., ser. SPIE Proceedings, SPIE, 1984, p. 164. DOI: 10.1117/12.941910.
- [34] D. W. Peters, “Corrosion and passivation of copper”, in *Handbook of cleaning for semiconductor manufacturing*, K. A. Reinhardt and R. F. Reidy, Eds., vol. 145, Salem, Mass. and Hoboken, N.J.: Scrivener and John Wiley & Sons, 2011, pp. 395–428, ISBN: 9781118071748. DOI: 10.1002/9781118071748.ch11.
- [35] Y. Yong, M. T. Nguyen, H. Tsukamoto, M. Matsubara, Y.-C. Liao, and T. Yonezawa, “Effect of decomposition and organic residues on resistivity of copper films fabricated via low-temperature sintering of complex particle mixed dispersions”, *Scientific Reports*, vol. 7, p. 45150, 2017. DOI: 10.1038/srep45150.
- [36] H. Park and S. E. Kim, “Two-step plasma treatment on copper surface for low temperature cu thermo-compression bonding”, *IEEE Transactions on Components, Packaging and Manufacturing Technology*, p. 1, 2019, ISSN: 2156-3950. DOI: 10.1109/TCPMT.2019.2928323.
- [37] M. Samouhos, A. Peppas, P. Angelopoulos, M. Taxiarchou, and P. Tsakiridis, “Optimization of copper thermocompression diffusion bonding under vacuum: Microstructural and mechanical characteristics”, *Metals*, vol. 9, no. 10, p. 1044, 2019. DOI: 10.3390/met9101044.

- [38] N. Malik, K. Schjølberg-Henriksen, E. Poppe, M. Taklo, and T. G. Finstad, “Alal thermocompression bonding for wafer-level mems sealing”, *Sensors and Actuators A: Physical*, vol. 211, pp. 115–120, 2014, ISSN: 09244247. DOI: 10.1016/j.sna.2014.02.030.
- [39] P. Ramm, J. J.-Q. Lu, and M. M. V. Taklo, Eds., *Handbook of wafer bonding*. Weinheim, Germany: Wiley-VCH, 2012, ISBN: 9783527326464. DOI: 10.1002/9783527644223. [Online]. Available: <http://site.ebrary.com/lib/alltitles/docDetail.action?docID=10529302>.
- [40] X. Luan, Y. Liu, C. Wang, X. Niu, J. Wang, and W. Zhang, “A study on exploring the alkaline copper cmp slurry without inhibitors to achieve high planarization efficiency”, *Microelectronic Engineering*, vol. 160, pp. 5–11, 2016, ISSN: 01679317. DOI: 10.1016/j.mee.2016.02.044.
- [41] J. Dietz, “Scientific characterisation of copper composites for semiconductor applications”, Master Thesis, Technical University Dresden, Dresden, 2018.
- [42] Karner S., “Three-dimensional integration of power electronic devices sing wafer level deposited copper sinter paste”, Master Thesis, Montanuniversity Leoben, Leoben, 2019.
- [43] *Dek horizon 02i*. [Online]. Available: https://www.pmtech.co.uk/pdfs/TDS/Equipment/dek/dek%5C_horizon02i%5C_TDS.pdf.
- [44] *Chad wafer mate 200*. [Online]. Available: https://www.chadautomation.com/dam/jcr:318f65ea-e489-43e1-a34d-cc8e02ef5375/WaferMate200%5C%20_JabilChadAutomation%5C_AutomationSheet%5C_web.pdf.
- [45] *Yield engineering systems (yes): Quality process equipment built for process engineers*. [Online]. Available: <https://www.yieldengineering.com/>.
- [46] *Sro-700 table top – ir vacuum reflow system*. [Online]. Available: <https://www.atv-tech.com/sro-700>.
- [47] *T.i.p.s. - technical innovation - physical solutions*, 7.11.2019. [Online]. Available: <https://www.tips.co.at/>.
- [48] *Fineplacer*. [Online]. Available: <https://www.finetech.de/de/produkte/uebersicht/fineplacerr-lambda/>.
- [49] I. Miccoli, F. Edler, H. Pfnür, and C. Tegenkamp, “The 100th anniversary of the four-point probe technique: The role of probe geometries in isotropic and anisotropic systems”, *Journal of physics. Condensed matter : an Institute of Physics journal*, vol. 27, no. 22, p. 223 201, 2015. DOI: 10.1088/0953-8984/27/22/223201.

- [50] L. J. van der Pauw, “A method of measuring specific resistivity and hall effect of discs of arbitrary shape”, in *Semiconductor devices*, S. M. Sze, Ed., Singapore and [Teaneck], N.J.: WORLD SCIENTIFIC, 1991, pp. 174–182, ISBN: 978-981-02-0209-5. DOI: 10.1142/9789814503464{\textunderscore}0017.
- [51] J. C. Li, Y. Wang, and D. C. Ba, “Characterization of semiconductor surface conductivity by using microscopic four-point probe technique”, *Physics Procedia*, vol. 32, pp. 347–355, 2012, ISSN: 18753892. DOI: 10.1016/j.phpro.2012.03.568.
- [52] *Olympus mx61l*. [Online]. Available: www.bbmicro.com/products/file/MX61%5C_61L%5C_51%5C_UIS2%20012207.pdf.
- [53] *Hitachi su-8010*. [Online]. Available: <https://www.hitachi-hightech.com/global/about/news/2011/nr20110214.html>.
- [54] *S neox specifications - dimensions, options & accessories*. [Online]. Available: <https://www.sensofar.com/metrology/sneox/specifications/>.
- [55] *Up to 8" resmap 178 - cpa - creative design engineering*, 22.12.2019. [Online]. Available: <https://cde-resmap.com/up-to-8-resmap-178/>.
- [56] *Coretech integrated limited*. [Online]. Available: <http://www.coretechint.com/product.php?category=3&product=4>.
- [57] *Gen6 | csam | acoustic micro imaging | scanning acoustic microscope - sonoscan, inc.* [Online]. Available: <https://sonoscan.com/instruments/gen6>.
- [58] X. B. V, *Condor sigma bond tester - shear, push and pull testing*. [Online]. Available: <https://www.xyztec.com/en/condor-sigma/>.
- [59] c. H. AG, *Cornerstone (application)*. [Online]. Available: <https://www.camline.com/de/produkte/cornerstone/cornerstone-application.html>.
- [60] *R: The r project for statistical computing*, 12.12.2019. [Online]. Available: <https://www.r-project.org/>.
- [61] L. M. Collins, J. J. Dziak, and R. Li, “Design of experiments with multiple independent variables: A resource management perspective on complete and reduced factorial designs”, *Psychological methods*, vol. 14, no. 3, pp. 202–224, 2009, ISSN: 1082-989X. DOI: 10.1037/a0015826.
- [62] F. S. Nahm, “What the p values really tell us”, *The Korean Journal of Pain*, vol. 30, no. 4, pp. 241–242, 2017, ISSN: 2005-9159. DOI: 10.3344/kjp.2017.30.4.241.
- [63] R. C. Craft and C. Leake, “The pareto principle in organizational decision making”, *Management Decision*, vol. 40, no. 8, pp. 729–733, 2002, ISSN: 0025-1747. DOI: 10.1108/00251740210437699.

- [64] Williamson, D & Parker, RA & Kendrick, Juliette, “The box plot: A simple visual method to interpret data”, *Annals of internal medicine*, 1989.
- [65] V. Strejc, “Least squares parameter estimation”, *IFAC Proceedings Volumes*, vol. 12, no. 8, pp. 535–550, 1979, ISSN: 14746670. DOI: 10.1016/S1474-6670(17)53975-0.
- [66] A. Schneider, G. Hommel, and M. Blettner, “Linear regression analysis: Part 14 of a series on evaluation of scientific publications”, *Deutsches Arzteblatt international*, vol. 107, no. 44, pp. 776–782, 2010. DOI: 10.3238/arztebl.2010.0776.
- [67] *Introduction to imagej*, 26.11.2019. [Online]. Available: <https://imagej.net/Introduction>.
- [68] J. Li, T. Shi, C. Feng, Q. Liang, X. Yu, J. Fan, S. Cheng, G. Liao, and Z. Tang, “The novel cu nanoaggregates formed by 5 nm cu nanoparticles with high sintering performance at low temperature”, *Materials Letters*, vol. 216, pp. 20–23, 2018, ISSN: 0167577X. DOI: 10.1016/j.matlet.2017.12.094.
- [69] S. Özbilen, “Satellite formation mechanism in gas atomised powders”, *Powder Metallurgy*, vol. 42, no. 1, pp. 70–78, 1999, ISSN: 0032-5899. DOI: 10.1179/pom.1999.42.1.70.
- [70] an Harvey Arellano, “Fingerprints of epoxy bleed-out on porous ceramic surface”, *International Research Journal of Advanced Engineering and Science*, vol. 4, no. 3, pp. 198–201, 2019.
- [71] K. J. Puttlitz and K. A. Stalter, *Handbook of lead-free solder technology for micro-electronic assemblies*, ser. Mechanical engineering. New York: Marcel Dekker, 2004, vol. 170, ISBN: 0-8247-4870-0.
- [72] A. Briggs, Ed., *Advances in acoustic microscopy*. New York: Springer Science+Business Media, LLC, 1995, ISBN: 978-1-4615-1873-0.
- [73] A. Haris, D. Witten, and N. Simon, “Convex modeling of interactions with strong heredity”, *Journal of computational and graphical statistics : a joint publication of American Statistical Association, Institute of Mathematical Statistics, Interface Foundation of North America*, vol. 25, no. 4, pp. 981–1004, 2016, ISSN: 1061-8600. DOI: 10.1080/10618600.2015.1067217.
- [74] Y. Tang, R. Zhou, H. Li, W. Yuan, and L. Lu, “Experimental study on the tensile strength of a sintered porous metal composite”, *Materials Science and Engineering: A*, vol. 607, pp. 536–541, 2014, ISSN: 09215093. DOI: 10.1016/j.msea.2014.04.039.

- [75] Stamoulis Konstantinos, “Mechanics aspects of wafer thermocompression bonding”, Master thesis, Massachusetts Institute of Technology, Cambridge, 2005. [Online]. Available: <https://pdfs.semanticscholar.org/f60c/1b23eb3547134e618f07a192c73e7907b77a.pdf>.
- [76] Dillinger F., “Process development of thermal sintering processes for printable cu pastes on semiconductor wafers”, unpublished Master thesis, Technical University Vienna, Vienna, 2020.
- [77] J. Montes, F. Cuevas, J. Cintas, F. Ternero Fernández, and E. Caballero, *Electrical Resistivity of Powdered Porous Compacts*. Jan. 2019, ISBN: 978-1-78984-929-5. DOI: 10.5772/intechopen.76159.
- [78] T. F. Murphy, B. A. Lindsley, and C. T. Schade, “A metallographic examination into fatigue-crack initiation and growth in ferrous pm materials”, 2013.
- [79] D. Ishikawa, H. Nakako, Y. Kawana, C. Sugama, M. Negishi, Y. Ejiri, S. Ueda, B. N. An, H. Wurst, B. Leyrer, T. Blank, and M. Weber, “Copper die-bonding sinter paste: Sintering and bonding properties”, in *2018 7th Electronic System-Integration Technology Conference (ESTC)*, [S.l.]: IEEE, 9/18/2018 - 9/21/2018, pp. 01–10, ISBN: 978-1-5386-6814-6. DOI: 10.1109/ESTC.2018.8546455.
- [80] J.-W. Yoon and J.-H. Back, “Effect of sintering conditions on the mechanical strength of cu-sintered joints for high-power applications”, *Materials (Basel, Switzerland)*, vol. 11, no. 11, 2018, ISSN: 1996-1944. DOI: 10.3390/ma11112105.
- [81] H. Nishikawa, T. Hirano, and T. Takemoto, “Bonding process of cu/cu joint using cunanoparticle paste”, *Transactions of JWRI.*, vol. 40 (2), P.33–P.36, 2011-12. [Online]. Available: <http://hdl.handle.net/11094/5952>.
- [82] W. Zhou and Z. L. Wang, *Scanning microscopy for nanotechnology: Techniques and applications*. New York, NY: Springer, 2007, ISBN: 9780387333250. DOI: 10.1007/978-0-387-39620-0. [Online]. Available: <http://site.ebrary.com/lib/alltitles/docDetail.action?docID=10161201>.
- [83] F. Bertocci, A. Grandoni, and T. Djuric-Rissner, “Scanning acoustic microscopy (sam): A robust method for defect detection during the manufacturing process of ultrasound probes for medical imaging”, *Sensors*, vol. 19, p. 4868, Nov. 2019. DOI: 10.3390/s19224868.

Appendices

A Analytical Equipment

A.1 Scanning Electron Microscope

The scanning electron microscope (SEM) is a widely used device for morphological and chemical analyses. The SEM utilizes an electron beam in a high vacuum atmosphere. The electron beam is accelerated to energy levels between 0.1 keV and 30 keV. The maximum resolution limit of a SEM with an electron beam energy of 30 keV is approximately 0.4 nm, as given by Abbe's equation. Equation 9 describes the minimum distance of two points, that can be distinguished in the optical analysis. The distance d is calculated through the wavelength of the input signal λ and the numeric aperture NA [82].

$$d = \frac{0.612 * \lambda}{NA} \quad (9)$$

The electron beam can generate elastic and inelastic interactions with the measured sample. The generated interactions on the sample are, as depicted in Figure A.1, Auger electrons, secondary electrons, backscatter electrons and characteristic x-rays.

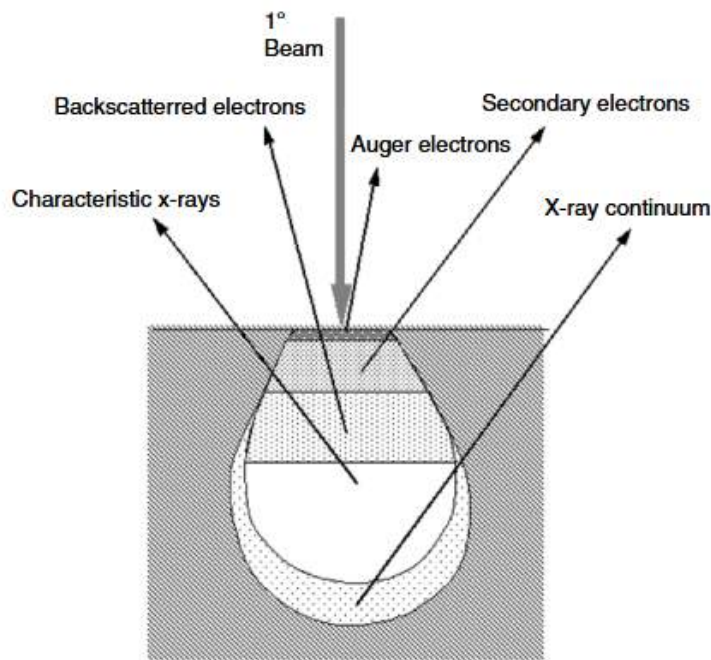


Figure A.1. Illustration of the interaction volume of elastic and inelastic interactions of the electron beam with the measured sample [82].

Within this thesis, the scanning electron microscopes SU8010 and S4800 from Hitachi, depicted in Figure A.2 were used for the morphological analysis of pre-conditioned copper pastes. The morphological image analysis utilized secondary electrons.



Figure A.2. The surface electron microscope (SEM) S4800 from Hitachi.

Auger electron analyses of the pre-conditioned copper pastes were performed to measure the surface contamination of the copper pastes. The chemical composition on the surface can be assessed due to the characteristic energy levels of the generated Auger electrons. The Auger electrons carry away the excess energy of the ionisation of surface atoms. The excess energy of the Auger electrons is characteristic for each element. The energy of these Auger electrons is quite low and therefore Auger electrons have a low penetration depth of only a few nm [82].

A.2 Optical Profiler

The 3D optical profiler S Neox from Sensofar depicted in Figure A.3 measures the surface topography of a sample through the confocal reflection of a light source. The profiler utilizes a monochromatic light source to generate an image stack in z-direction and combine them into a single topological image. The z coordinate of a position on the sample is determined by the profiler through alternating the focal plane of the light source in z-direction and calculating the positions of the return signals in the focal plane on the sample. An algorithm calculates the topography of the sample from the signals. The profiler can measure fast line profiles and 3D areal scans.



Figure A.3. The optical profiler S Neox from Sensofar.

A.3 RESMAP

The RESMAP 178 from CDE Inc. depicted in Figure A.4 is an automated wafer level tool for surface resistance measurement. It can automatically measure wafers and wafer fragments of up to 8". It utilises the four-point probe technique described in Section 3.2.4.1. The tool was used to measure the surface resistance of the full face printed and pre-conditioned copper paste layers on Si wafers. The measured positions were defined in a set radial pattern.



Figure A.4. The RESMAP 178 from CDE Inc.

A.4 Scanning Acoustic Microscopy

The scanning acoustic microscope (SAM) is a non-destructive imaging device. The SAM utilizes ultrasonic waves of up to 300 GHz to penetrate the measured samples. The acoustic wave is generated by a piezoelectric transducer and focused via acoustic lenses before reaching the sample. The acoustic wave is transmitted to the surface of the sample through a fluid film, which is most commonly distilled water. The contrast of the resulting image depends on the acoustic properties of the materials in the measured sample, such as reflectivity. The SAM imaging can identify interfaces, voids, inclusions and delaminations through the change of the acoustic impedance, as depicted in Figure A.5. The results are displayed in a contrast image [83].

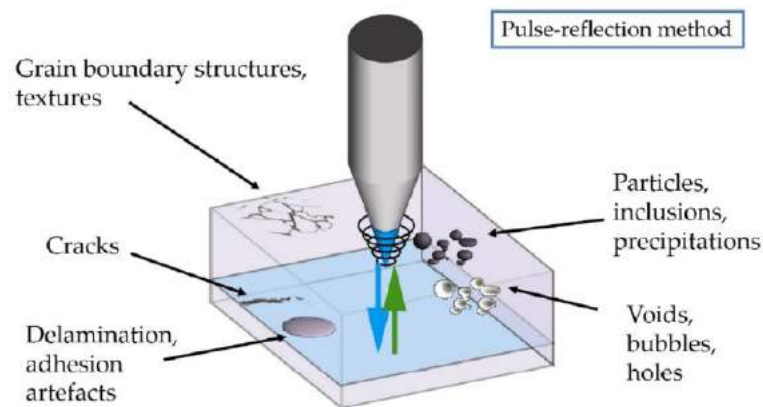


Figure A.5. Schematic of a scanning acoustic microscope (SAM) [83].

The SAM used within this thesis to illustrate the properly bonded area of the chip stack was the Sonoscan Gen6 depicted in Figure A.6.



Figure A.6. The Sensoscan Gen6.

A.5 Shear Tester

The shear tester Condor Sigma from XYZTEC depicted in Figure A.7 was used to measure the shear strength of the TCB samples in the bonding DoEs.



Figure A.7. Shear tester Condor Sigma from XYZTEC.

The shear tester applies a shear force by pressing a shear head against the side wall of the top chip of the bonded sample. The shear tester maps a force-displacement diagram, as depicted in Figure 5.9. The maximum force at the point of the initiation of critical crack growth is catalogued as the bonding strength of the sample. The sheared sample is documented with an image by an integrated camera.

B Results

B.1 Auger Electron Spectroscopy of the Sinter Pastes

The surfaces of the pre-conditioned sinter pastes was analysed by Auger electron spectroscopy to determine their cleanliness. The cleanliness of the surface is an important parameter for the bondability of the sinter pastes. Organic residues on the surface can hinder the formation of a sinter connection of the pre-conditioned sinter paste layer on the bottom chip and the metallisation of the top chip.

The Auger electron analysis was combined with a focussed ion beam (FIB) ablation to generate a limited depth profile of the measured samples. The ablation time of 2 min equals an ablated depth of 14 nm. The Auger electron spectroscopy depth profile of pre-conditioned CP1 depicted in Figure B.1 shows a high carbon level on the surface, which decreases rapidly. CP1 shows low oxygen levels throughout the depth profile. The Auger electron spectroscopy depth profile of pre-conditioned CP2 depicted in Figure B.2 shows a high oxygen level on the surface, which decreases rapidly in depth. The carbon level in CP2 is low throughout the depth profile. The Auger electron spectroscopy depth profile of pre-conditioned CP3 depicted in Figure B.3 indicates a significantly higher carbon contamination on the surface, which steadily decreases in depth. CP3 shows almost no oxygen throughout the depth profile. The difference in the carbon and oxygen contamination between the copper pastes stem from the distinctive organic additives of the copper pastes. The Auger electron spectroscopy depth profile of pre-conditioned CP1 after an additional CMP treatment depicted in Figure B.4 evidences a change of the organic residue throughout the depth profile, but no additional elemental contamination through the CMP treatment.

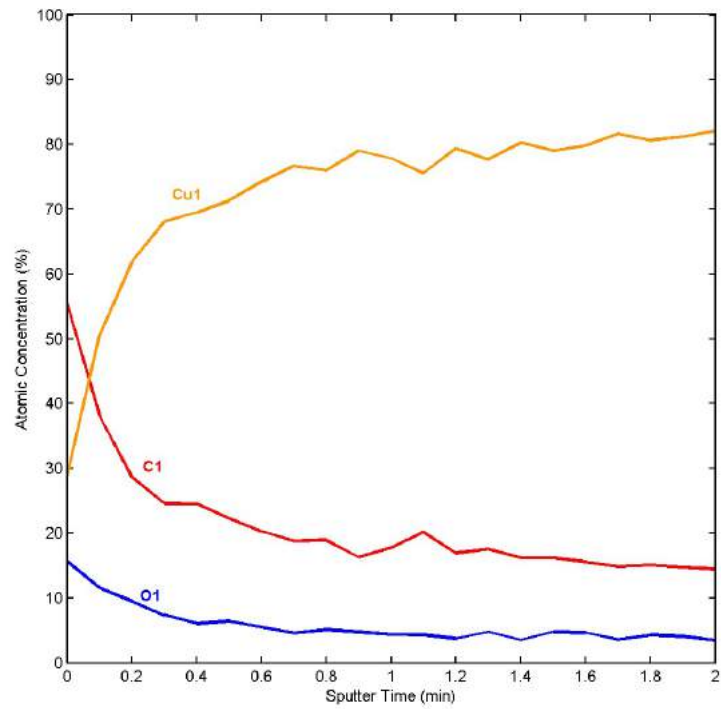


Figure B.1. Auger electron spectroscopy depth profile of a pre-conditioned CP1 wafer.

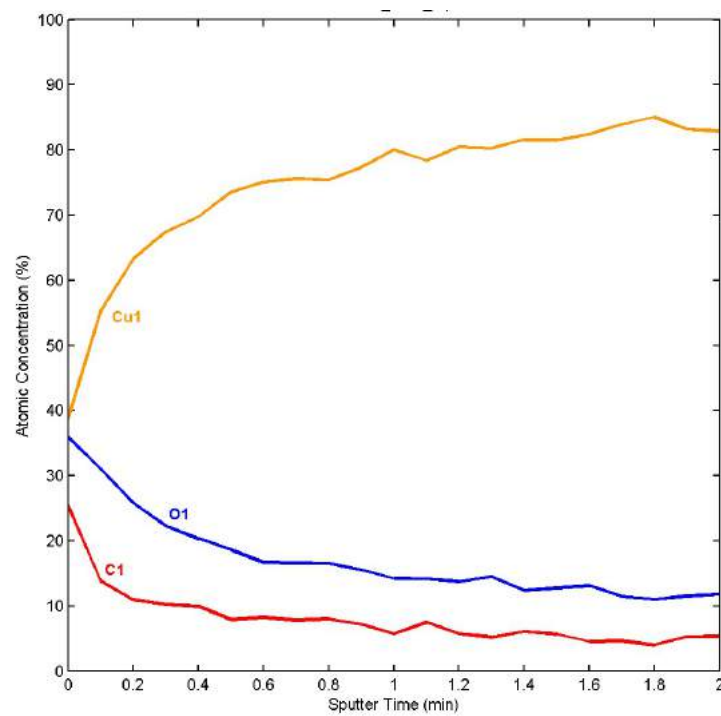


Figure B.2. Auger electron spectroscopy depth profile of a pre-conditioned CP2 wafer.

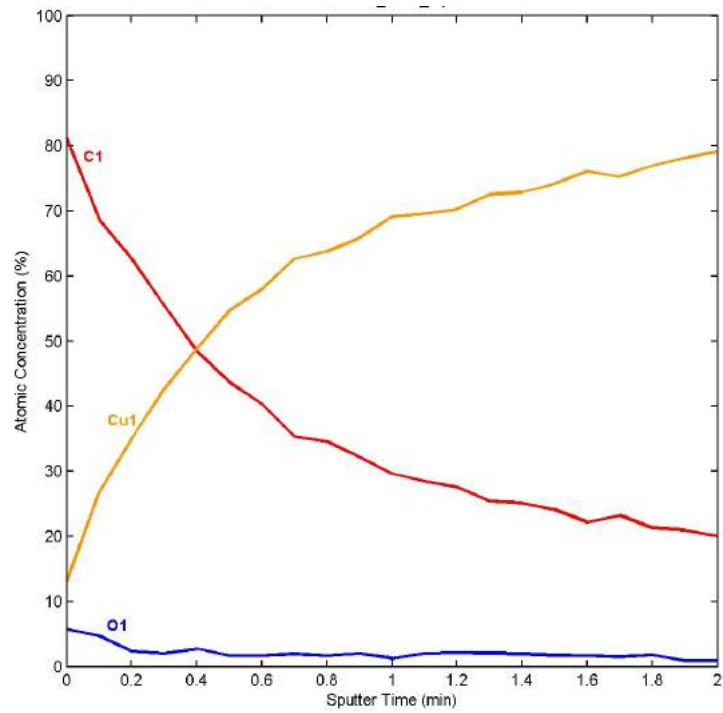


Figure B.3. Auger electron spectroscopy depth profile of a pre-conditioned CP3 wafer.

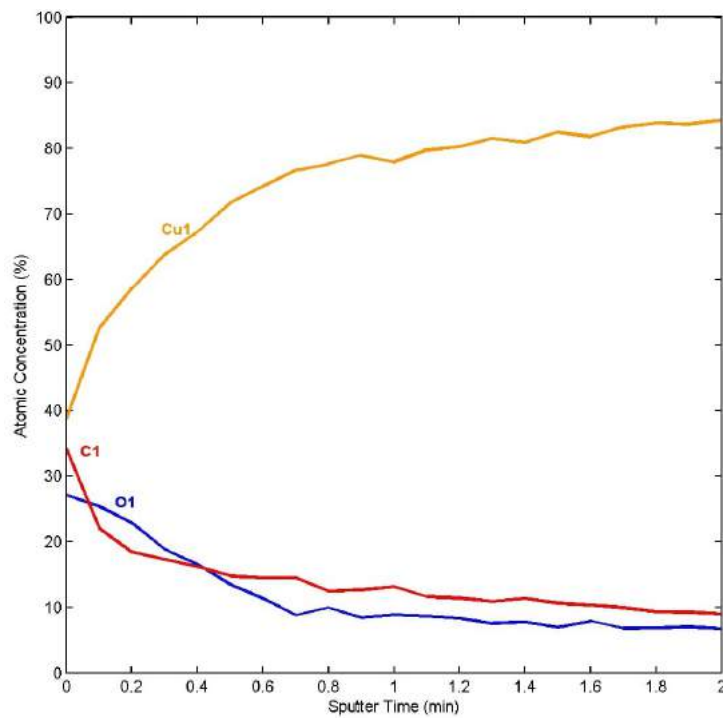


Figure B.4. Auger electron spectroscopy depth profile of a pre-conditioned CP1 wafer after an additional CMP treatment.

B.2 Surface Profiling of the CMP treated wafers

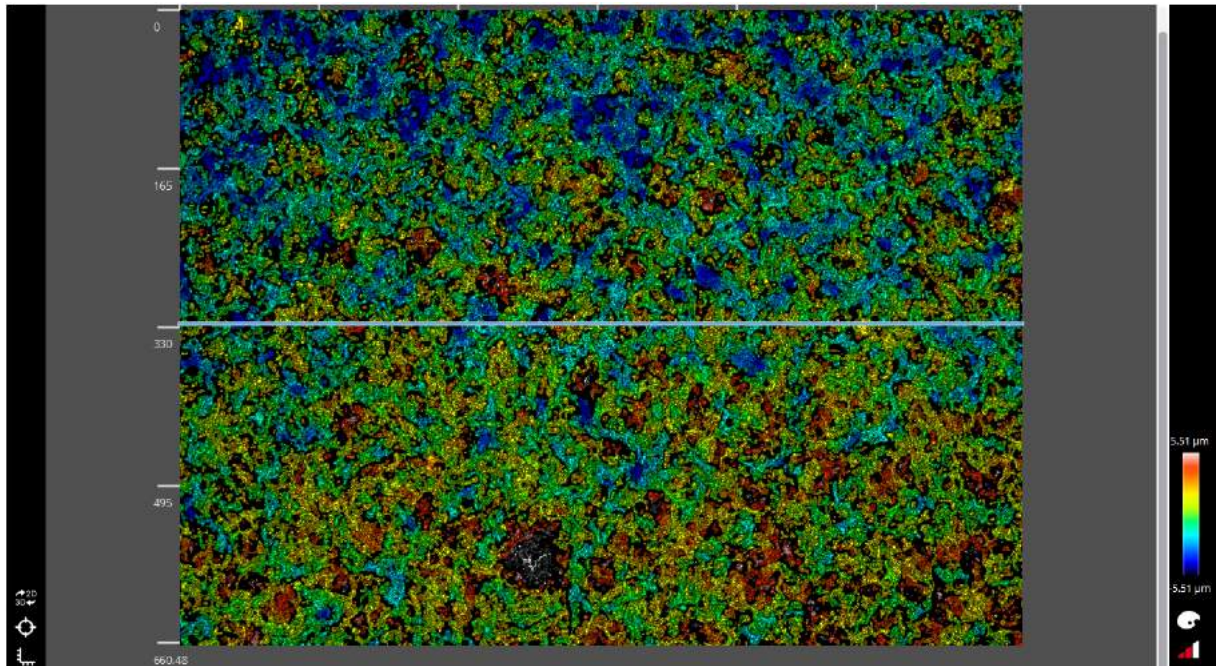


Figure B.5. False color topological image of sample CP1_0 of the CMP DoE of pre-conditioned CP1.

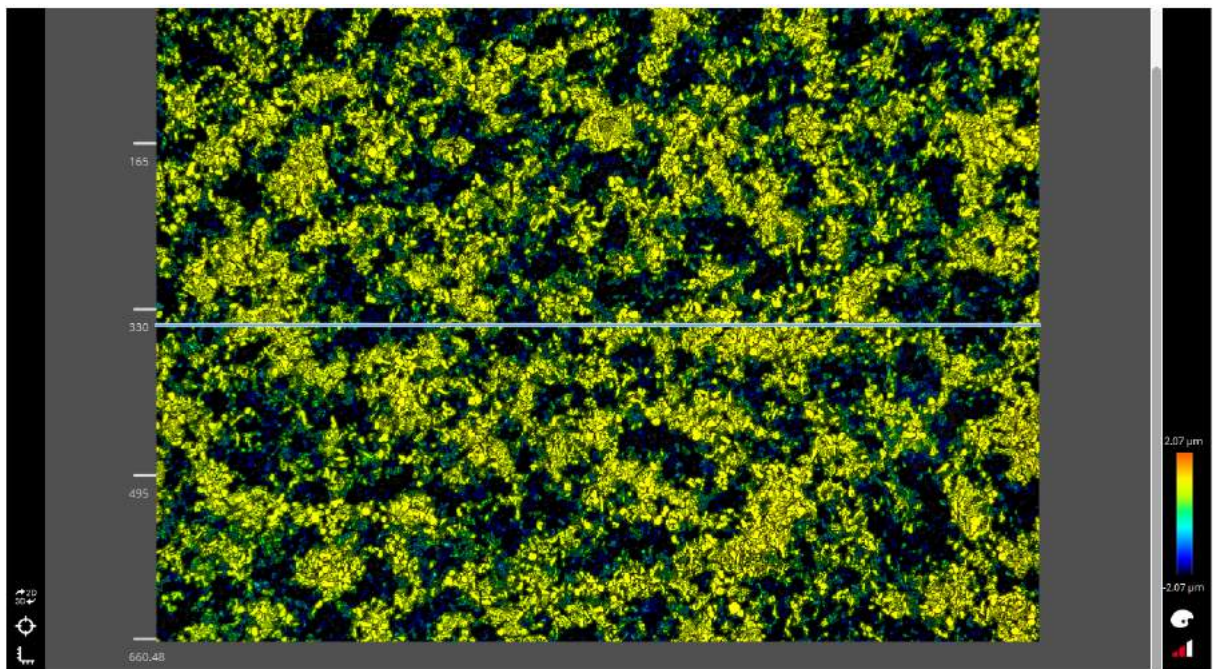


Figure B.6. False color topological image of sample CP1_120 of the CMP DoE of pre-conditioned CP1.

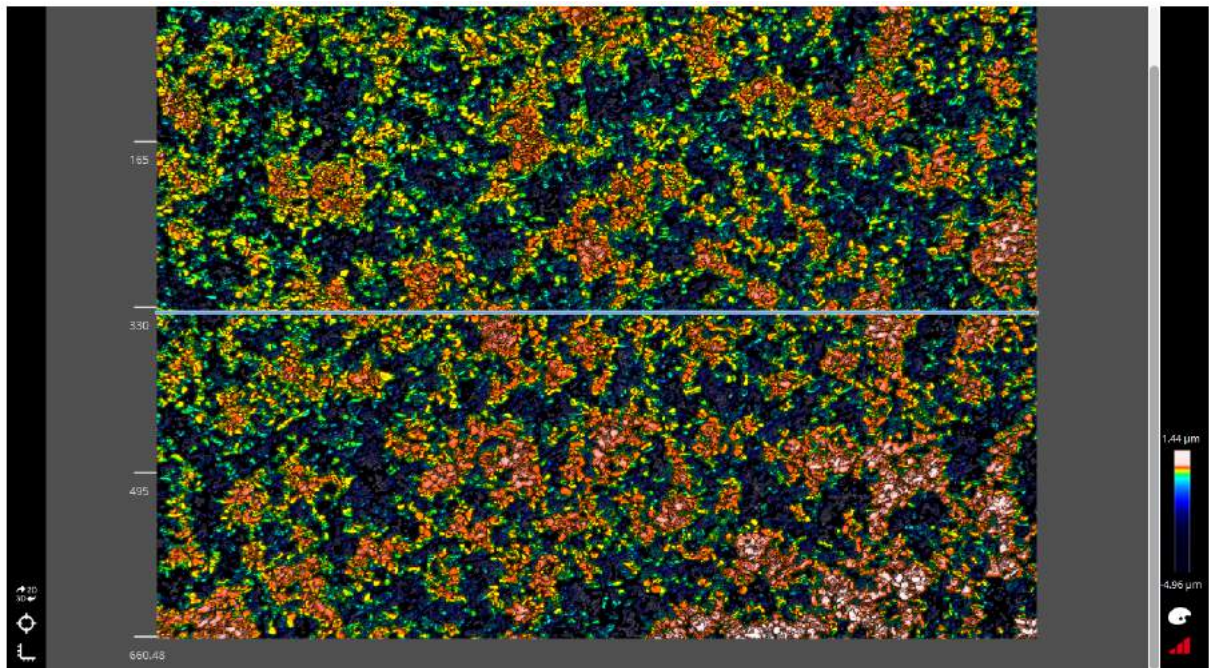


Figure B.7. False color topological image of sample CP1_180 of the CMP DoE of pre-conditioned CP1.

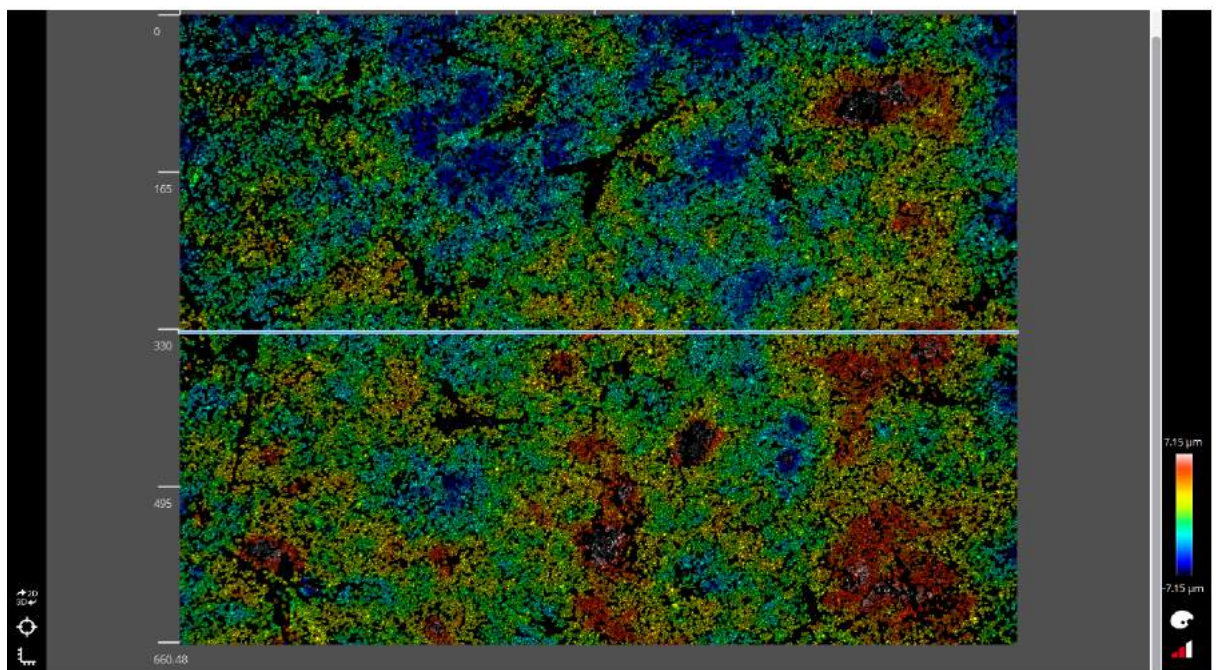


Figure B.8. False color topological image of sample CP2_0 of the CMP DoE of pre-conditioned CP1.

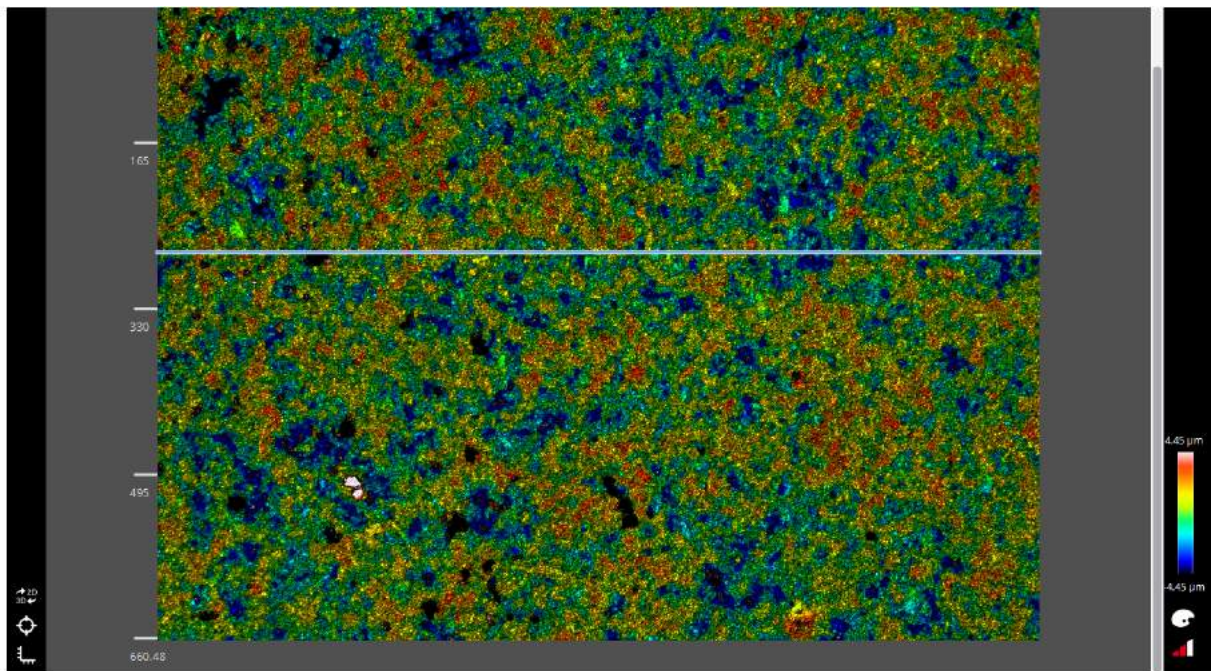


Figure B.9. False color topological image of sample CP2_120 of the CMP DoE of pre-conditioned CP1.

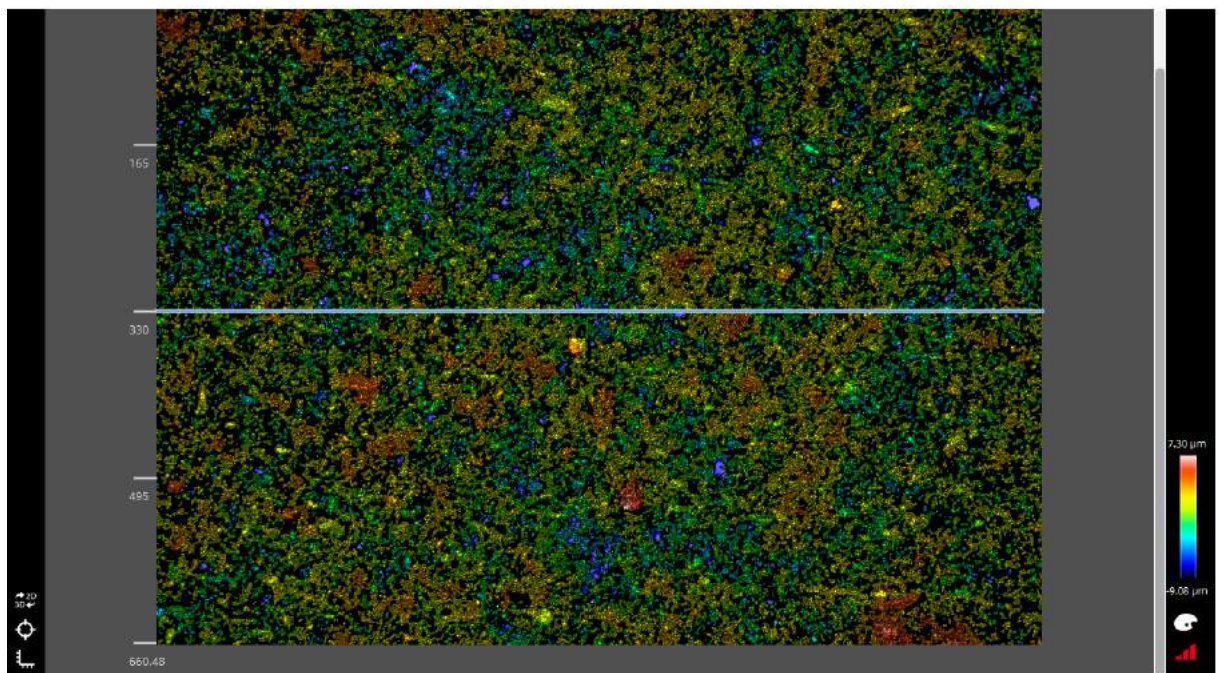
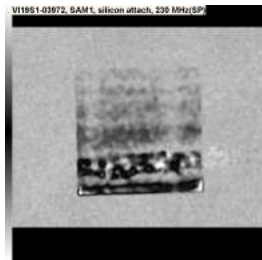


Figure B.10. False color topological image of sample CP2_180 of the CMP DoE of pre-conditioned CP1.

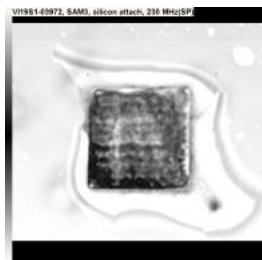
B.3 CP2 DoE



Sample 1 SAM



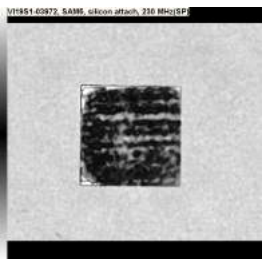
Sample 2 SAM



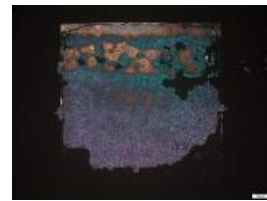
Sample 3 SAM



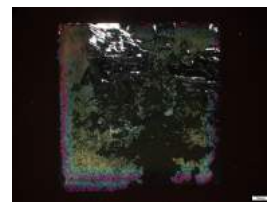
Sample 4 SAM



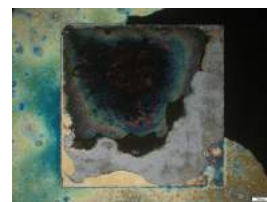
Sample 5 SAM



Sample 1 shear test



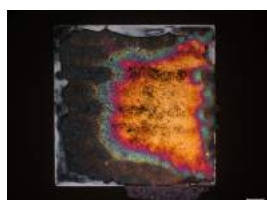
Sample 2 shear test



Sample 3 shear test



Sample 4 shear test



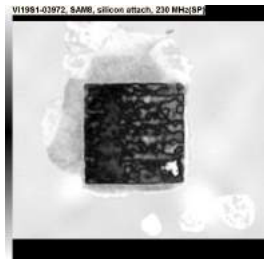
Sample 5 shear test



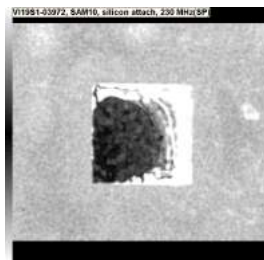
Sample 6 SAM



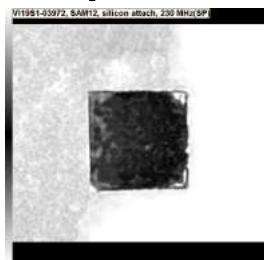
Sample 7 SAM



Sample 8 SAM



Sample 12 SAM



Sample 16 SAM



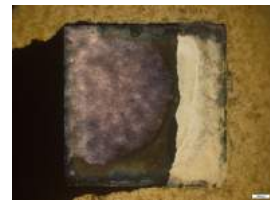
Sample 6 shear test



Sample 7 shear test



Sample 8 shear test



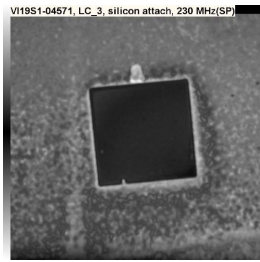
Sample 12 shear test



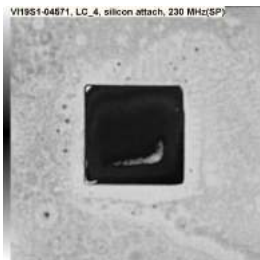
Sample 16 shear test

Figure B.11. SAM images and images of the samples after the shear test for the CP2 bonding DoE.

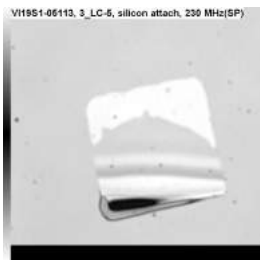
B.4 CP3 DoE



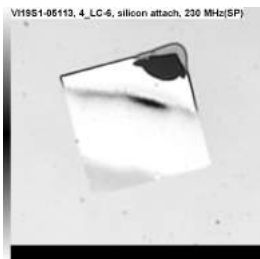
Sample 3 SAM



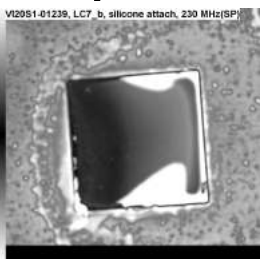
Sample 4 SAM



Sample 5 SAM



Sample 6 SAM



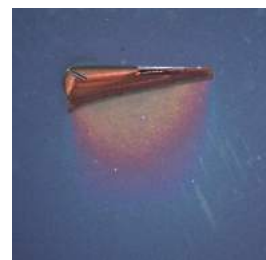
Sample 7 SAM



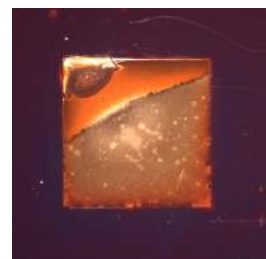
Sample 3 shear test



Sample 4 shear test



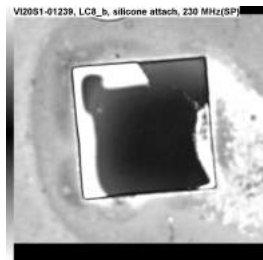
Sample 5 shear test



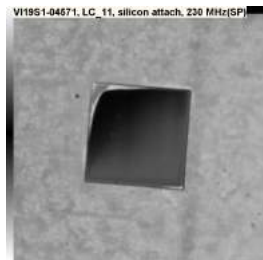
Sample 6 shear test



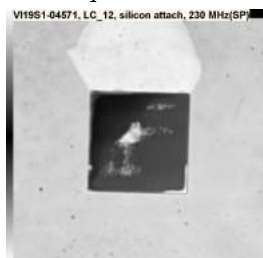
Sample 7 shear test



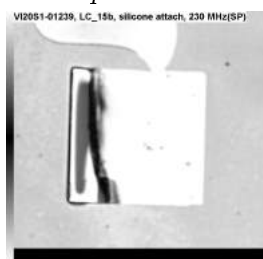
Sample 8 SAM



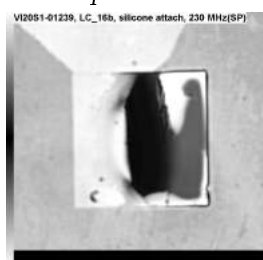
Sample 11 SAM



Sample 12 SAM



Sample 15 SAM



Sample 16 SAM



Sample 8 shear test



Sample 11 shear test



Sample 12 shear test



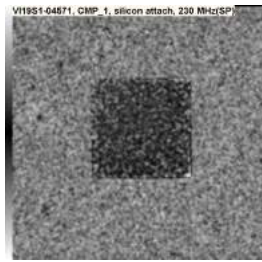
Sample 15 shear test



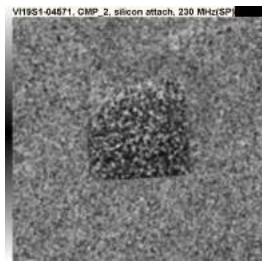
Sample 16 shear test

Figure B.12. SAM images and images of the samples after the shear test for the CP3 bonding DoE.

B.5 CMP DoE



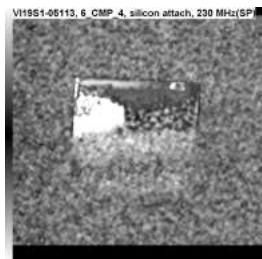
Sample 1 SAM



Sample 2 SAM



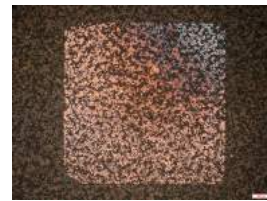
Sample 3 SAM



Sample 4 SAM



Sample 5 SAM



Sample 1 shear test



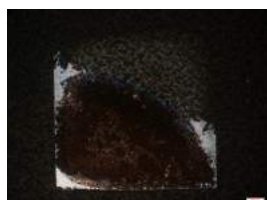
Sample 2 shear test



Sample 3 shear test



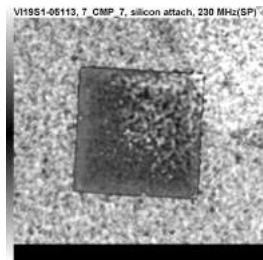
Sample 4 shear test



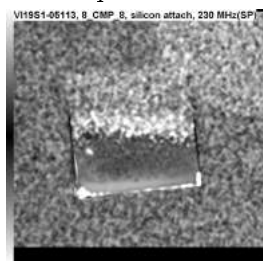
Sample 5 shear test



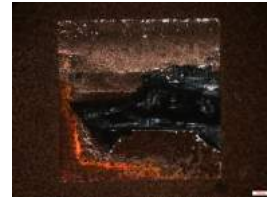
Sample 6 SAM



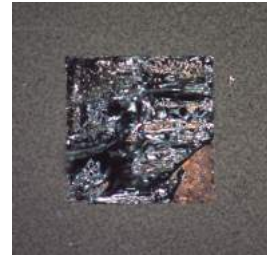
Sample 7 SAM



Sample 8 SAM



Sample 6 shear test



Sample 7 shear test



Sample 8 shear test

Figure B.13. SAM images and images of the samples after the shear test for the CMP bonding DoE.